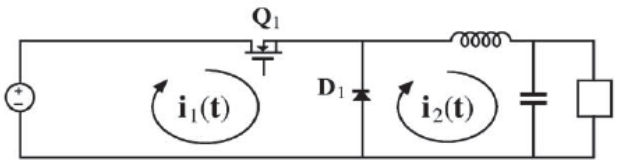
Outline

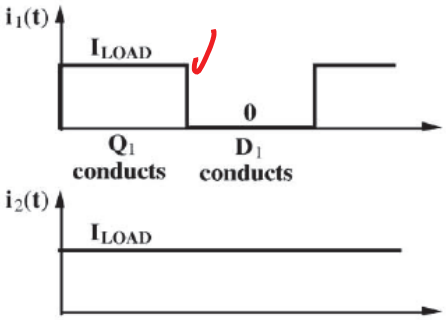
1. Power Converter Layout
2. Loss Analysis and Design
   - Low Frequency Conduction Losses
   - Inductor AC Losses
   - Core Losses
   - Inductor Design Approaches

POWER CONVERTER LAYOUT

Power Converter Layout: Buck Example

Use loop analysis





switched input current $i_1(t)$ contains large high frequency harmonics

—hence inductance of input loop is critical

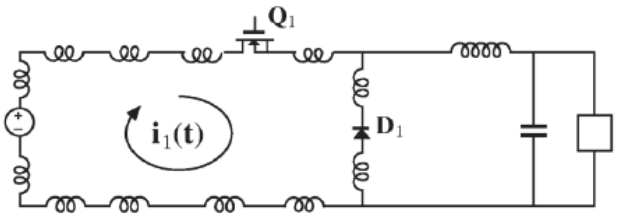
inductance causes ringing, voltage spikes, switching loss, generation of B- and E-fields, radiated EMI

the second loop contains a filter inductor, and hence its current $i_2(t)$ is nearly dc

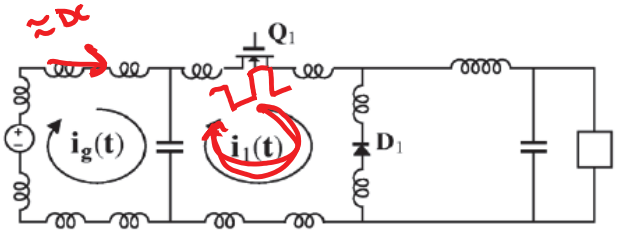
—hence additional inductance is not a significant problem in the second loop

Parasitic Wire Inductances

Parasitic inductances of input loop explicitly shown:



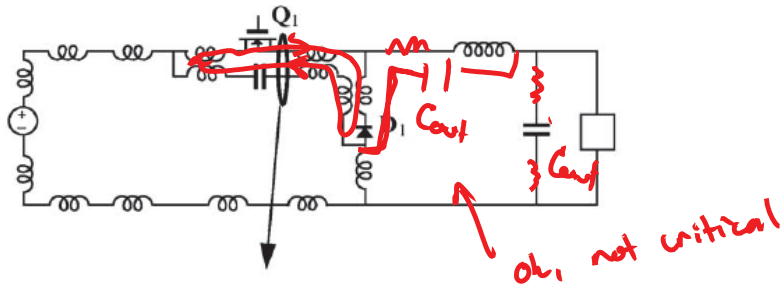
Addition of bypass capacitor confines the pulsating current to a smaller loop:

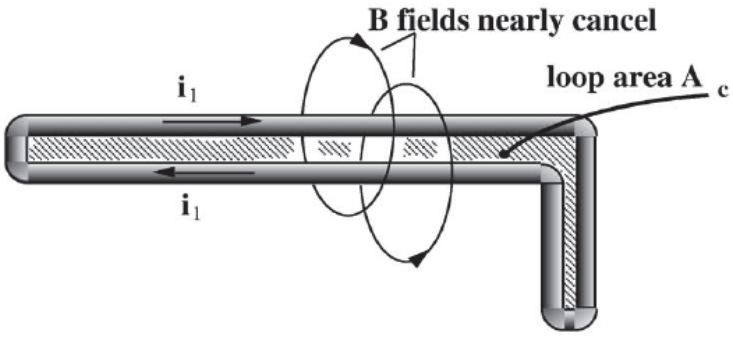


high frequency currents are shunted through capacitor instead of input source

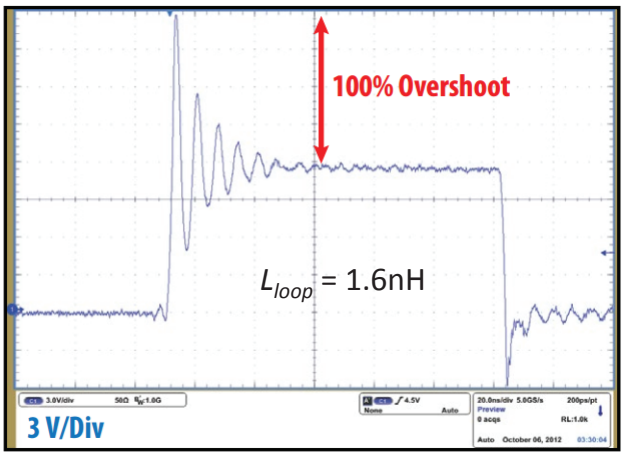
Loop Minimization

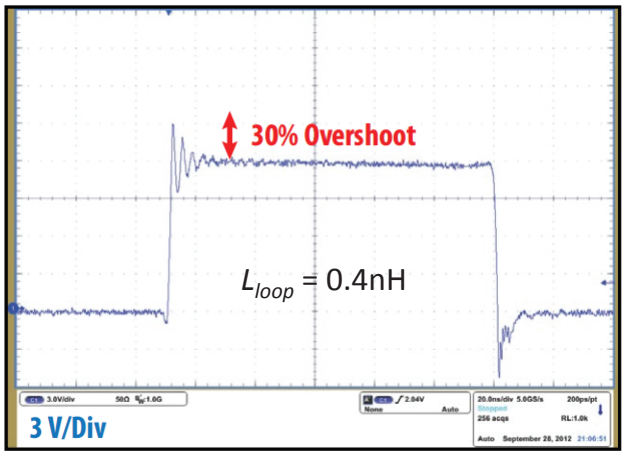
Even better: minimize area of the high frequency loop, thereby minimizing its inductance

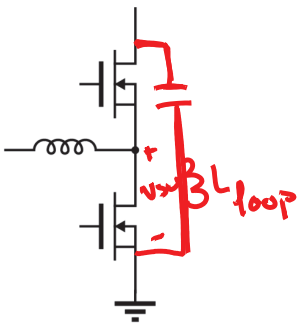


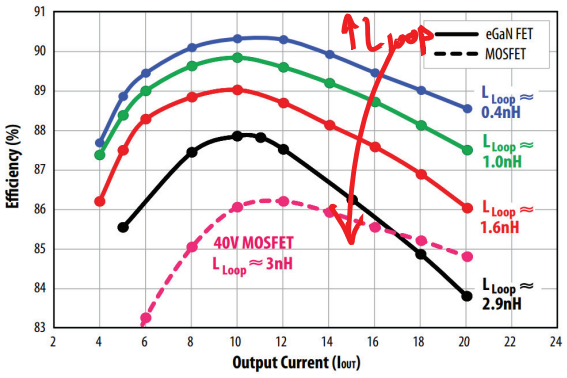


Effect of Loop Inductance

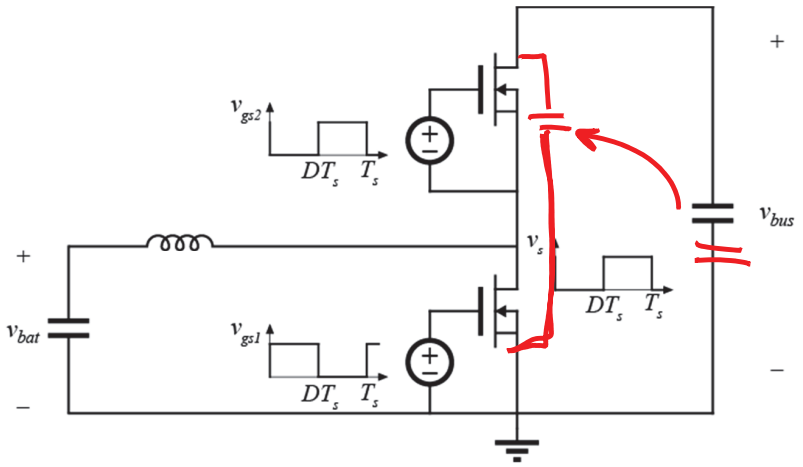






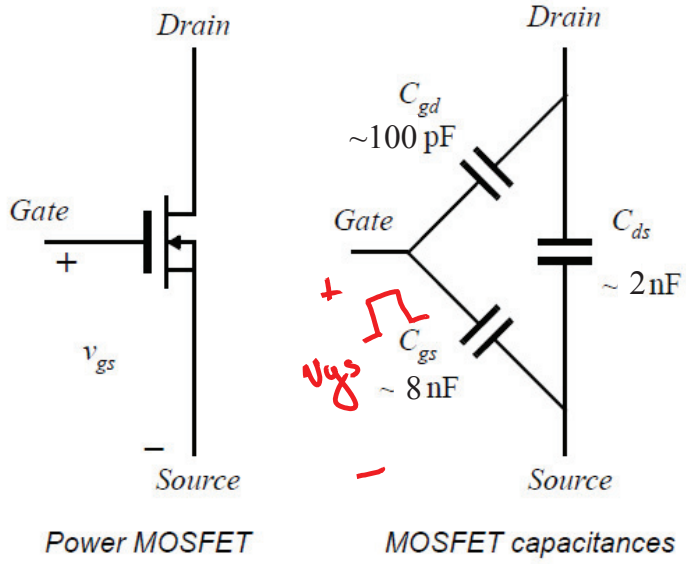


Half Bridge Gate Drive Waveforms



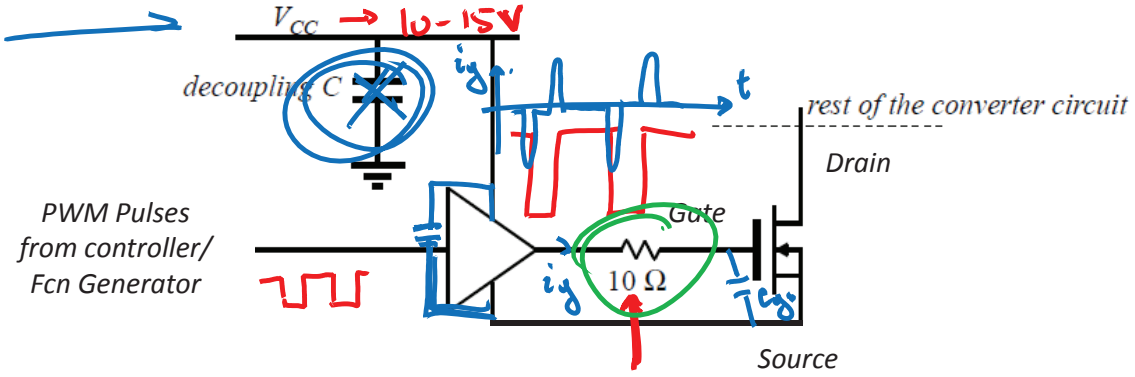
- Gate driver chip must implement v_{gs} waveforms
- Sources will have pulsating currents and need decoupling

Driving a Power MOSFET Switch



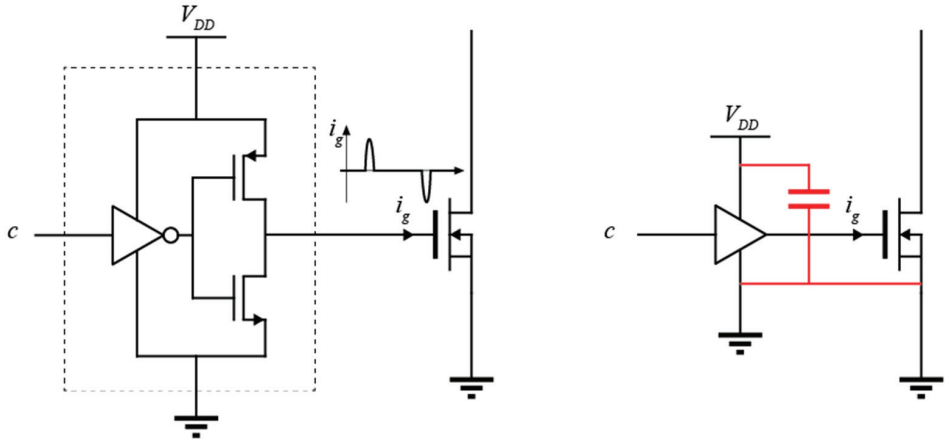
- MOSFET is off when $v_{gs} < V_{th} \approx 3$ V
- MOSFET fully on when v_{gs} is sufficiently large (10-15 V)
- Warning: MOSFET gate oxide breaks down and the device fails when $v_{gs} > 20$ V.
- Fast turn on or turn off (10's of ns) requires a large spike (1-2 A) of gate current to charge or discharge the gate capacitance
- MOSFET gate driver is a logic buffer that has high output current capability

Driving a Power MOSFET Switch



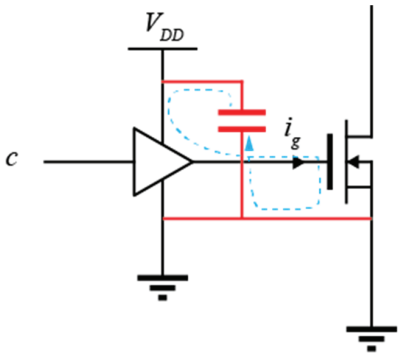
- MOSFET gate driver is used as a logic buffer with high output current (~1.8 A) capability
- The amplitude of the gate voltage equals the supply voltage *VCC*
- Decoupling capacitors are necessary at all supply pins of LM5104 (and all ICs)
- Gate resistance used to slow dv/dt at switch node

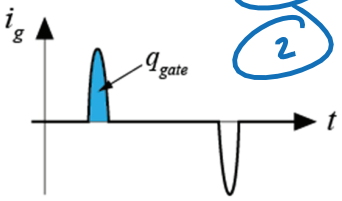
Gate Drive Implementation



- Gate driver is cascaded half-bridges of increasing size to obtain quick rise times
- Reminder: keep loops which handle pulsating current small by decoupling and making close connections

Capacitor Sizing – Pulsed Caps





Most Important loops in Power converter layout

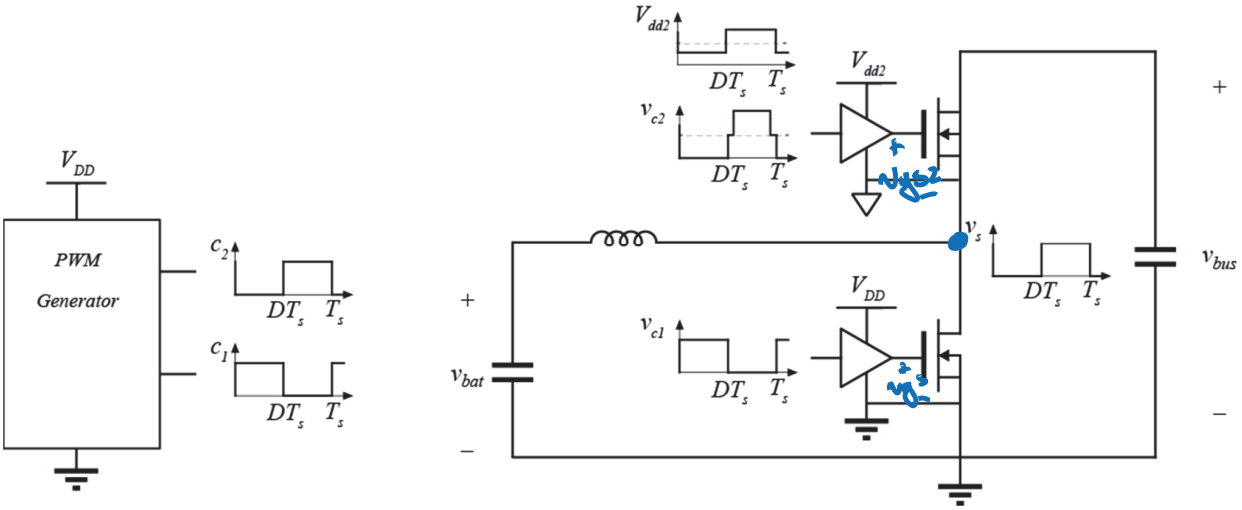
1. Power loop
2. Each gate drive loop

$$\frac{q_{gate}}{\Delta V_{DD}} = C$$

everything else

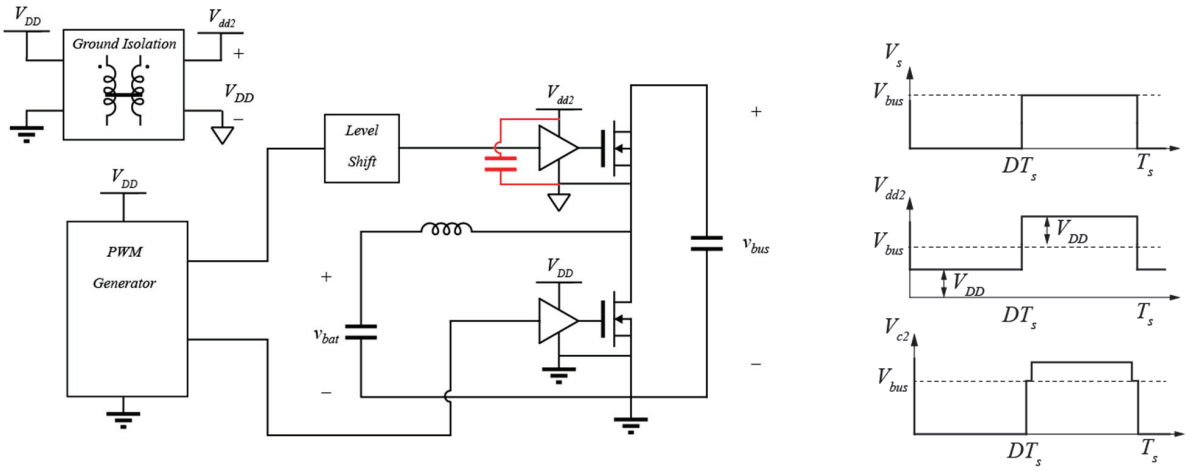
- Area of current pulse is total charge supplied to gate of capacitor
- All charge must be supplied from gate drive decoupling capacitor

High Side Signal Ground



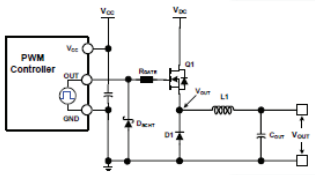
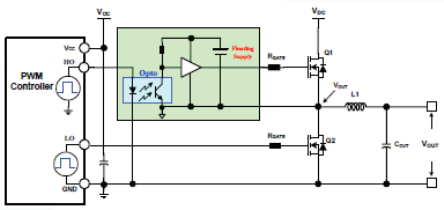
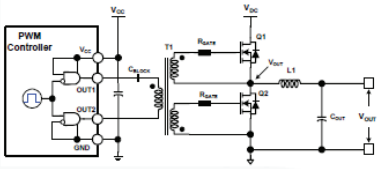
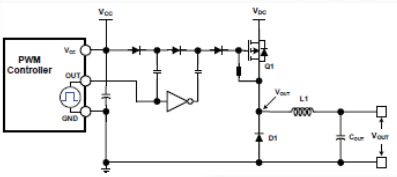
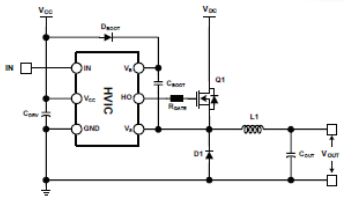
- Gate driver chip must implement v_{gs} waveforms
- Issue: source of Q_2 is not grounded

Generating Floating Supply



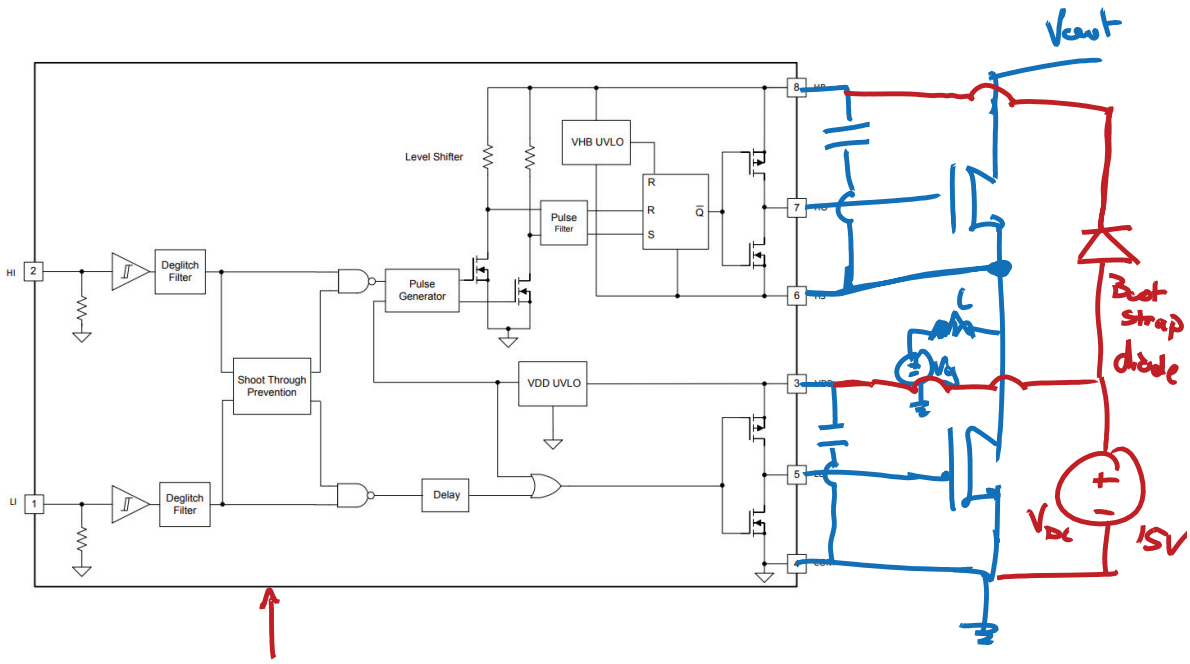
- Isolated supplies sometimes used; Isolated DC-DC, batteries
- Bootstrap concept: capacitor can be charged when V_s is low, then switched

THE UNIVERSITY OF TENNESSEE KNOXVILLE

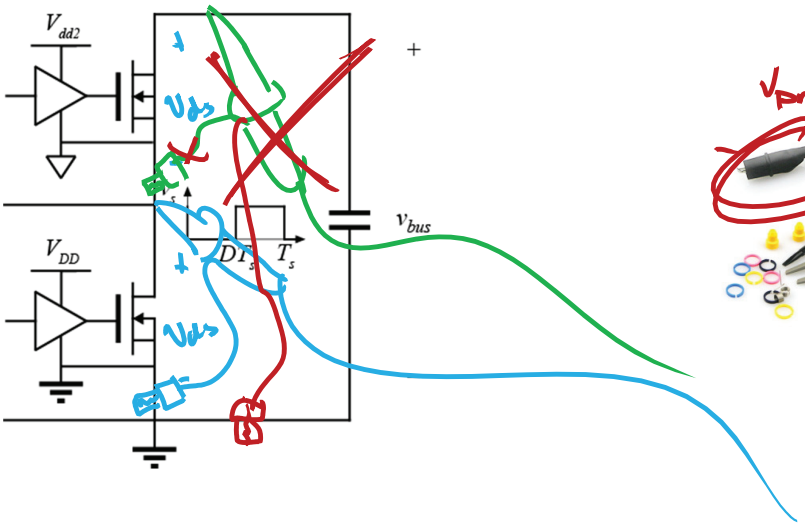
Direct Drive		Easiest high-side application the MOSFEF and can be driven directly by the PWM controller or by a ground referenced driver, but it must meet two conditions, as follows: $V_{CC} < V_{GS,MAX}$ and $V_{DC} < V_{CC} - V_{GS,Miller}$
Floating Supply Gate Drive		Cost impact of isolated supply is significant. Opto-coupler tends to be relatively expensive, limited in bandwidth, and noise sensitive.
Transformer Coupled Drive		Gives full gate control for an indefinite period of time, but is somewhat limited in switching performance. This can be improved with added complexity.
Charge Pump Drive		The turn-on times tend to be long for switching applications. Inefficiencies in the voltage multiplication circuit may require more than low stages of pumping.
Bootstrap Drive		Simple and inexpensive with limitations; such as, the duty cycle and on-time are both constrained by the need to refresh the bootstrap capacitor. Requires level shift, with the associated difficulties.

Fairchild Semi App Note AN-6076

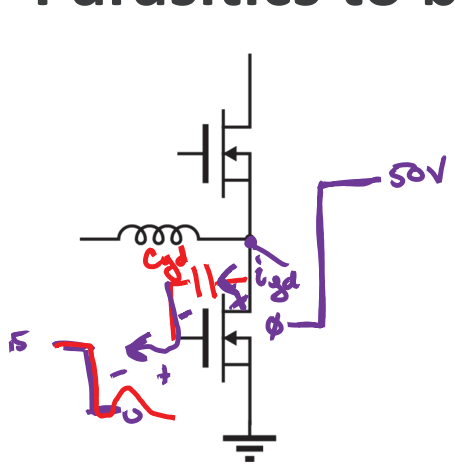
UCC27712 Internal Diagram



A Note on Grounding



Parasitics to be Aware of

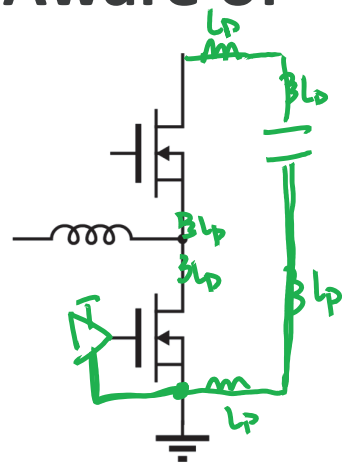


Cross-talk from Cgd

Remedy:

↓ gate driver turn-off impedance

↑ High side FETs turn-on impedance

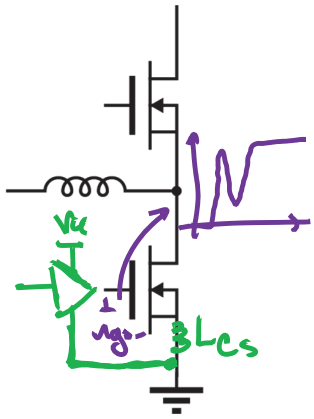


power loop inductance

Remedy:

↓ loop area

- Moving or adding capacitors

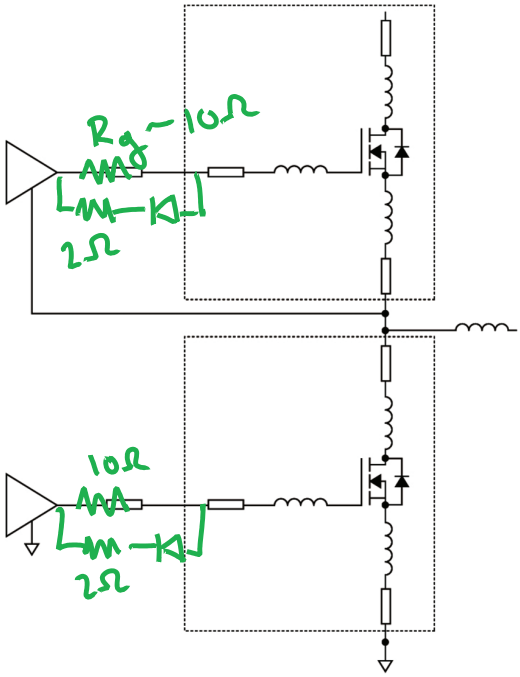


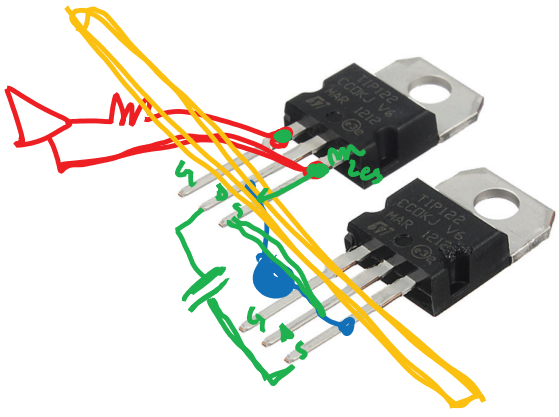
Common-Source Inductance

Remedy

- ↓ Lcs
- ↑ Turn-on resistance

Power Loop Inductances





Persson E., "What really limits MOSFET performance: silicon, package, driver or circuit board?"

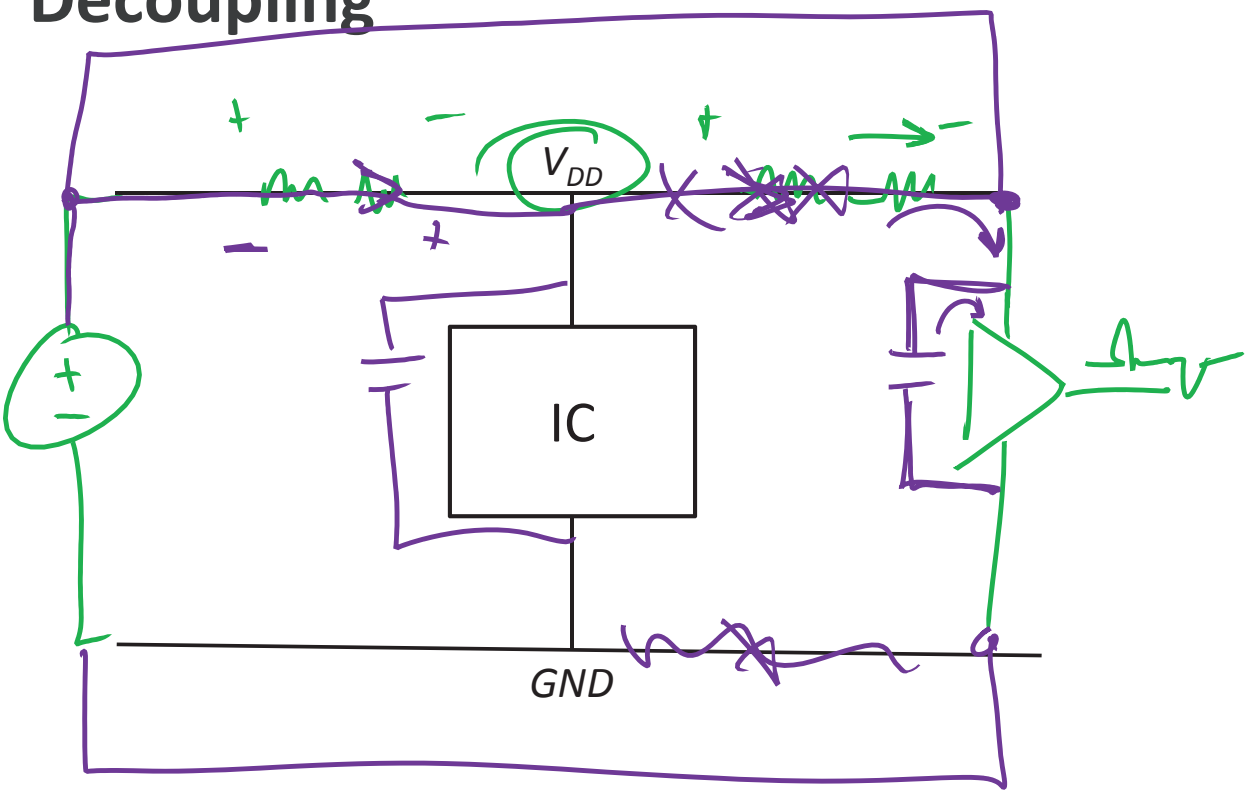
Complete Routing of Signal

- Always consider return path
- Ground plane can help, but still need to consider the path and optimize

Decoupling

- Always add bypass capacitor at power supply for any IC/reference
- Use small-valued (~100nf), low ESR and ESL capacitors (ceramic)
- Limit loop for any di/dt

Decoupling



Star-Grounding Vs. Daisy Chain

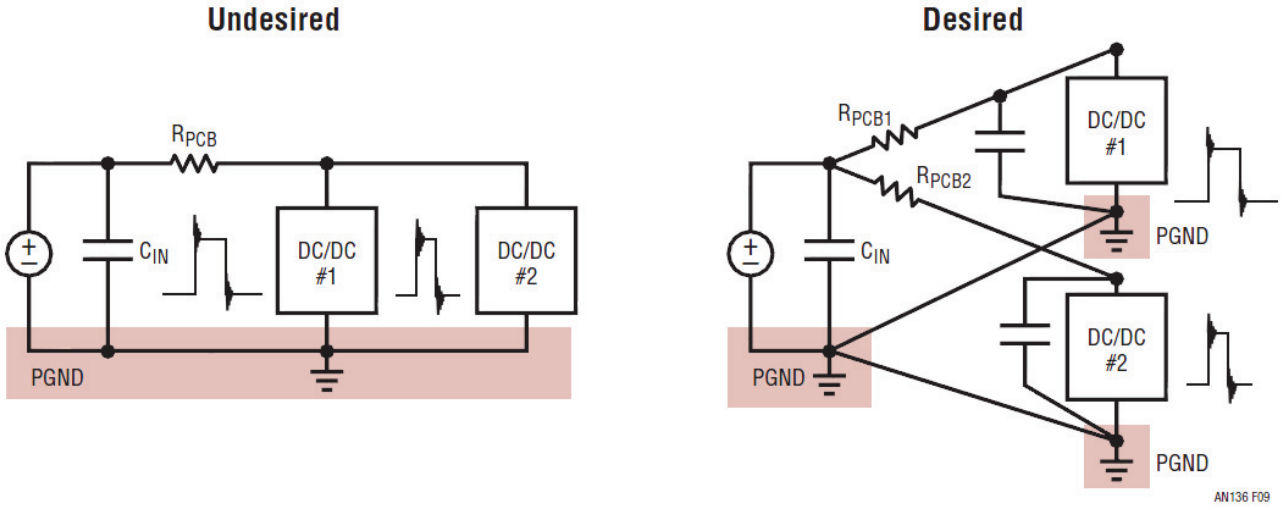
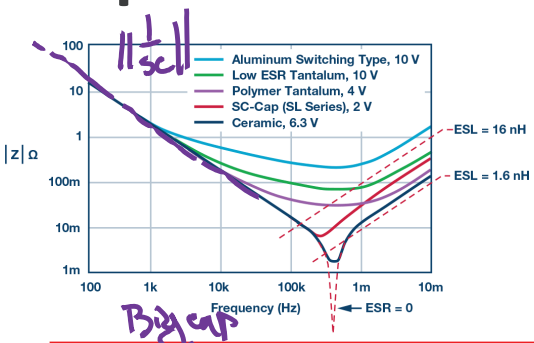


Figure 9. Separate the Input Current Paths Among Supplies

Capacitor Sizing – Filter Caps



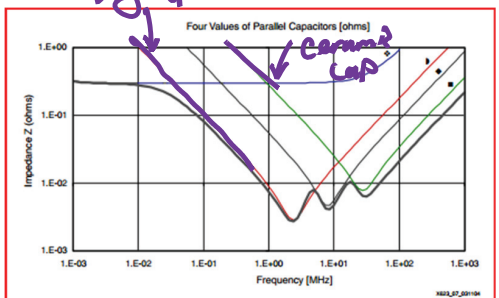


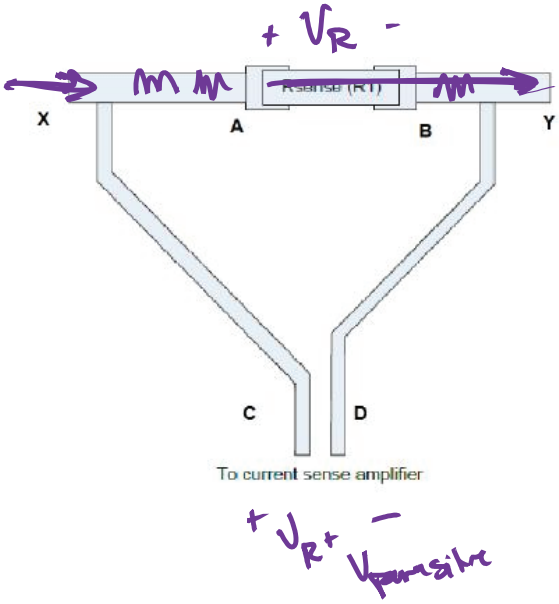
Figure 8: **PDS Impedance Versus Frequency Plot**

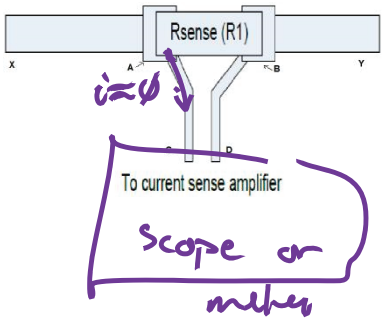
Table 8: **Values Used in Impedance Plot of Figure 8**

Quantity	Symbol	Package	Capacitive Values (µF)	Parasitic Inductance (nH)	Parasitic Resistance (ohms)
2	❖	E	680	2.8	0.57
7	◗	0805	2.2	2.0	0.02
13	◆	0603	0.22	1.8	0.06
26	■	0402	0.022	1.5	0.20

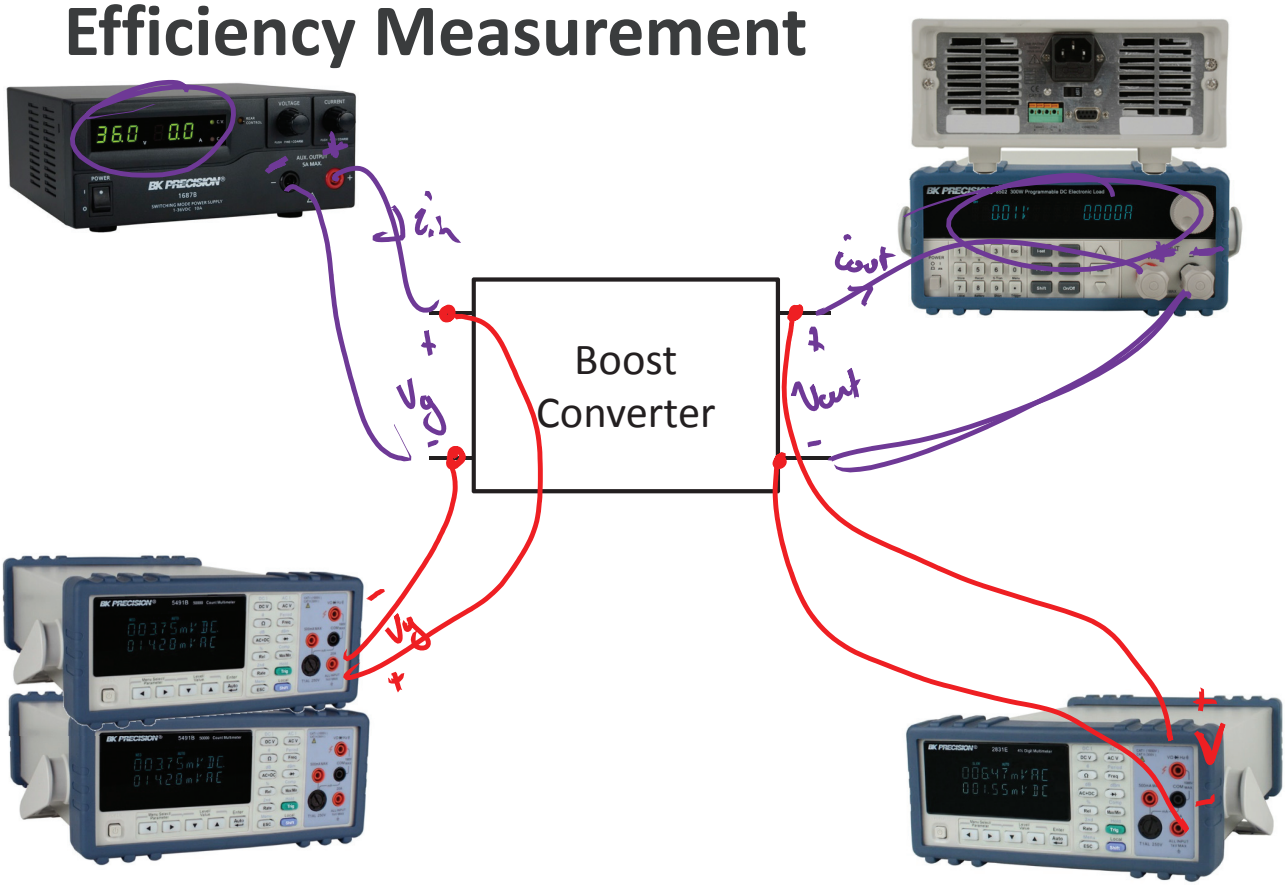
https://www.intersil.com/content/dam/Intersil/documents/an13/an1325.pdf

Kelvin Connection

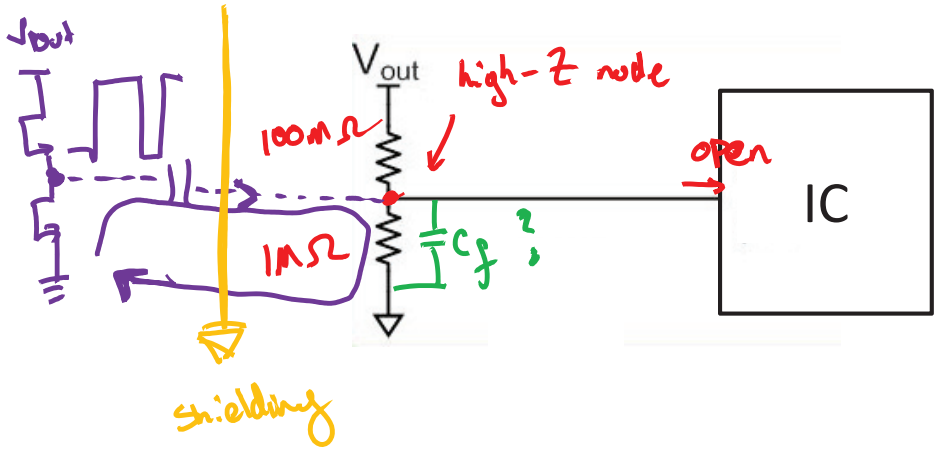




Efficiency Measurement

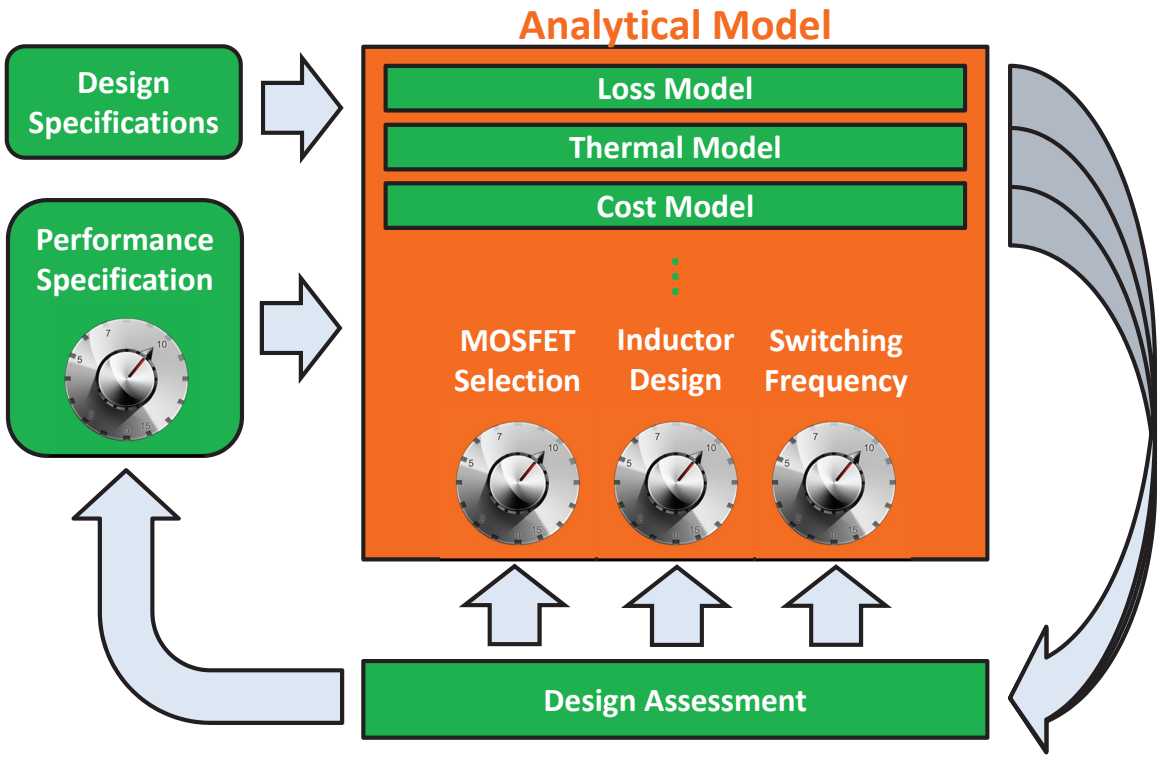


High Impedance Nodes



POWER CONVERTER DESIGN AND LOSS ANALYSIS

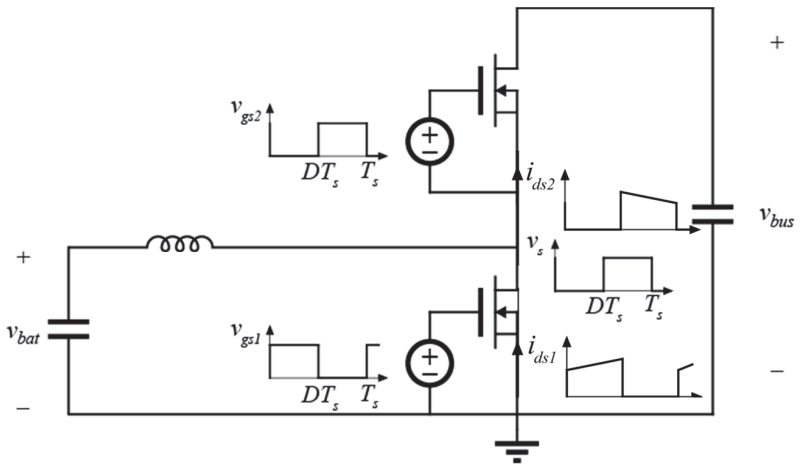
Converter Design



Analytical Loss Modeling

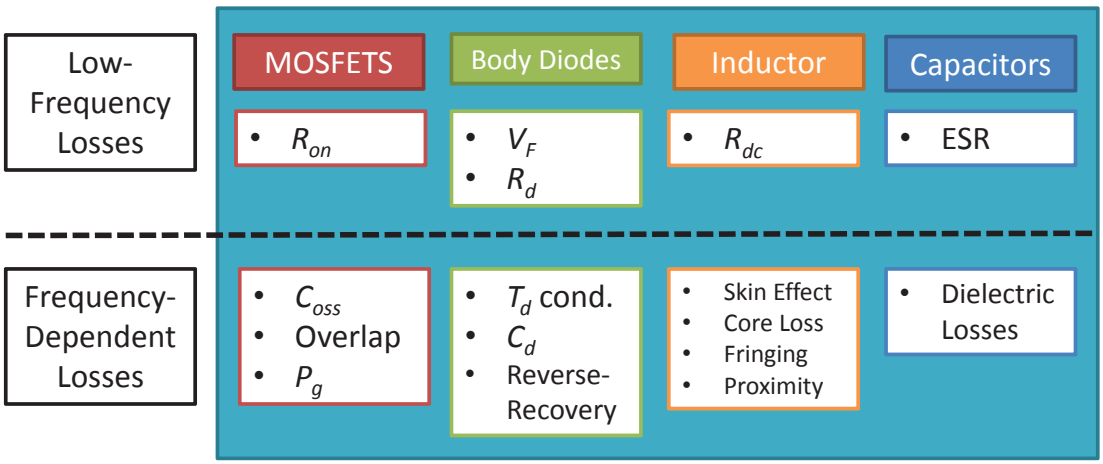
- High efficiency approximation is acceptable for hand calculations, as long as it is justified
  - Solve ideal waveforms of lossless converter, then calculate losses
- Argue which losses need to be included, and which may be neglected
  - “Rough” approximation to gain insight into significance

Boost Converter Loss Analysis



- Begin by solving important waveforms throughout converter assuming lossless operation

Power Stage Losses



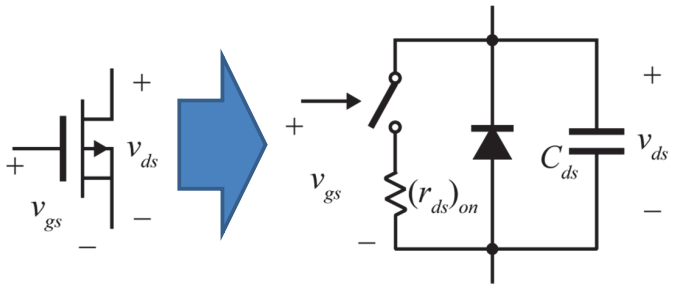
Supplemental Lectures

Device	Loss Mechanism	ECE 481	ECE 581
MOSFET	R_{on}	Lecture 7-8	
	C_{oss}		Lecture 7
	Overlap		Lecture 5-6
	P_g		Lecture 5
Diode	V_F	Lecture 7-8	
	R_d	Lecture 7-8	
	t_d cond		Lecture 5
	C_d		Lecture 7 (see: C_{oss})
	Reverse-Recovery	Lecture 11	
Inductor	R_{dc}	Lecture 38	
	Skin Effect	Lecture 39	
	Core Loss	Lecture 39	
	Fringing		
	Proximity	Lecture 39	

ECE581: http://web.eecs.utk.edu/~dcostine/ECE581/Fall2018/schedule.php
ECE481: http://web.eecs.utk.edu/~dcostine/ECE481/Fall2017/schedule.php

LOW FREQUENCY CONDUCTION LOSSES

MOSFET Equivalent Circuit



- Considering only power stage losses (gate drive neglected)
- MOSFET operated as power switch
- Intrinsic body diode behaviors considered using normal diode analysis

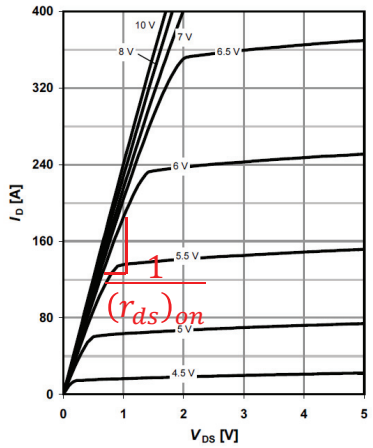
Datasheet Interpretation

Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=50 A	-	16	20	mΩ
		V_{GS}=8 V, I_D=25 A	-	16	20	

5 Typ. output characteristics

$I_D=f(V_{DS})$; T_j=25 °C

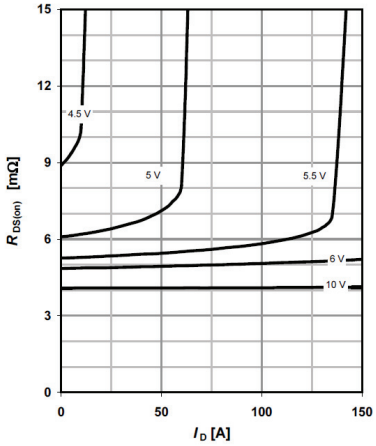
parameter: V_{GS}



6 Typ. drain-source on resistance

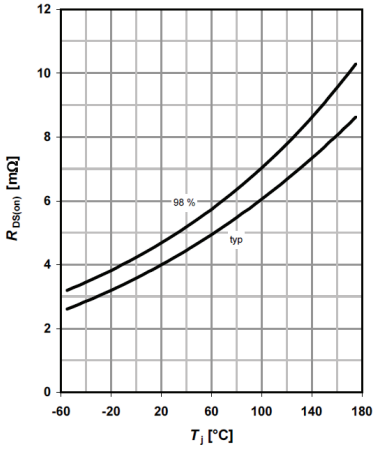
$R_{DS(on)}=f(I_D)$; T_j=25 °C

parameter: V_{GS}



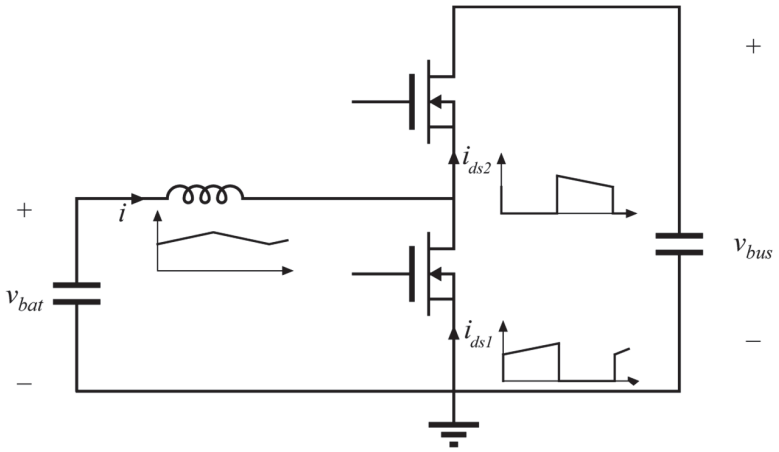
9 Drain-source on-state resistance

$R_{DS(on)}=f(T_j)$; I_D=100 A; V_{GS}=10 V



- On resistance extracted from datasheet waveforms
- Significantly dependent on V_{gs} amplitude, temperature

Boost Converter RMS Currents



- MOSFET conduction losses due to $(r_{ds})_{on}$ depend given as

$$P_{cond,FET} = {I_{di,rms}}^2 (r_{ds})_{on}$$

MOSFET Conduction Losses

Pulsating waveform with linear ripple, Fig. A.6:

$$rms = I\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i}{I}\right)^2} \quad \text{(A.6)}$$

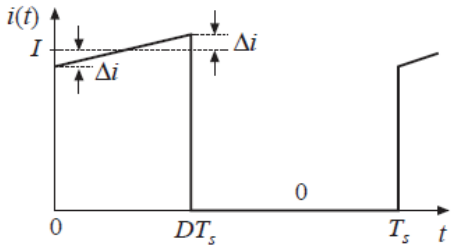
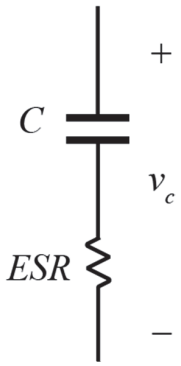
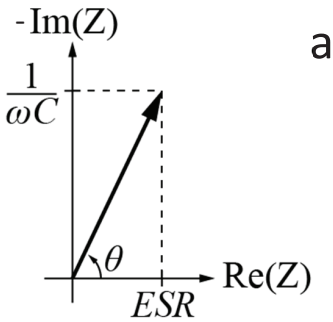


Fig. A.6

- RMS values of commonly observed waveforms appendix from Power Book

Capacitor Loss Model



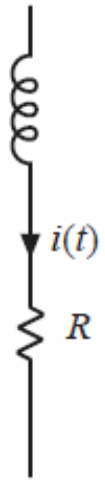


- Operation well below resonance
- All loss mechanisms in a capacitor are generally lumped into an empirical loss model
- Equivalent Series Resistance (ESR) is *highly* frequency dependent
- Datasheets may give effective impedance at a frequency, or loss factor:

$$\delta = \frac{\pi}{2} - \theta$$

$$D = \tan(\delta)$$

DC Inductor Resistance



- DC Resistance given by

$$R_{DC} = \rho \frac{l_b}{A_w}$$

- At room temp, ρ = 1.724·10^{-6} Ω-cm
- At 100°C, ρ = 2.3·10^{-6} Ω-cm

- Losses due to DC current:

$$P_{cu,DC} = {I_{L,rms}}^2 R_{DC}$$

Inductor Conduction Losses

DC plus linear ripple, Fig. A.2:

$$rms = I\sqrt{1 + \frac{1}{3}\left(\frac{\Delta i}{I}\right)^2} \qquad \text{(A.2)}$$

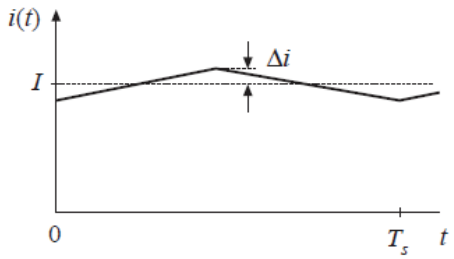
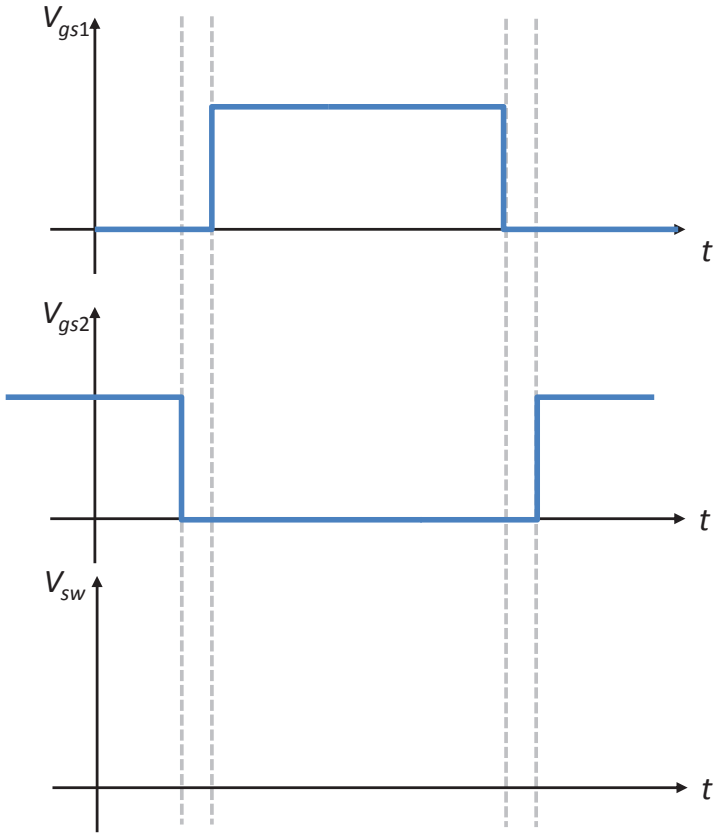


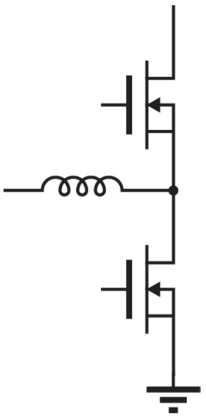
Fig. A.2

- Conduction losses dependent on RMS current through inductor

Switching Loss

Switching Loss Modeling





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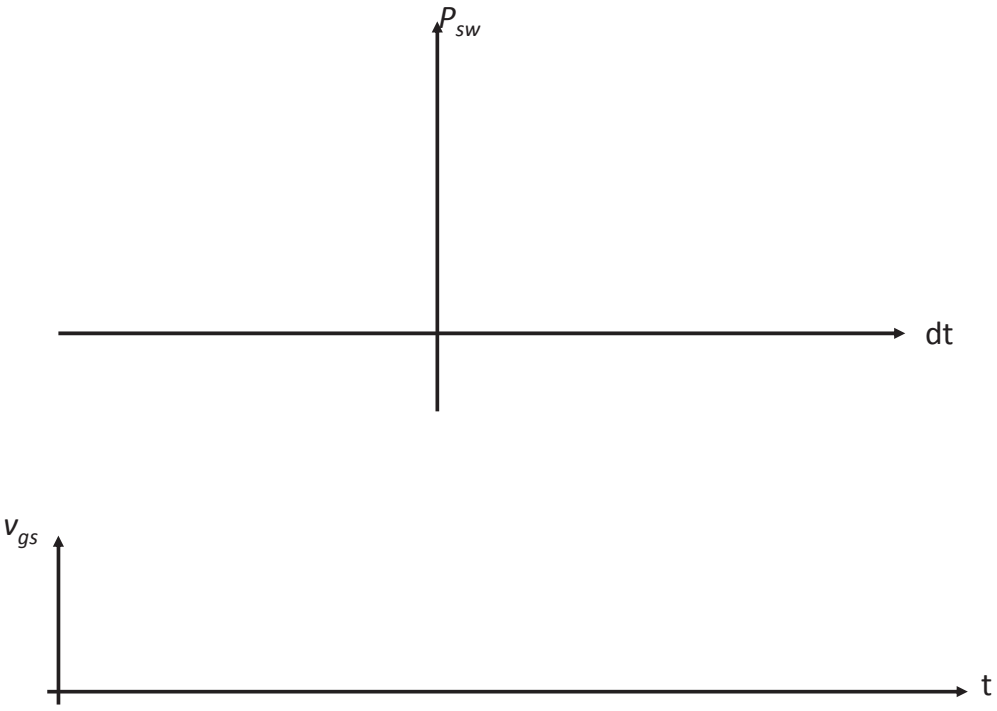
Dead Time Selection



Types of Switching Loss

1. Gate Charge Loss
2. Overlap Loss
3. Capacitive Loss
4. Body Diode Conduction
5. Reverse Recovery
6. Parasitic Inductive Losses
7. Anomalous Losses

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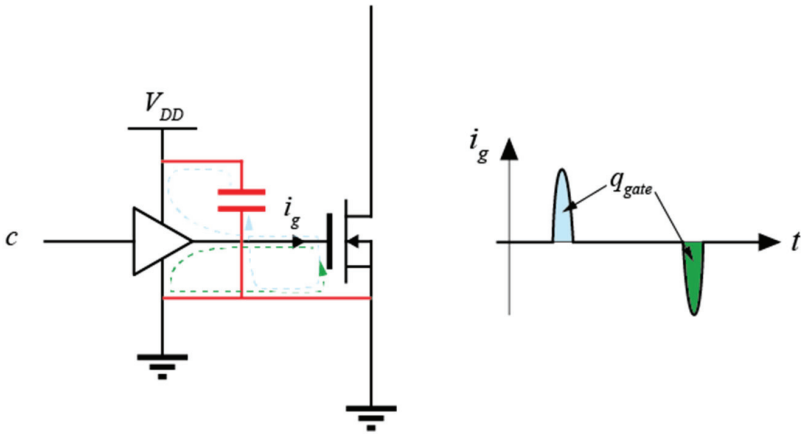
Gate Drive Losses



$$E_{loss} = q_{gate} V_{DD}$$

$$P_{sw,g} = E_{loss} f_s$$

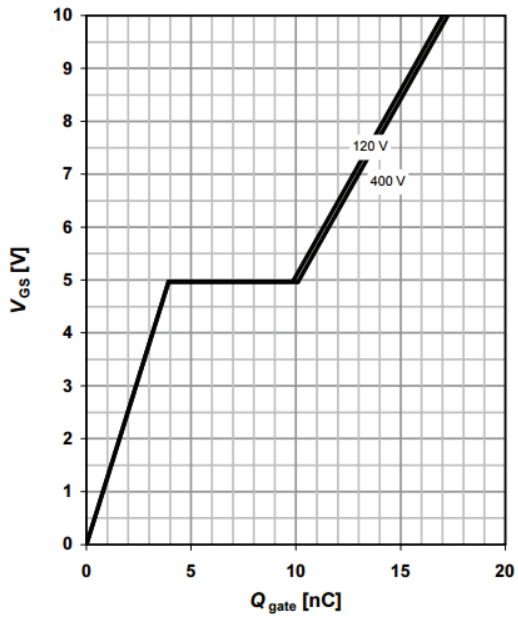
- Gate charge is supplied through driver resistance during switch turn-on
- Gate charge is dissipated in gate driver on switch turn-off

Gate Charge Loss

9 Typ. gate charge

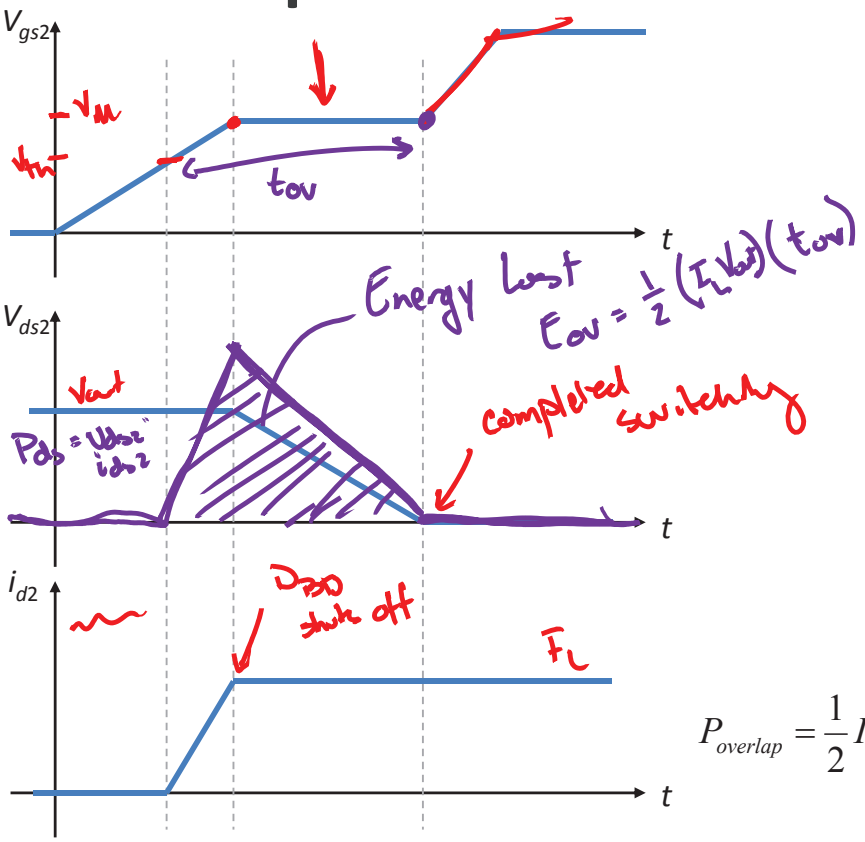
V_{GS}=f(Q_{gate}); I_D=5.2 A pulsed

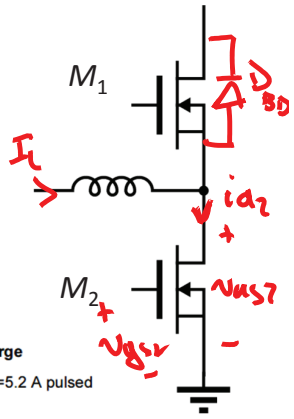
parameter: V_{DD}

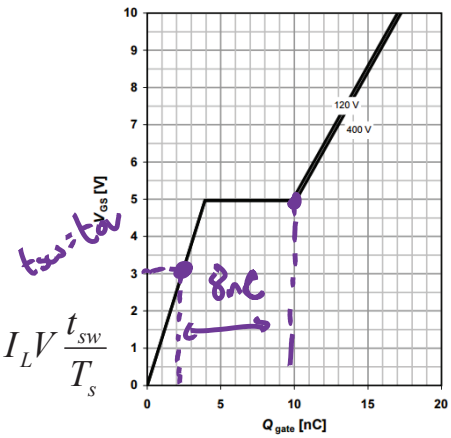


$$P_g = Q_g V_{cc} f_s$$

Overlap Loss



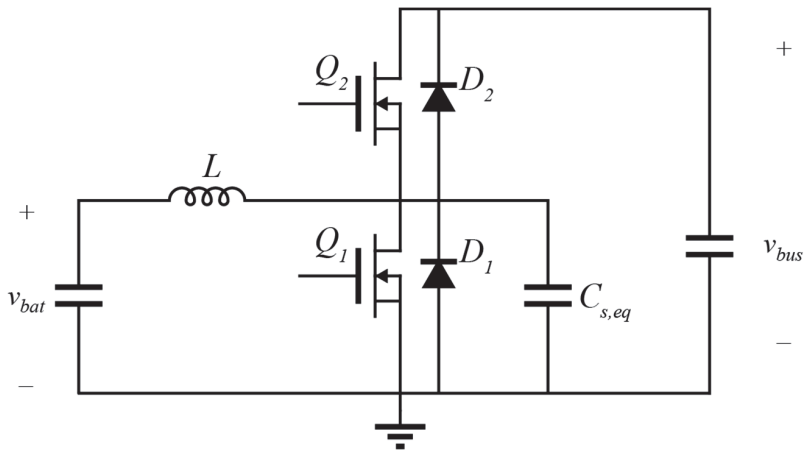




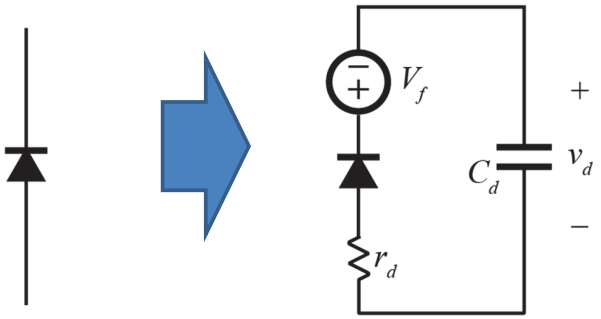
$$P_{overlap} = \frac{1}{2} I_L V \frac{t_{sw}}{T_s}$$

Lump Switched Node Capacitance

- Consider a single equivalent capacitor at switched node which combines energy storage due to all four semiconductor devices



Diode Loss Model



- Example loss model includes resistance and forward voltage drop extracted from datasheet

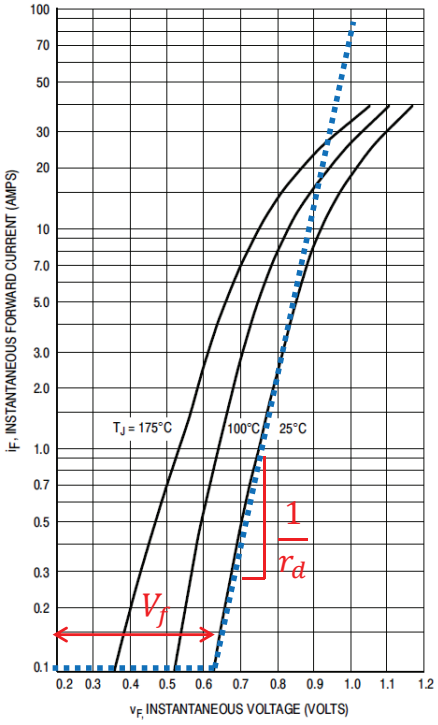
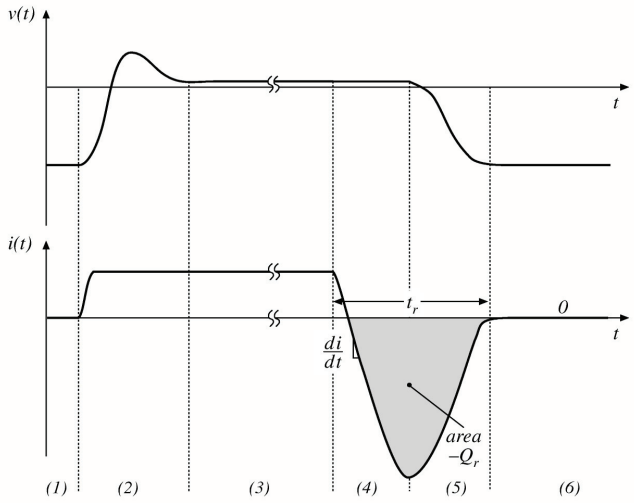


Figure 1. Typical Forward Voltage

Diode Reverse Recovery

- FET body diodes may turn on during dead time intervals
- Significant reverse recovery losses possible



$$E_{on,rr} = \left(\left(I_L - \Delta i_L \right) t_{rr} + Q_{rr} \right) V_{bus}$$

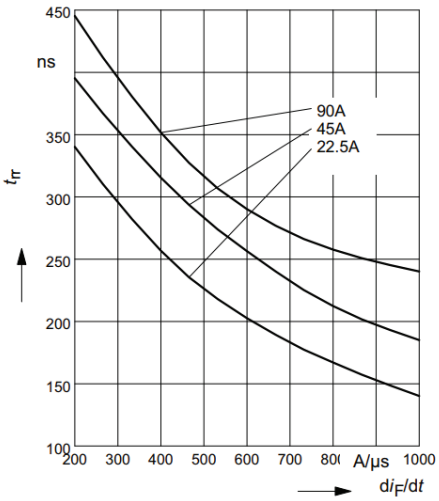
Reverse Recovery - Datasheet

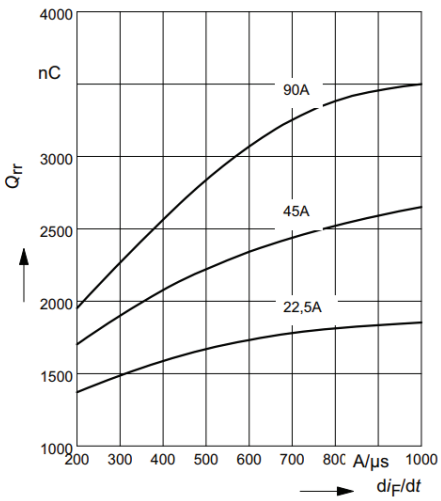
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Dynamic Characteristics					
Reverse recovery time	t_{rr}				ns
V_R=400V, I_F=45A, di_F/dt=1000A/µs, T_j=25°C		-	140	-	
V_R=400V, I_F=45A, di_F/dt=1000A/µs, T_j=125°C		-	185	-	
V_R=400V, I_F=45A, di_F/dt=1000A/µs, T_j=150°C		-	195	-	
Reverse recovery charge	Q_{rr}				nC
V_R=400V, I_F=45A, di_F/dt=1000A/µs, T_j=25°C		-	1400	-	
V_R=400V, I_F =45A, di_F/dt=1000A/µs, T_j=125°C		-	2650	-	
V_R=400V, I_F =45A, di_F/dt=1000A/µs, T_j=150°C		-	2900	-	

5 Typ. reverse recovery time

$t_{rr} = f\,(di_F/dt)$

parameter: V_R = 400V, T_j = 125°



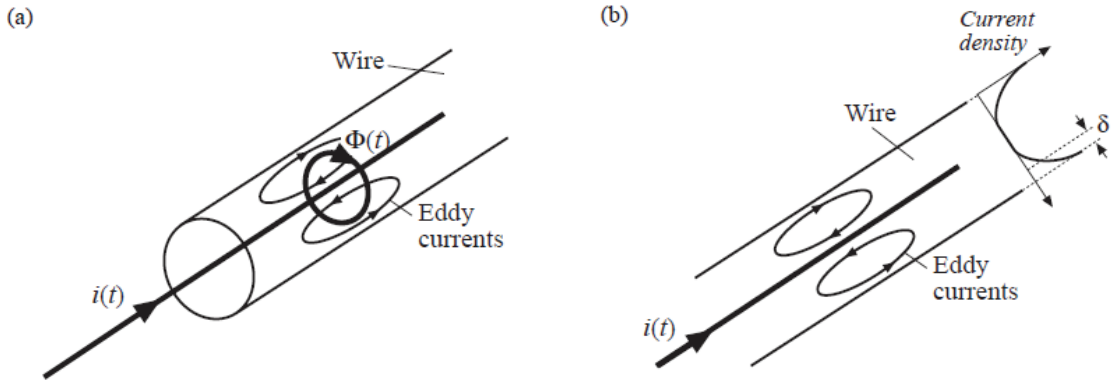


Reverse Recovery – Rough Approximations

- $E_{rr} \approx E_{rr\_datasheet} \dfrac{I_F}{I_{F\_datasheet}} \dfrac{V_{DC}}{V_{DC\_datasheet}}$
- **Rough** approximation with $I_F \ll I_{max}$

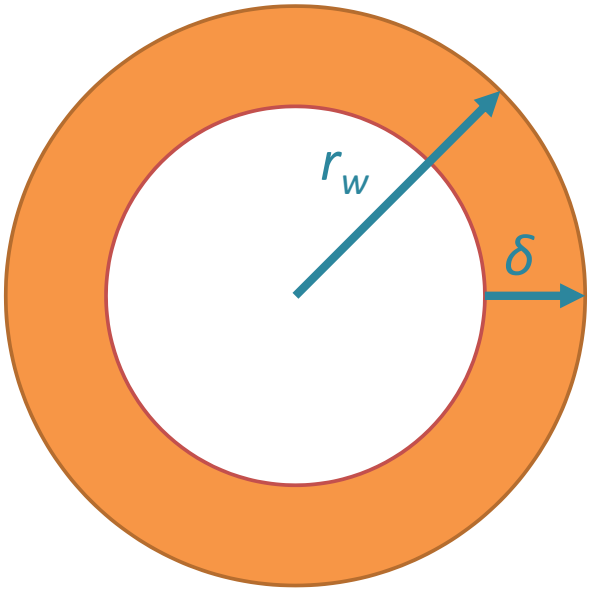
INDUCTOR AC LOSSES

Skin Effect in Copper Wire



- Current profile at high frequency is exponential function of distance from center with characteristic length δ

AC Resistance



$$A_{w,eff} = \pi {r_w}^2 - \pi(r_w - \delta)^2$$

$$R_{ac} = \rho \frac{l_b}{A_{w,eff}}$$

Skin Depth

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}}$$

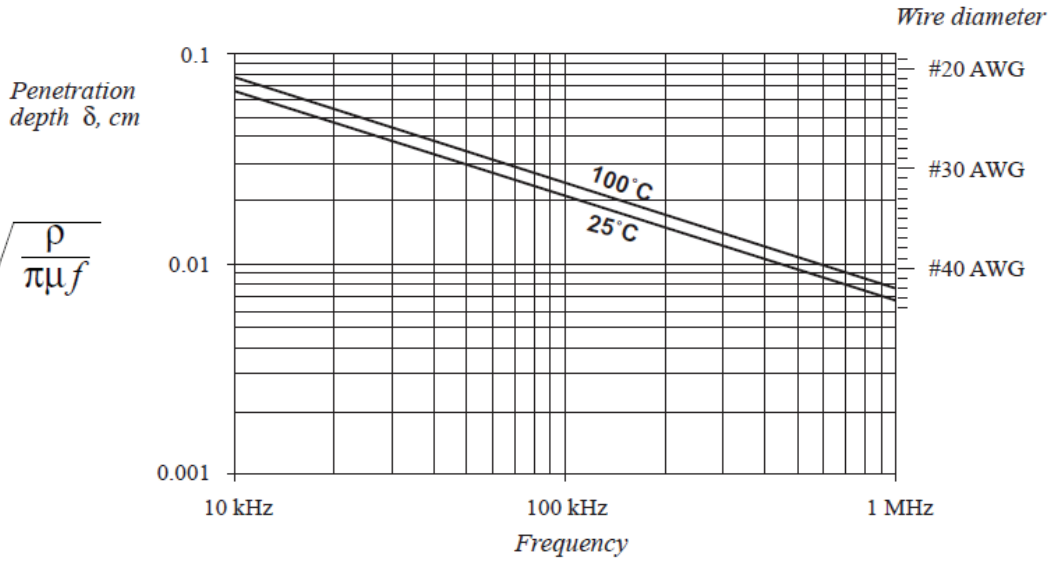
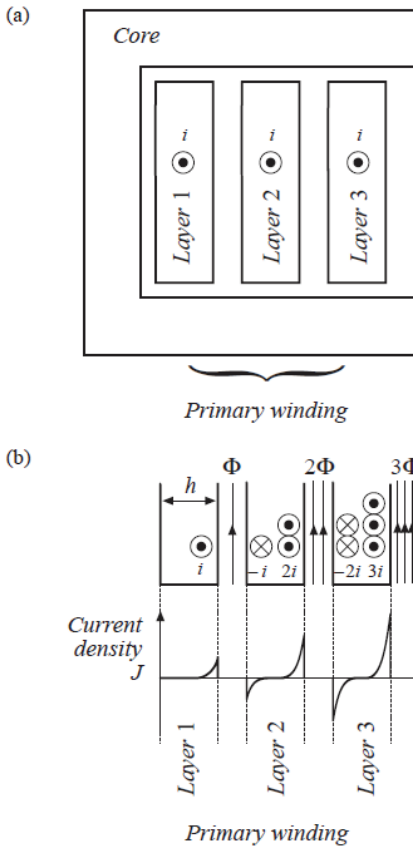


Fig. 13.23 Penetration depth δ, as a function of frequency *f*, for copper wire.

Proximity Effect



- In *foil* conductor closely spaced with $h >> \delta$, flux between layers generates additional current according to Lentz's law.

$$P_1 = I_{L,rms}{}^2 R_{ac}$$

- Power loss in layer 2:

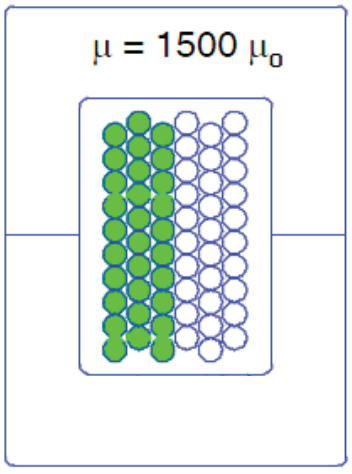
$$P_2 = I_{L,rms}{}^2 R_{ac} + \left(2 I_{L,rms}\right)^2 R_{ac}$$

$$P_2 = 5 P_1$$

- Needs modification for non-foil conductors

See *Fundamentals of Power Electronics*, Section 13.4

Simulation Example



- AWG#30 copper wire
  - Diameter d = 0.294 mm
  - $d = \delta$ at around 50 kHz
- 1:1 transformer
  - Primary and secondary are the same, 30 turns in 3 layers
- Sinusoidal currents,

$I_{1rms} = I_{2rms} = 1$ A

Numerical field and current density solutions using FEMM (Finite Element Method Magnetics), a free 2D solver, http://www.femm.info/wiki/HomePage

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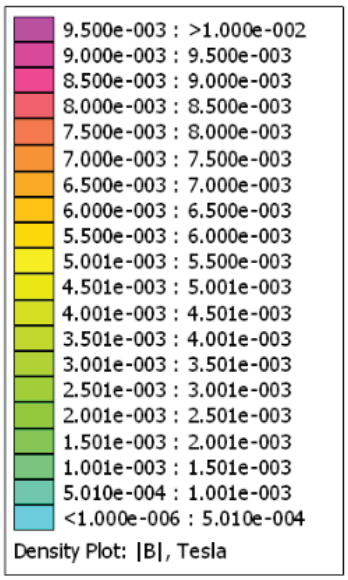
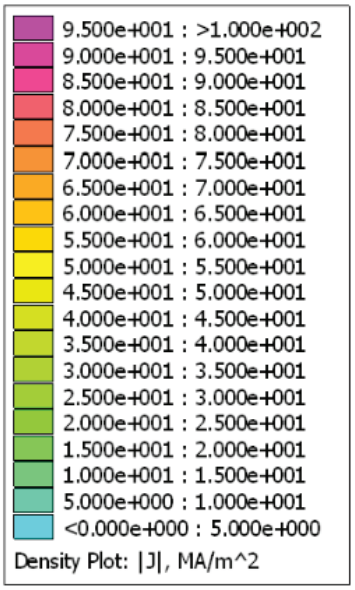
Flux density magnitude

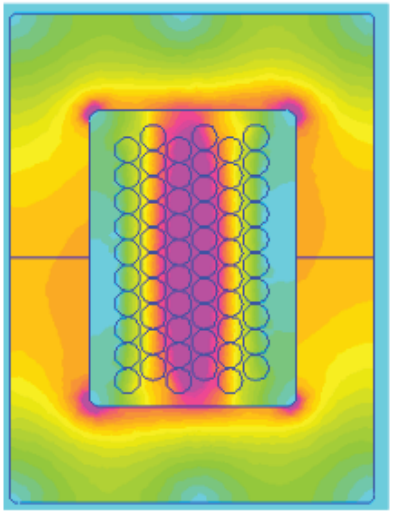


Current density magnitude

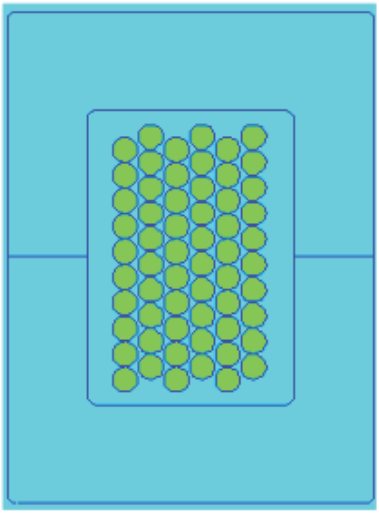


Frequency: 1 kHz

Flux density

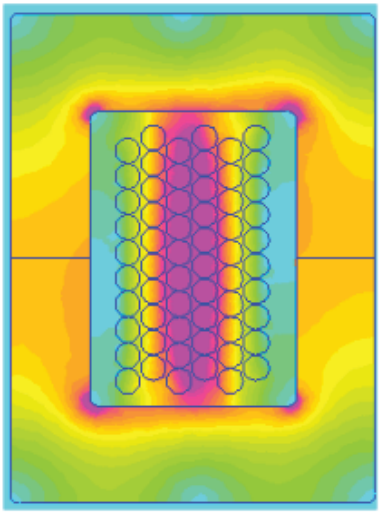


Current Density

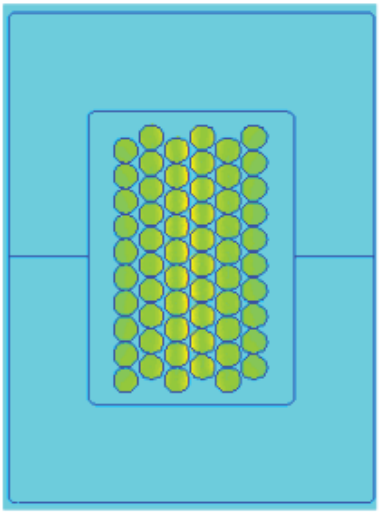


Frequency: 100 kHz

Flux density



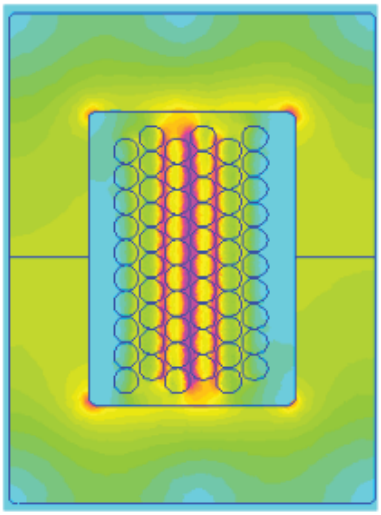
Current Density



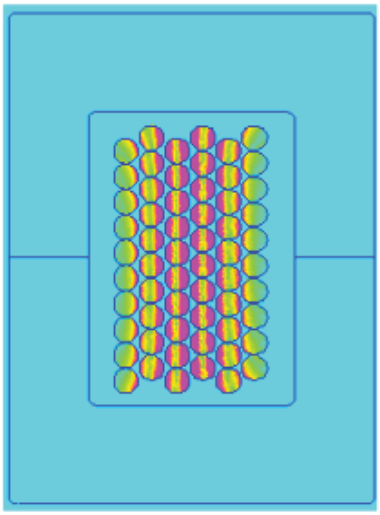
Total copper losses 1.8 larger than at 1 kHz

Frequency: 1 MHz

Flux density

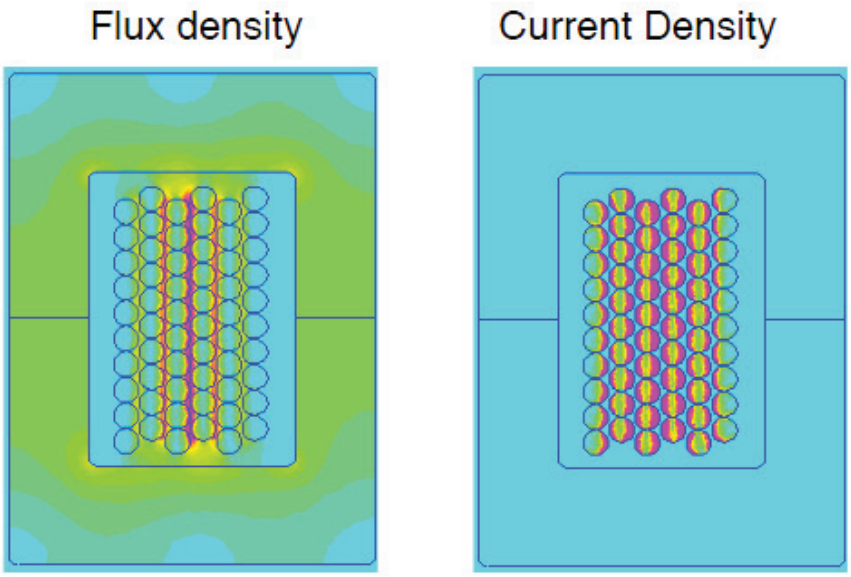


Current Density



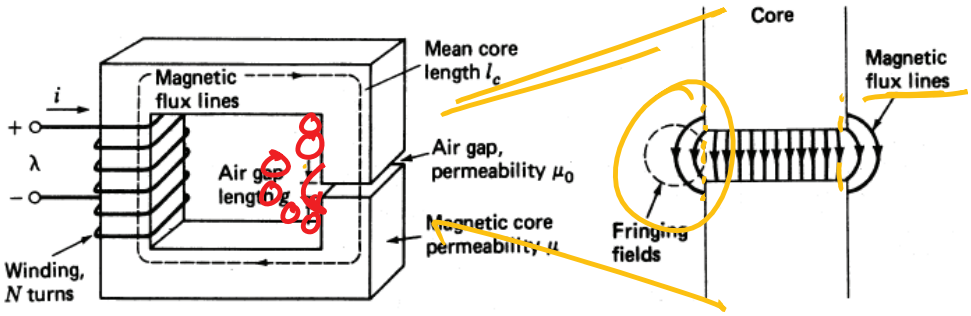
Total copper losses 20 times larger than at 1 kHz

Frequency: 10 MHz



Very significant proximity effect
Total copper losses = 65 times larger than at 1 KHz

Fringing

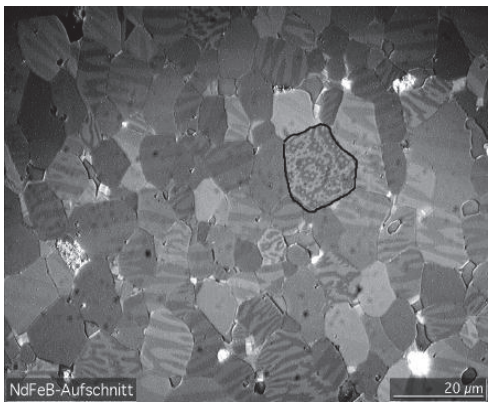


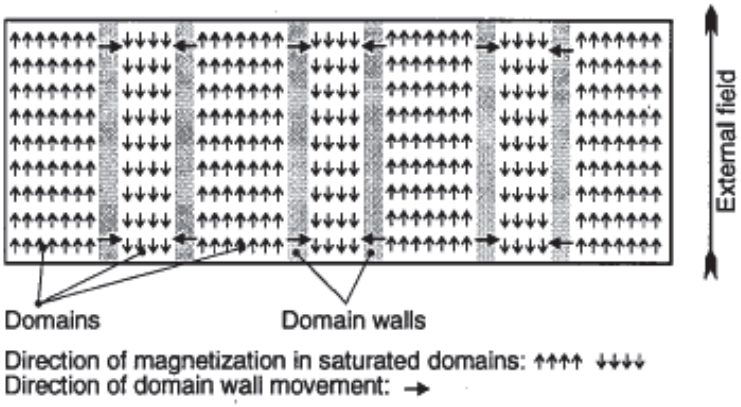
A simple magnetic circuit with an air gap

- Near air gap, flux may bow out significantly, causing additional eddy current losses in nearby conductors

Physical Origin of Core Loss

- Magnetic material is divided into “domains” of saturated material
- Both Hysteresis and Eddy Current losses occur from domain wall shifting





Reinert, J.; Brockmeyer, A.; De Doncker, R.W.; , "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation,"

Inductor Core Loss

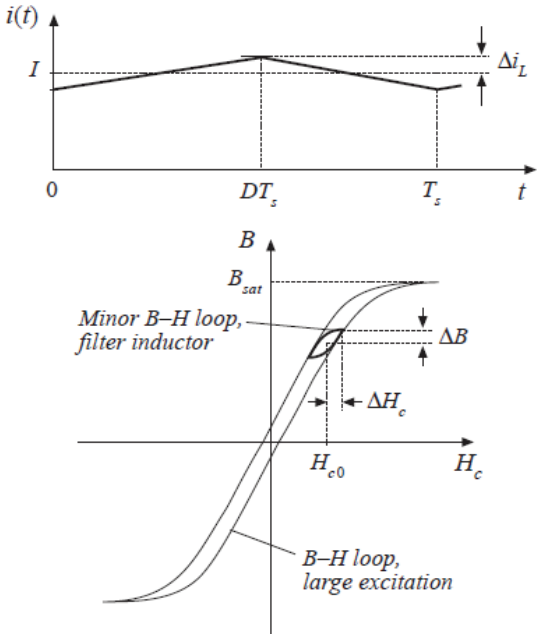
- Governed by Steinmetz Equation:

$$P_v = K_{fe} f_s^{\alpha} (\Delta B)^{\beta} \quad [\text{mW/cm}^3]$$

- Parameters K_{fe}, α, and β extracted from manufacturer data

$$P_{fe} = P_v A_c l_m \ [\text{mW}]$$

- $\Delta B \propto \Delta i_L \rightarrow$ small losses with small ripple



Steinmetz Parameter Extraction

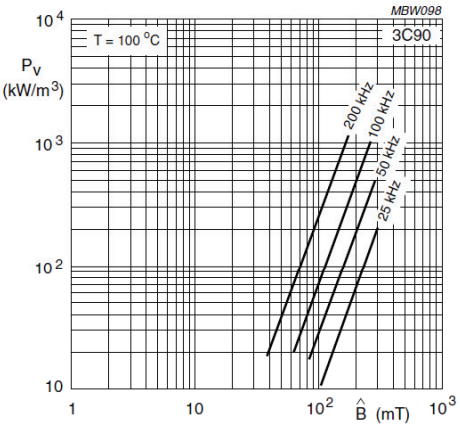


Fig.6 Specific power loss as a function of peak flux density with frequency as a parameter.

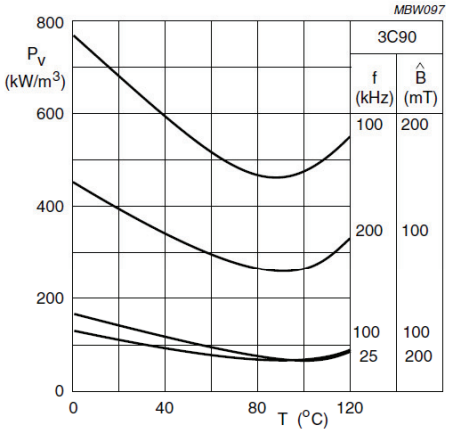


Fig.7 Specific power loss for several frequency/flux density combinations as a function of temperature.

Ferroxcube Curve Fit Parameters

Power losses in our ferrites have been measured as a function of frequency (f in Hz), peak flux density (B in T) and temperature (T in °C). Core loss density can be approximated (2) by the following formula :

$$P_{core} = C_m \cdot f^x \cdot B_{peak}^y (ct_0 - ct_1 T + ct_2 T^2) \quad [3]$$

$$= C_m \cdot C_T \cdot f^x \cdot B_{peak}^y \quad [mW/cm^3]$$

ferrite	f (kHz)	Cm	x	y	ct_2	ct_1	ct_0
3C30	20-100	$7.13.10^{-3}$	1.42	3.02	$3.65.10^{-4}$	$6.65.10^{-2}$	4
	100-200	$7.13.10^{-3}$	1.42	3.02	4.10^{-4}	$6.8 .10^{-2}$	3.8
3C90	20-200	$3.2.10^{-3}$	1.46	2.75	$1.65.10^{-4}$	$3.1.10^{-2}$	2.45
3C94	20-200	$2.37.10^{-3}$	1.46	2.75	$1.65.10^{-4}$	$3.1.10^{-2}$	2.45
	200-400	2.10^{-9}	2.6	2.75	$1.65.10^{-4}$	$3.1.10^{-2}$	2.45
3F3	100-300	$0.25.10^{-3}$	1.63	2.45	$0.79.10^{-4}$	$1.05.10^{-2}$	1.26
	300-500	2.10^{-5}	1.8	2.5	$0.77.10^{-4}$	$1.05.10^{-2}$	1.28
	500-1000	$3.6.10^{-9}$	2.4	2.25	$0.67.10^{-4}$	$0.81.10^{-2}$	1.14
3F4	500-1000	12.10^{-4}	1.75	2.9	$0.95.10^{-4}$	$1.1.10^{-2}$	1.15
	1000-3000	$1.1.10^{-11}$	2.8	2.4	$0.34.10^{-4}$	$0.01.10^{-2}$	0.67

Table 1: Fit parameters to calculate the power loss density

NSE/iGSE

$$P_{NSE} = \left(\frac{\Delta B}{2}\right)^{\beta-\alpha} \frac{k_N}{T} \int_0^T \left|\frac{dB}{dt}\right|^{\alpha} dt$$

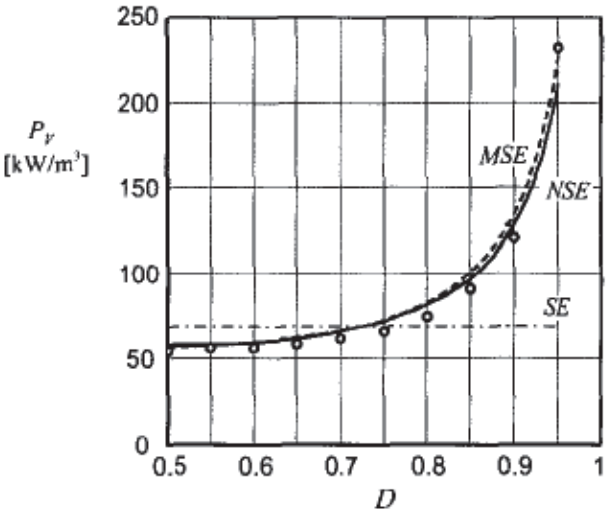
$$k_N = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} d\vartheta}$$

Simple Formula for Square-wave voltages:

$$P_{NSE} = k_N (2f)^{\alpha} (\Delta B)^{\beta} \left(D^{1-\alpha} + (1-D)^{1-\alpha}\right) \quad (10)$$

where f is the operating frequency;
$\Delta B / 2$ is the peak induction;
D is the duty ratio of the square wave voltage.

Note: The second and third harmonics are dominant at moderate values of duty ratio D. For extreme values of D (95%), a higher value of α could give better matching to the actual losses.



Van den Bossche, A.; Valchev, V.C.; Georgiev, G.B.; , "Measurement and loss model of ferrites with non-sinusoidal waveforms,"
K. Venkatachalam; C. R. Sullivan; T. Abdallah; H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters"

INDUCTOR DESIGN

THE UNIVERSITY OF TENNESSEE KNOXVILLE

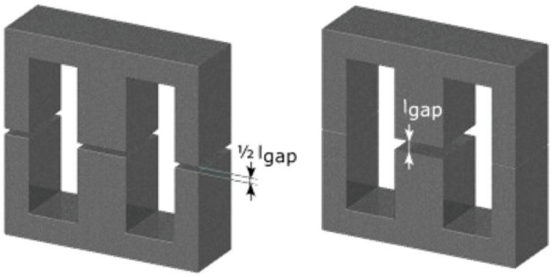
Inductor Design

Freedoms:

1. Core Size and Material
2. Number of turns and wire gauge
3. Length of Air Gap

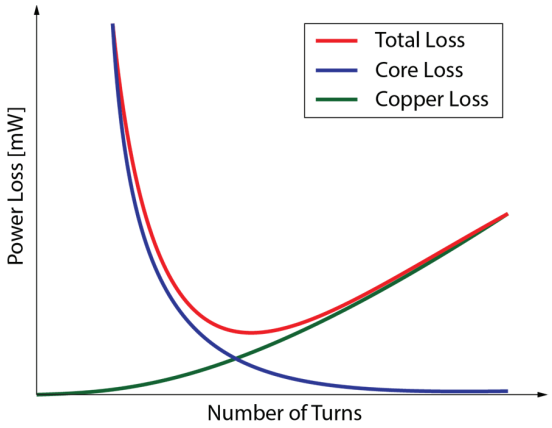
Constraints:

1. Obtain Designed L
2. Prevent Saturation
3. Minimize Losses

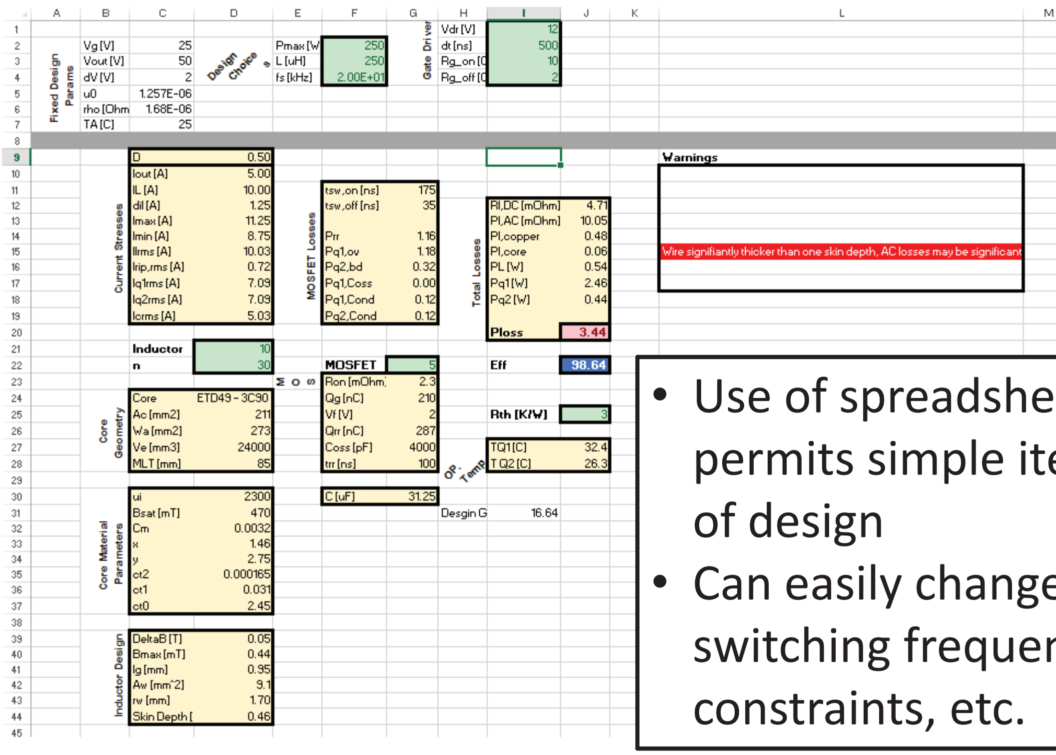


Minimization of Losses

- For given core, number of turns can be used to index possible designs, with air gap solved after (and limited) to get correct inductance
- A minimum sum of the two exists and can be solved
- Design always subject to constraint $B_{max} < B_{sat}$



Spreadsheet Design



- Use of spreadsheet permits simple iteration of design
- Can easily change core, switching frequency, loss constraints, etc.

Matlab (Programmatic) Design

```
function [n, lg, Pq1, Pq2, Pl, eta, Cmin ] = TestBoostDesign(Pmax, fs, L, dt, core_geom, core_mat, MOSFET)
%TestBoostDesign calculate boost conveter efficiency and temperature rise
%for various designs
%    fs  = switching frequency (in Hz)
%    L = inductance (in Henries)
%    n = number of turns on inductor
%    dt = switching dead time (in seconds)
%    core_geom = core geometry, chosen from 'EFD25', 'ETD29', 'ETD39', 'ETD44', or 'ETD49'
%    core_mat = core material, chosen from '3F3', '3C90', or '3F4'
%    MOSFET = MOSFET selection, chosen from 'AOT', 'FDP', 'IPP2', 'IRF',
%    'CSD' or 'IPP0'

Vg = 25;
Vout = 50;
Iout = Pmax/Vout;
Ts = 1/fs;
D = 1-Vg/Vout;
dVout = 2;
Vdr = 12;

Rgon = 10;
Rgoff = 2;

rho = 1.724e-6; %ohms*cm
u0 = 4*pi*1e-7;

%% Inductor Datasheet Parameters
switch core_geom
    case 'EFD25'
        MLT = 46.4; %mm
        Ac = 58; %mm^2
        Ve = 3300; %mm^3
        Wa = 40.2; %mm^2
```

- Matlab, or similar, permits more powerful iteration and plotting/insight into design variation

Closed-Form Design Methods

- **Fundamentals of Power Electronics Ch 13-15**
  - Step-by-Step design methods
  - Simplified, and may require additional calculations

K_g and K_{gfe} Methods

- Two closed-form methods to solve for the optimal inductor design *under certain constraints/assumptions*
- Neither method considers losses other than DC copper and (possibly) steinmetz core loss
- Both methods particularly well suited to spreadsheet/iterative design procedures

	K_g	K_{gfe}
Losses	DC Copper (specified)	DC Copper, SE Core Loss (optimized)
Saturation	Specified	Checked After
B_{max}	Specified	Optimized

K_g Method

- Method useful for filter inductors where ΔB is small
- Core loss is not included, but may be significant particularly if large ripple is present
- Copper loss is specified through a set target resistance
- The desired B_{max} is given as a constraint
- Method does not check feasibility of design; must ensure that air gap is not extremely large or wire size excessively small
- Simple first-cut design technique; useful for determining approximate core size required
- Step-by-step design procedure included on website

The following quantities are specified, using the units

Wire resistivity	ρ	(Ω-cm)
Peak winding current	I_{max}	(A)
Inductance	L	(H)
Winding resistance	R	(Ω)
Winding fill factor	K_u	
Core maximum flux density	B_{max}	(T)

The core dimensions are expressed in cm:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)

$$K_g \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u} 10^8 \quad (\text{cm}^5)$$

$$\ell_g = \frac{\mu_0 L I_{max}^2}{B_{max}^2 A_c} 10^4 \quad (\text{m})$$

$$n = \frac{L I_{max}}{B_{max} A_c} 10^4$$

$$A_W \leq \frac{K_u W_A}{n} \quad (\text{cm}^2)$$

$$R = \frac{\rho n (MLT)}{A_w} \quad (\Omega)$$

K_{gfe} Method

- Method useful for cases when core loss and copper loss are expected to be significant
- Saturation is not included in the method, rather it must be checked afterward
- Enforces a design where the sum of core and copper is minimized

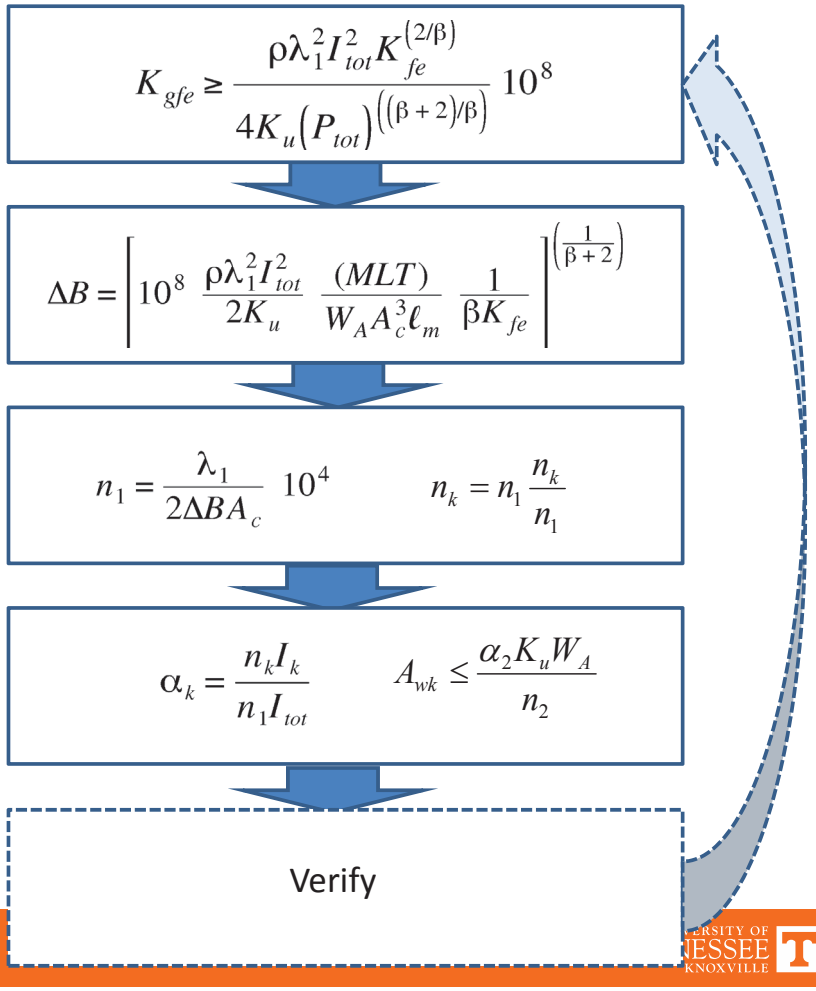
K_{gfe} Procedure

The following quantities are specified, using the units noted:

Wire effective resistivity	ρ	(Ω-cm)
Total rms winding current, ref to pri	I_{tot}	(A)
Desired turns ratios	n_2/n_1, n_3/n_1, etc.	
Applied pri volt-sec	λ_1	(V-sec)
Allowed total power dissipation	P_{tot}	(W)
Winding fill factor	K_u	
Core loss exponent	β	
Core loss coefficient	K_{fe}	(W/cm^3T^β)

Other quantities and their dimensions:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)
Magnetic path length	ℓ_e	(cm)
Wire areas	A_{w1}, …	(cm^2)
Peak ac flux density	ΔB	(T)



K_{gfe} Method: Summary

- Method enforces an operating ΔB in which core and copper losses are minimized
- Only takes into account losses from standard Steinmetz equation; not correct unless waveforms are sinusoidal
- Does not consider high frequency losses
- Step-by-step design procedure included on website