

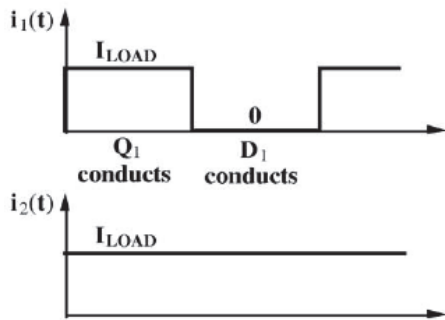
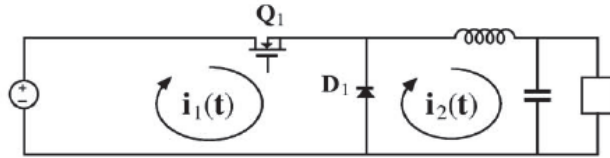
# Outline

1. Power Converter Layout
2. Loss Analysis and Design
  - Low Frequency Conduction Losses
  - Inductor AC Losses
  - Core Losses
  - Inductor Design Approaches

## POWER CONVERTER LAYOUT

# Power Converter Layout: Buck Example

Use loop analysis



switched input current  $i_1(t)$  contains large high frequency harmonics

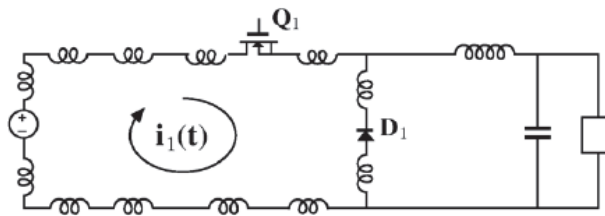
—hence inductance of input loop is critical  
inductance causes ringing, voltage spikes, switching loss, generation of B- and E-fields, radiated EMI

the second loop contains a filter inductor, and hence its current  $i_2(t)$  is nearly dc

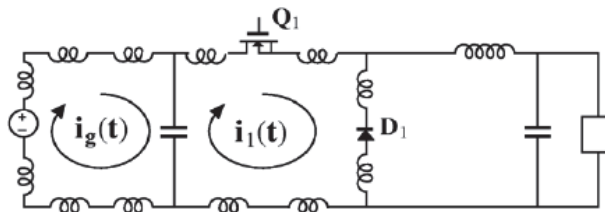
—hence additional inductance is not a significant problem in the second loop

## Parasitic Wire Inductances

Parasitic inductances of input loop explicitly shown:



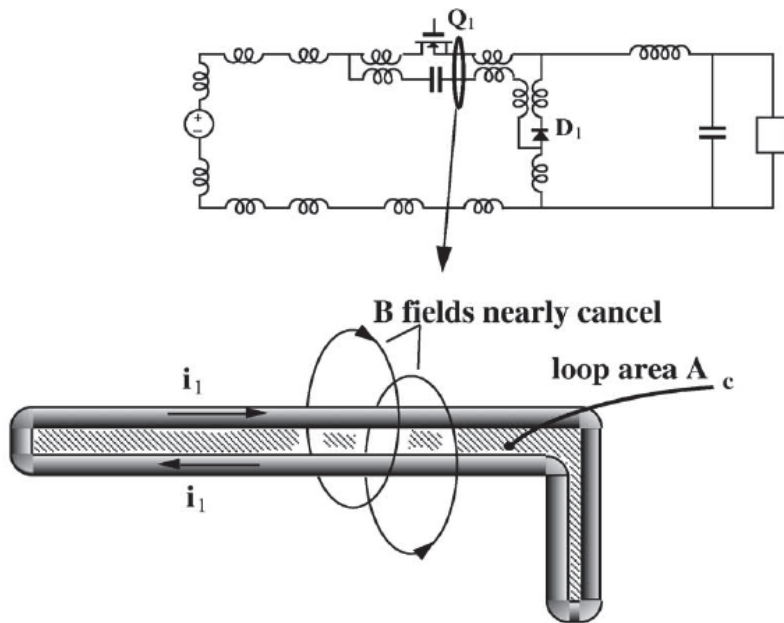
Addition of bypass capacitor confines the pulsating current to a smaller loop:



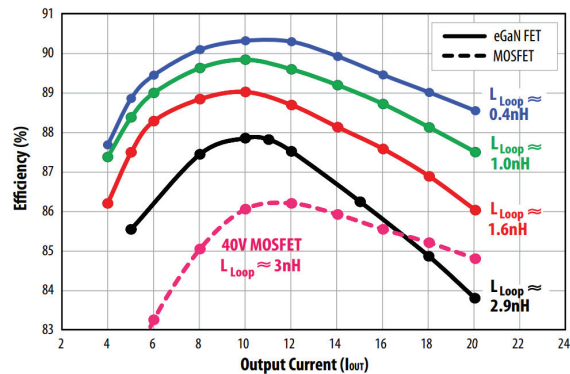
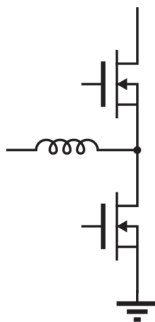
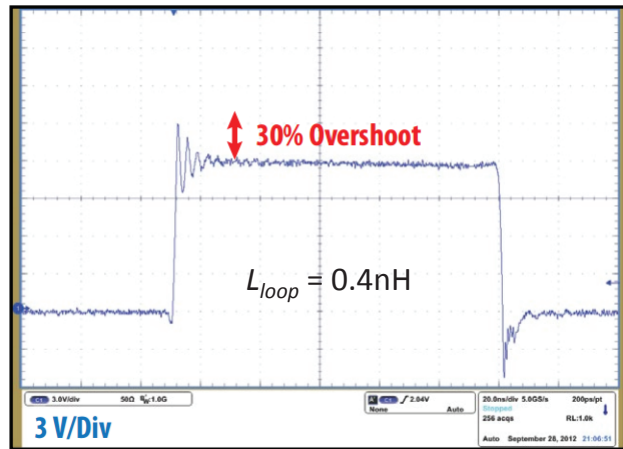
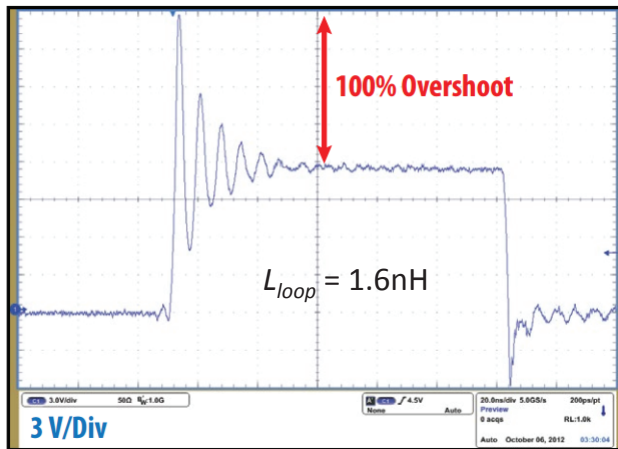
high frequency currents are shunted through capacitor instead of input source

# Loop Minimization

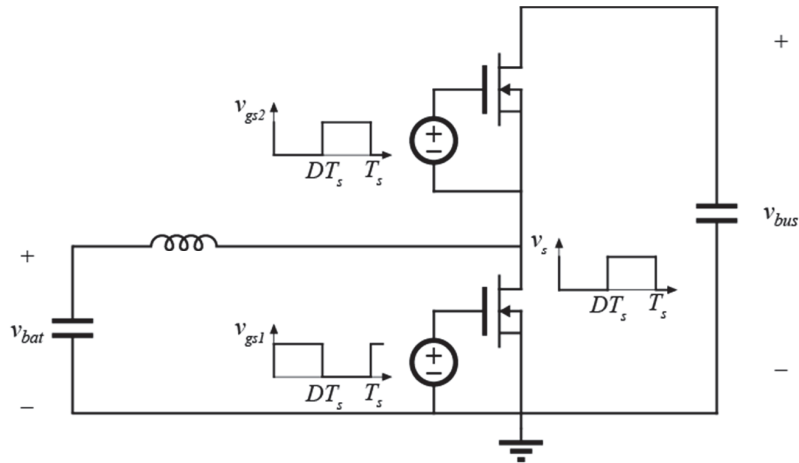
Even better: minimize area of the high frequency loop, thereby minimizing its inductance



## Effect of Loop Inductance

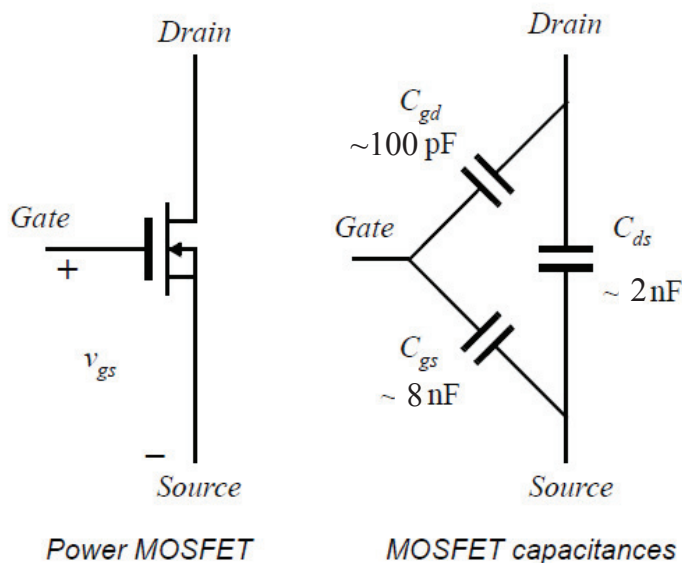


# Half Bridge Gate Drive Waveforms



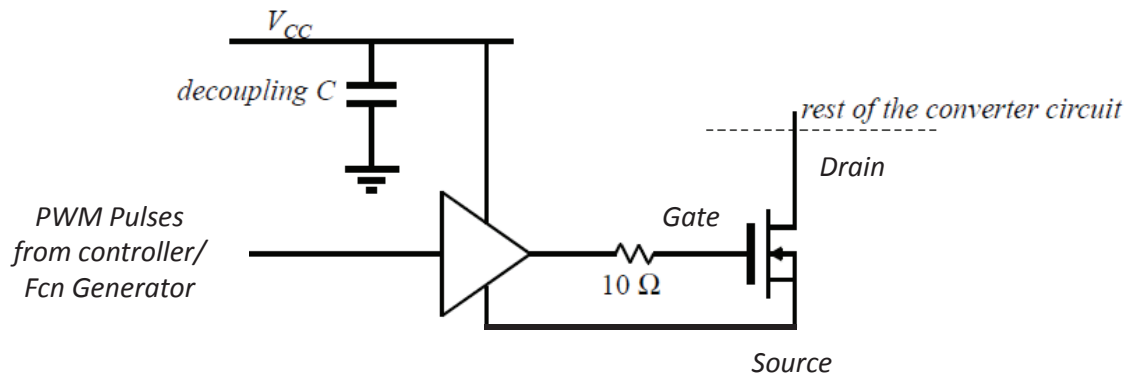
- Gate driver chip must implement  $v_{gs}$  waveforms
- Sources will have pulsating currents and need decoupling

## Driving a Power MOSFET Switch



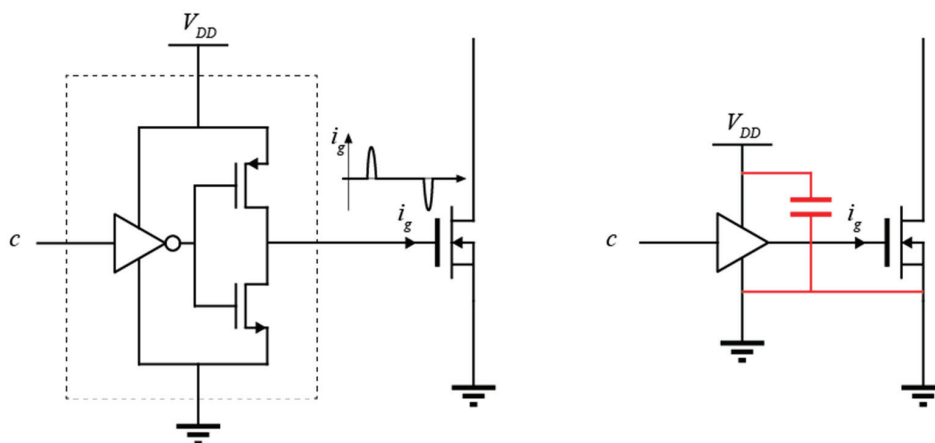
- MOSFET is off when  $v_{gs} < V_{th} \approx 3 \text{ V}$
- MOSFET fully on when  $v_{gs}$  is sufficiently large (10-15 V)
- Warning: MOSFET gate oxide breaks down and the device fails when  $v_{gs} > 20 \text{ V}$ .
- Fast turn on or turn off (10's of ns) requires a large spike (1-2 A) of gate current to charge or discharge the gate capacitance
- MOSFET gate driver is a logic buffer that has high output current capability

# Driving a Power MOSFET Switch



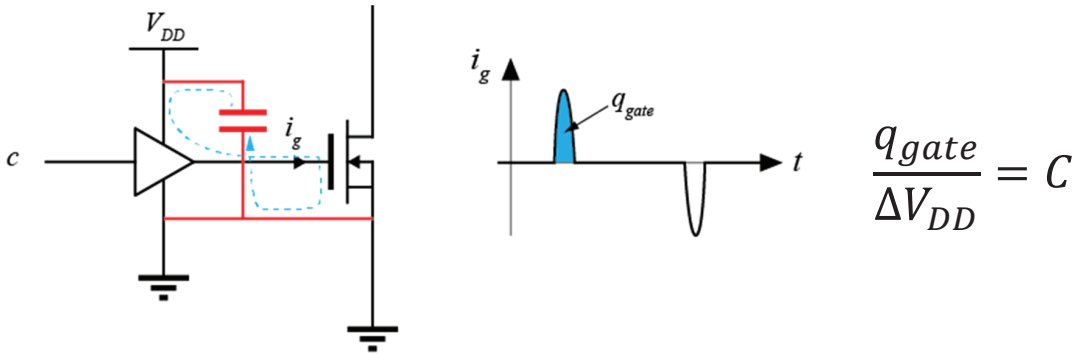
- MOSFET gate driver is used as a logic buffer with high output current ( $\sim 1.8$  A) capability
- The amplitude of the gate voltage equals the supply voltage  $V_{CC}$
- Decoupling capacitors are necessary at all supply pins of LM5104 (and all ICs)
- Gate resistance used to slow  $dv/dt$  at switch node

## Gate Drive Implementation



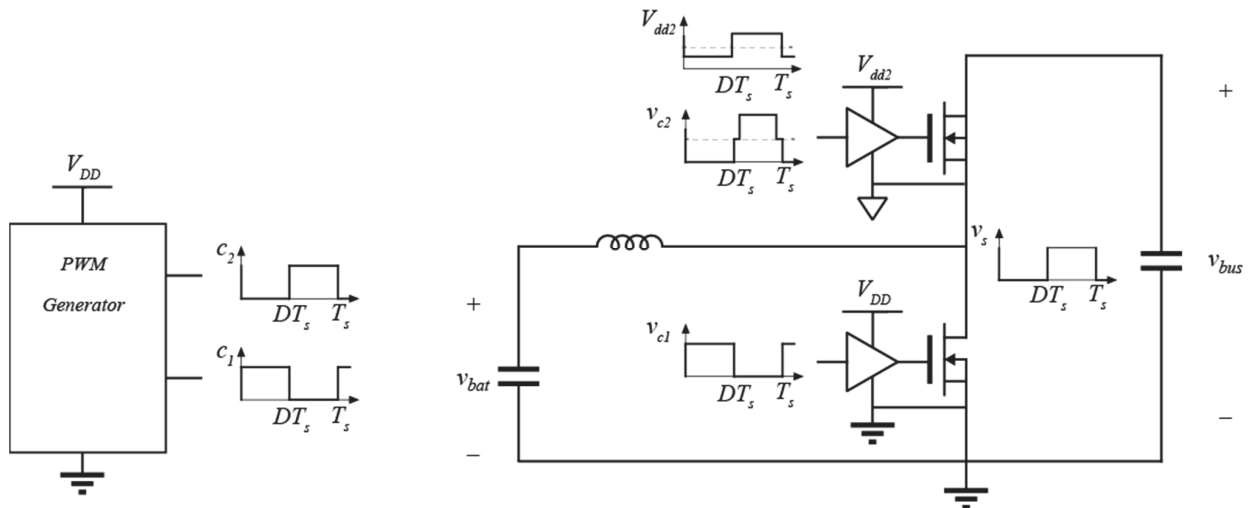
- Gate driver is cascaded half-bridges of increasing size to obtain quick rise times
- Reminder: keep loops which handle pulsating current small by decoupling and making close connections

# Capacitor Sizing – Pulsed Caps



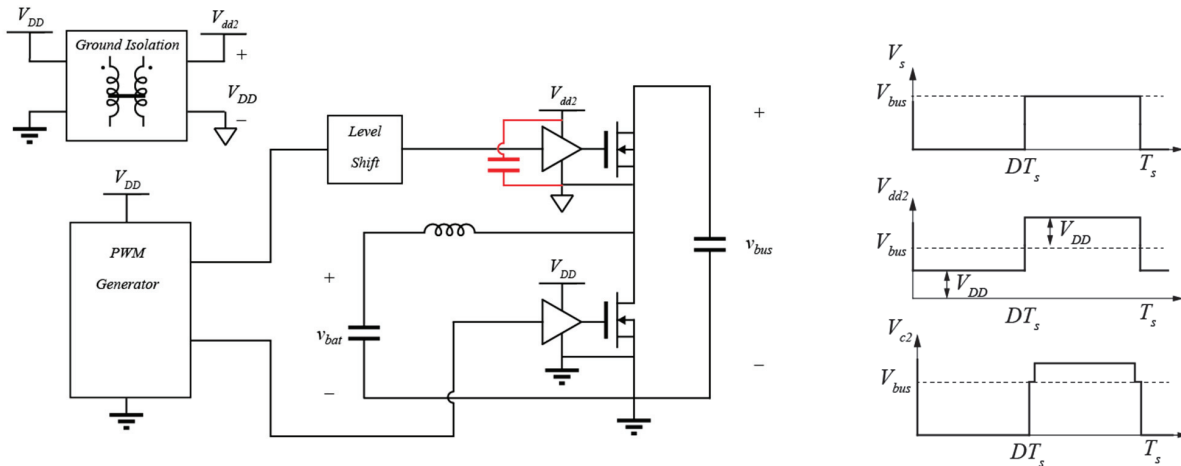
- Area of current pulse is total charge supplied to gate of capacitor
- All charge must be supplied from gate drive decoupling capacitor

# High Side Signal Ground



- Gate driver chip must implement  $v_{gs}$  waveforms
- Issue: source of  $Q_2$  is not grounded

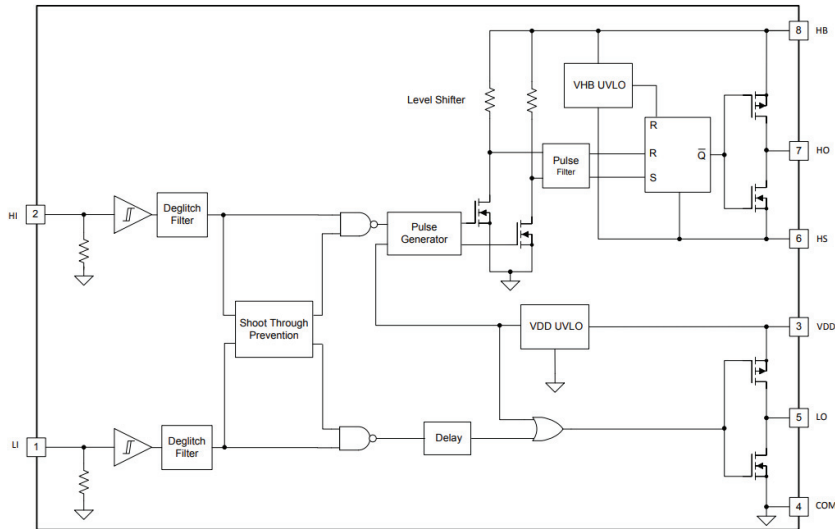
# Generating Floating Supply



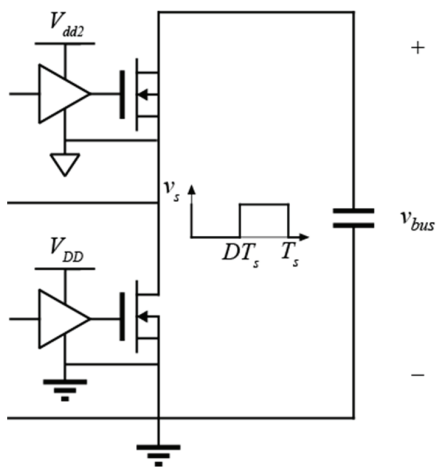
- Isolated supplies sometimes used; Isolated DC-DC, batteries
- Bootstrap concept: capacitor can be charged when  $V_s$  is low, then switched

Direct Drive		<p>Easiest high-side application the MOSFET and can be driven directly by the PWM controller or by a ground referenced driver, but it must meet two conditions, as follows:</p> $V_{CC} < V_{GS,MAX} \quad \text{and} \quad V_{DC} < V_{CC} - V_{GS,Miller}$
Floating Supply Gate Drive		<p>Cost impact of isolated supply is significant. Optocoupler tends to be relatively expensive, limited in bandwidth, and noise sensitive.</p>
Transformer Coupled Drive		<p>Gives full gate control for an indefinite period of time, but is somewhat limited in switching performance. This can be improved with added complexity.</p>
Charge Pump Drive		<p>The turn-on times tend to be long for switching applications. Inefficiencies in the voltage multiplication circuit may require more than low stages of pumping.</p>
Bootstrap Drive		<p>Simple and inexpensive with limitations; such as, the duty cycle and on-time are both constrained by the need to refresh the bootstrap capacitor. Requires level shift, with the associated difficulties.</p>

# UCC27712 Internal Diagram

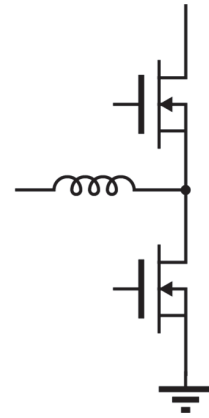
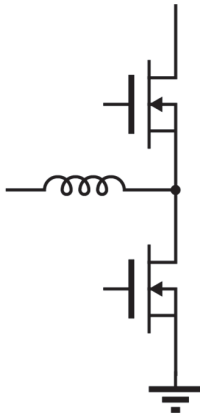
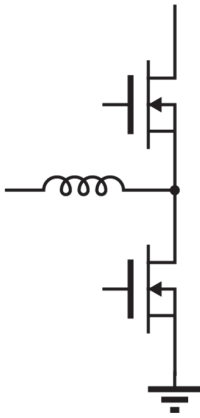


## A Note on Grounding

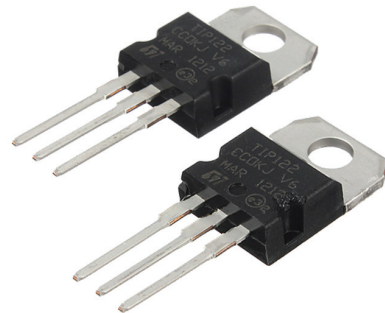
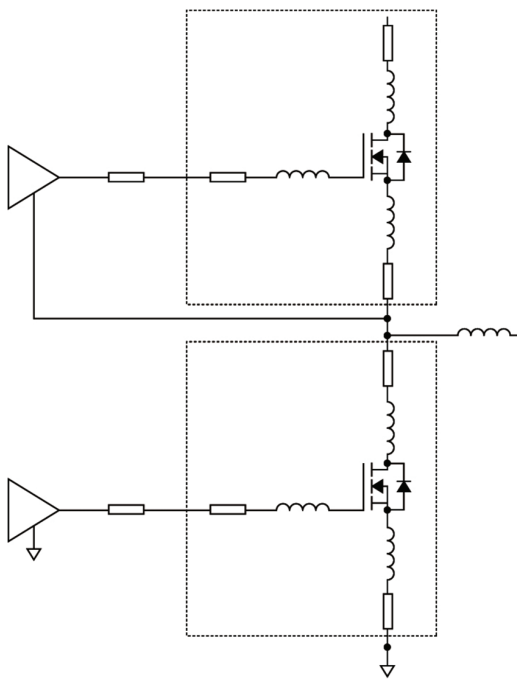




# Parasitics to be Aware of



# Power Loop Inductances



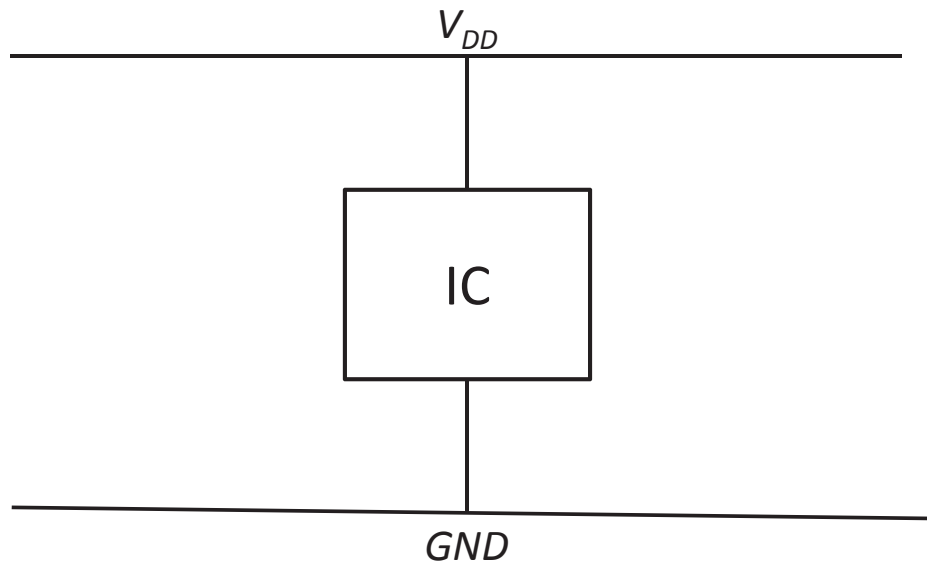
# Complete Routing of Signal

- Always consider return path
- Ground plane can help, but still need to consider the path and optimize

## Decoupling

- Always add bypass capacitor at power supply for any IC/reference
- Use small-valued ( $\sim 100\text{nf}$ ), low ESR and ESL capacitors (ceramic)
- Limit loop for any  $di/dt$

# Decoupling



## Star-Grounding Vs. Daisy Chain

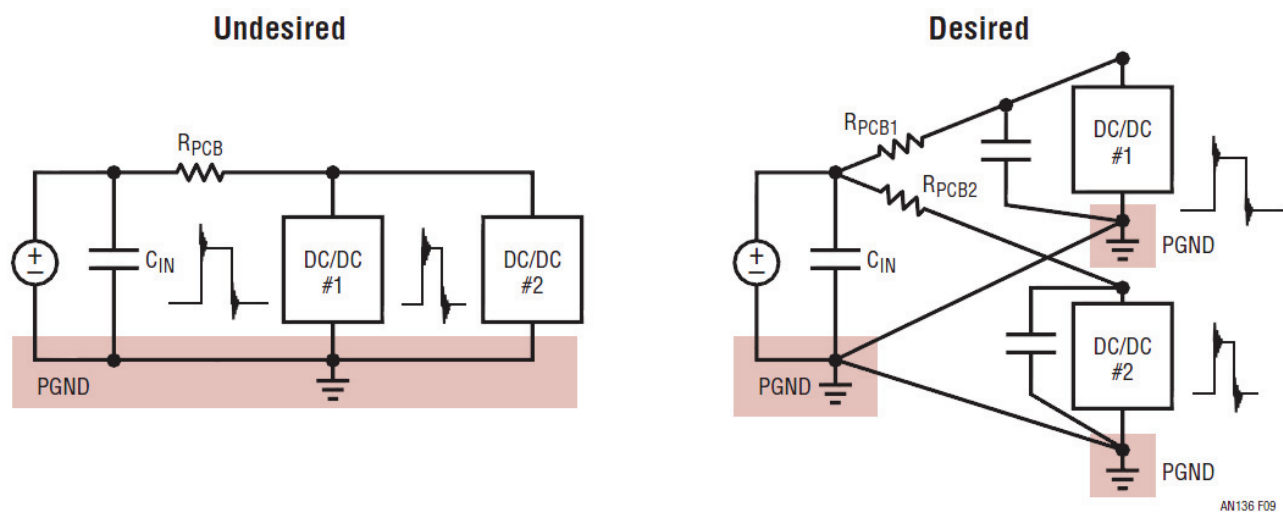
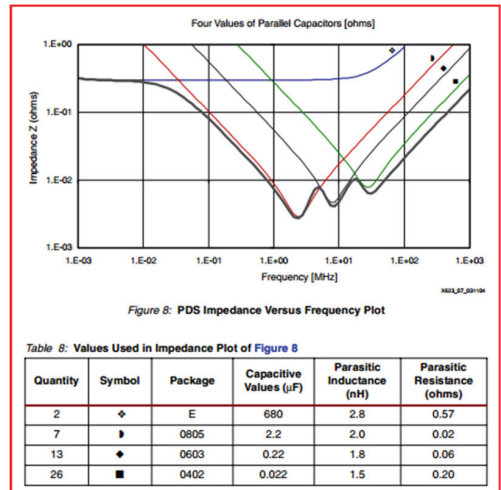
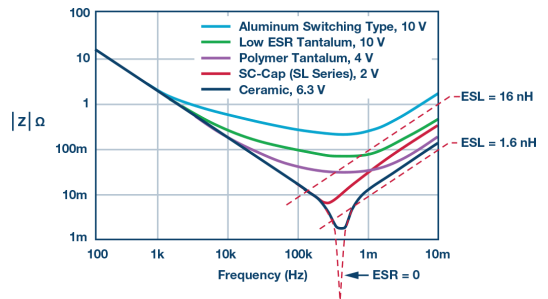


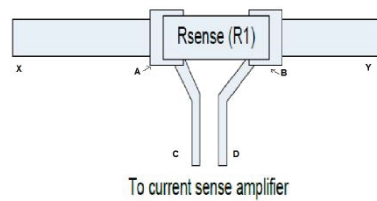
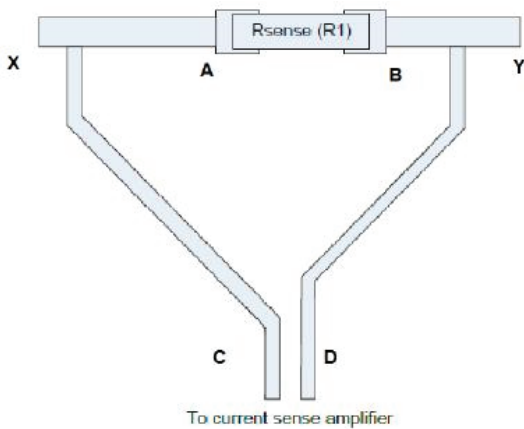
Figure 9. Separate the Input Current Paths Among Supplies

# Capacitor Sizing – Filter Caps

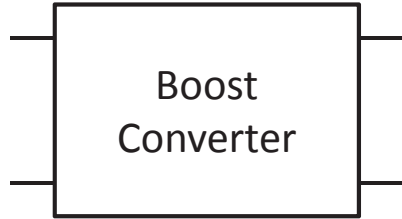


<https://www.intersil.com/content/dam/Intersil/documents/an13/an1325.pdf>

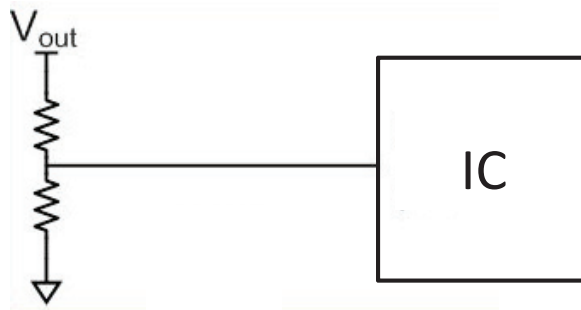
# Kelvin Connection



# Efficiency Measurement

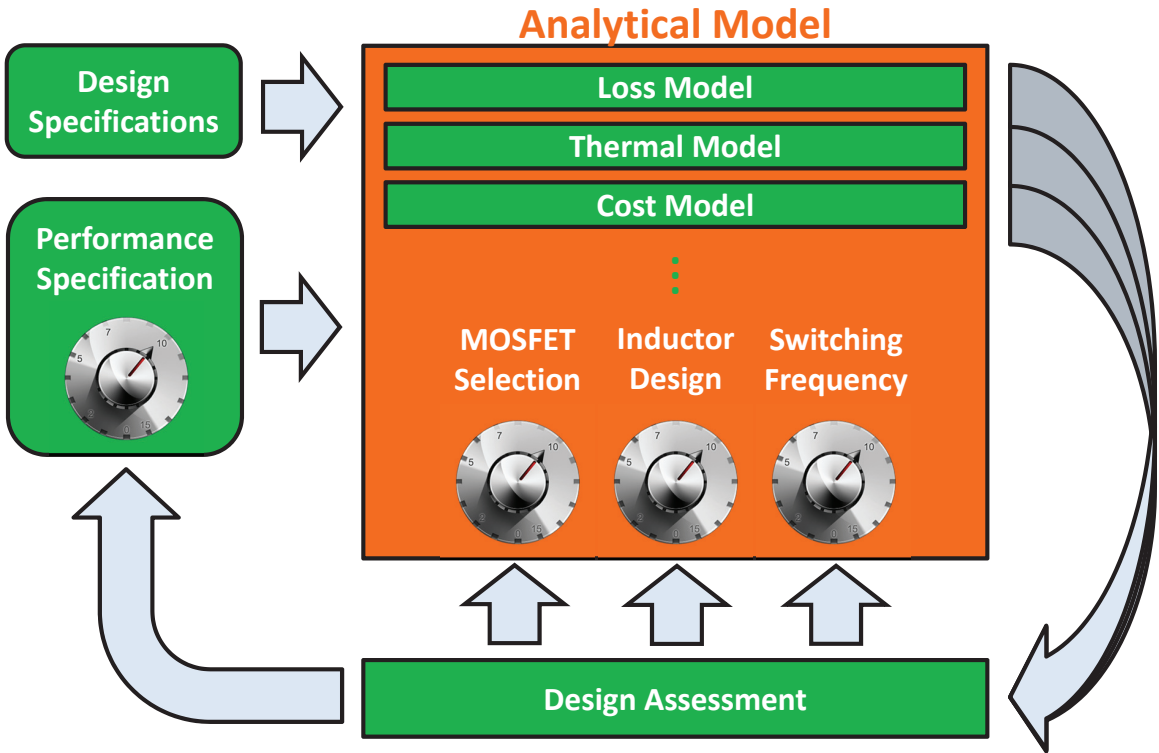


# High Impedance Nodes



# POWER CONVERTER DESIGN AND LOSS ANALYSIS

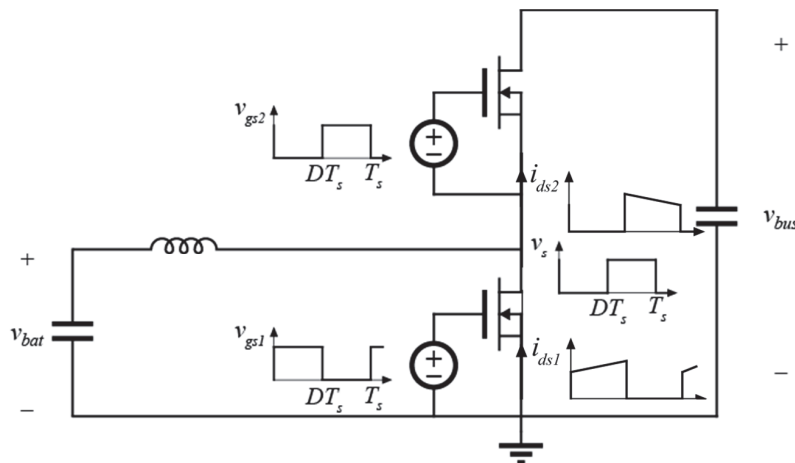
## Converter Design



# Analytical Loss Modeling

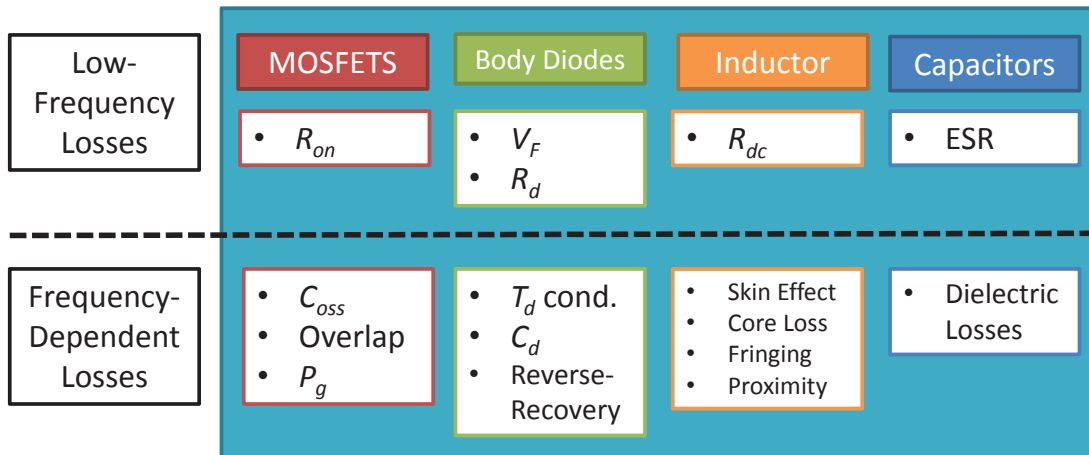
- High efficiency approximation is acceptable for hand calculations, as long as it is justified
  - Solve ideal waveforms of lossless converter, then calculate losses
- Argue which losses need to be included, and which may be neglected
  - “Rough” approximation to gain insight into significance

## Boost Converter Loss Analysis



- Begin by solving important waveforms throughout converter assuming lossless operation

# Power Stage Losses



## Supplemental Lectures

Device	Loss Mechanism	ECE 481	ECE 581
MOSFET	$R_{on}$	Lecture 7-8	
	$C_{oss}$		Lecture 7
	Overlap		Lecture 5-6
	$P_g$		Lecture 5
Diode	$V_F$	Lecture 7-8	
	$R_d$	Lecture 7-8	
	$t_d$ cond		Lecture 5
	$C_d$		Lecture 7 (see: $C_{oss}$ )
	Reverse-Recovery	Lecture 11	
Inductor	$R_{dc}$	Lecture 38	
	Skin Effect	Lecture 39	
	Core Loss	Lecture 39	
	Fringing		
	Proximity	Lecture 39	

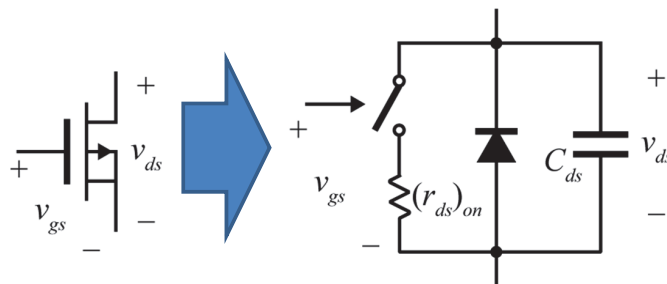
ECE581: <http://web.eecs.utk.edu/~dcostine/ECE581/Fall2018/schedule.php>

ECE481: <http://web.eecs.utk.edu/~dcostine/ECE481/Fall2017/schedule.php>



## LOW FREQUENCY CONDUCTION LOSSES

### MOSFET Equivalent Circuit



- Considering only power stage losses (gate drive neglected)
- MOSFET operated as power switch
- Intrinsic body diode behaviors considered using normal diode analysis

# Datasheet Interpretation

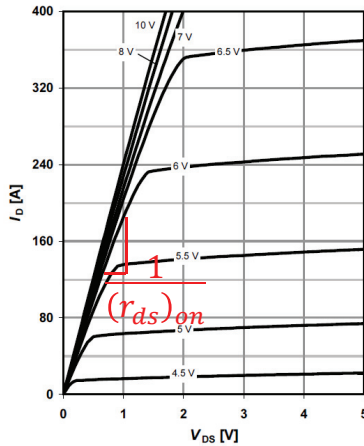
Drain-source on-state resistance

$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=50\text{ A}$	-	16	20	$m\Omega$
	$V_{GS}=8\text{ V}, I_D=25\text{ A}$	-	16	20	

5 Typ. output characteristics

$I_D=f(V_{DS}); T_J=25\text{ }^\circ\text{C}$

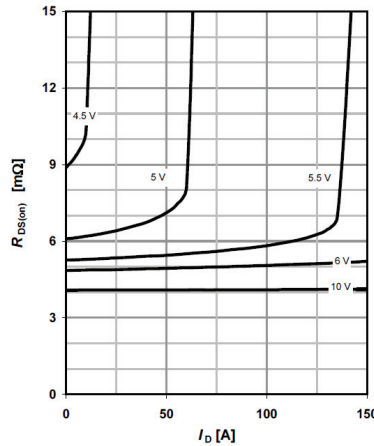
parameter:  $V_{GS}$



6 Typ. drain-source on resistance

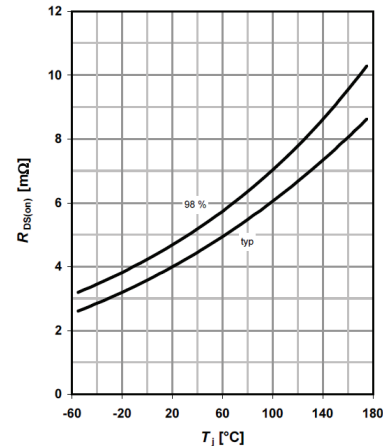
$R_{DS(on)}=f(I_D); T_J=25\text{ }^\circ\text{C}$

parameter:  $V_{GS}$



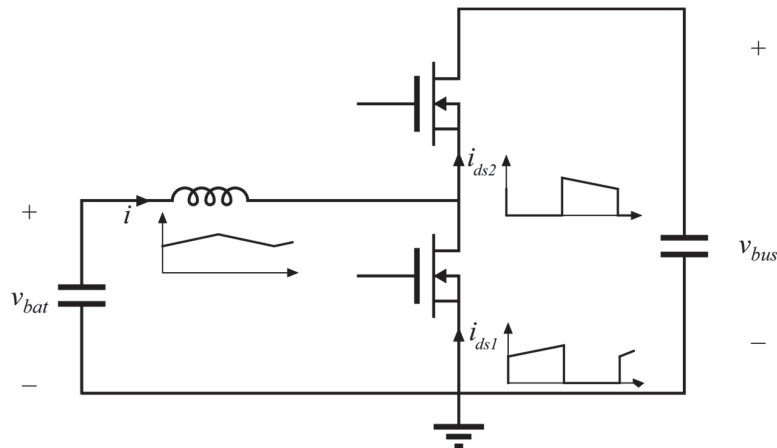
9 Drain-source on-state resistance

$R_{DS(on)}=f(T_J); I_D=100\text{ A}; V_{GS}=10\text{ V}$



- On resistance extracted from datasheet waveforms
- Significantly dependent on  $V_{GS}$  amplitude, temperature

## Boost Converter RMS Currents



- MOSFET conduction losses due to  $(r_{ds})_{on}$  depend given as

$$P_{cond,FET} = I_{di,rms}^2 (r_{ds})_{on}$$

# MOSFET Conduction Losses

Pulsating waveform with linear ripple, Fig. A.6:

$$rms = I\sqrt{D} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i}{I}\right)^2} \quad (A.6)$$

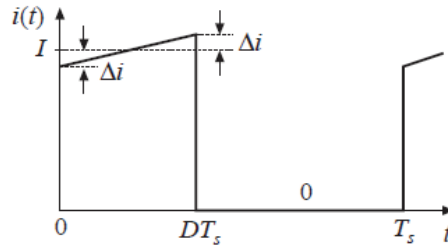
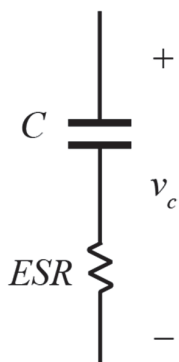


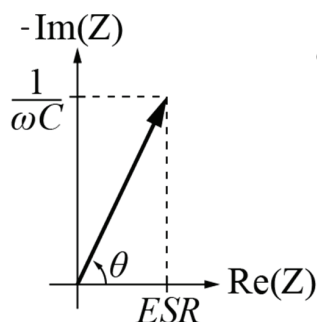
Fig. A.6

- RMS values of commonly observed waveforms appendix from Power Book

## Capacitor Loss Model



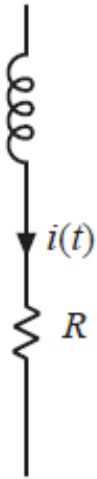
- Operation well below resonance
- All loss mechanisms in a capacitor are generally lumped into an empirical loss model
- Equivalent Series Resistance (ESR) is *highly* frequency dependent
- Datasheets may give effective impedance at a frequency, or loss factor:



$$\delta = \frac{\pi}{2} - \theta$$

$$D = \tan(\delta)$$

# DC Inductor Resistance



- DC Resistance given by

$$R_{DC} = \rho \frac{l_b}{A_w}$$

- At room temp,  $\rho = 1.724 \cdot 10^{-6} \Omega\text{-cm}$
- At  $100^\circ\text{C}$ ,  $\rho = 2.3 \cdot 10^{-6} \Omega\text{-cm}$
- Losses due to DC current:

$$P_{cu,DC} = I_{L,rms}^2 R_{DC}$$

## Inductor Conduction Losses

DC plus linear ripple, Fig. A.2:

$$rms = I \sqrt{1 + \frac{1}{3} \left( \frac{\Delta i}{I} \right)^2} \quad (\text{A.2})$$

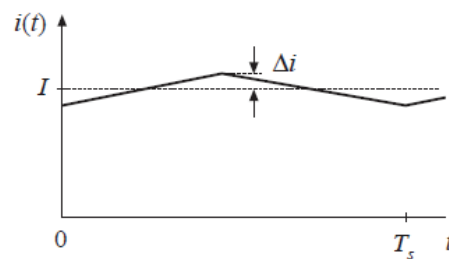
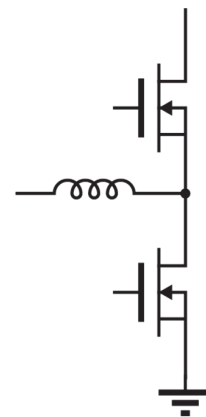
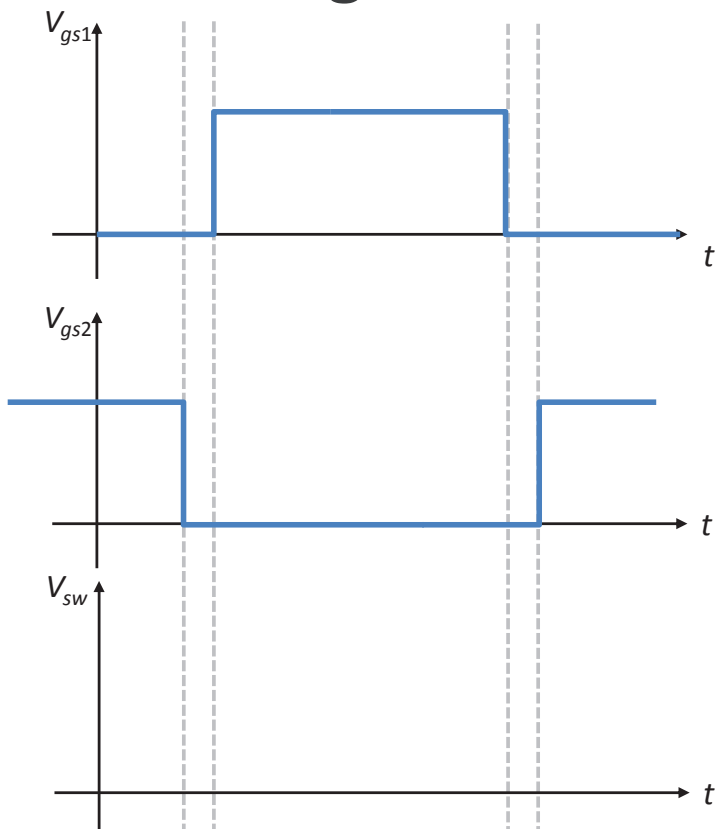


Fig. A.2

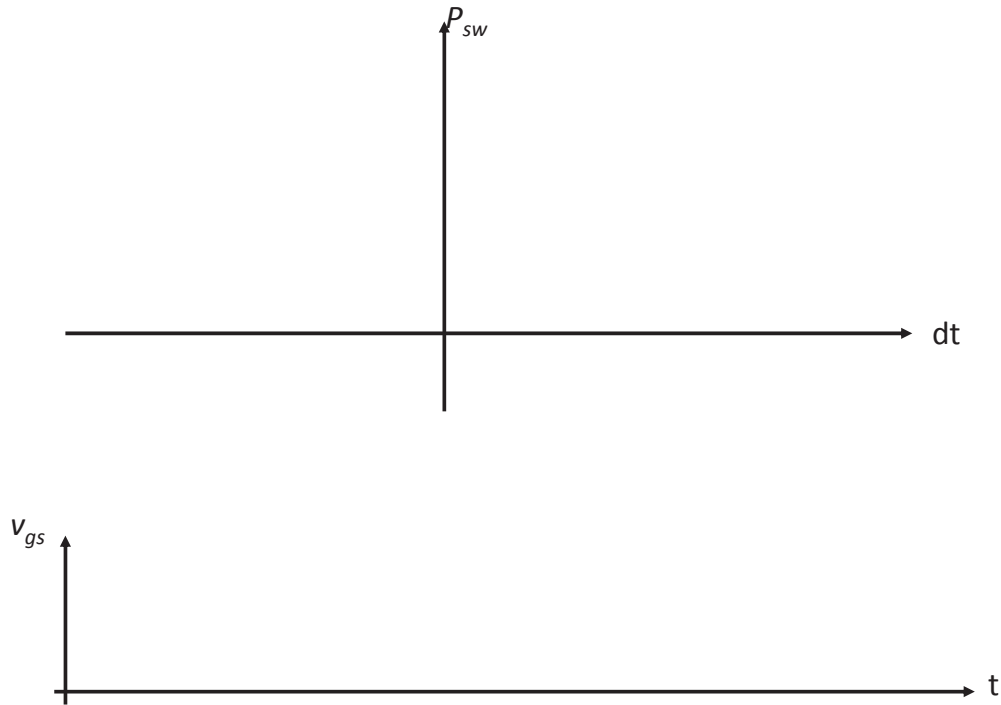
- Conduction losses dependent on RMS current through inductor

# Switching Loss

## Switching Loss Modeling



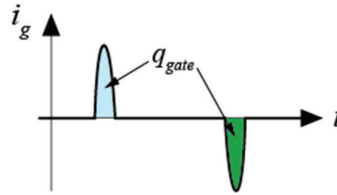
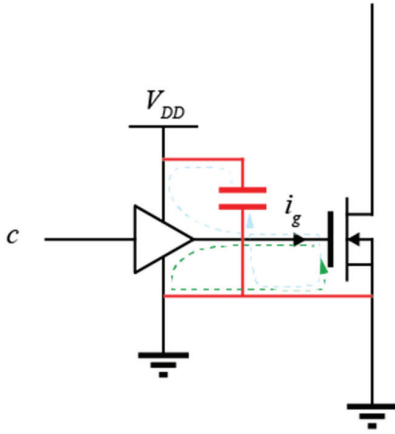
# Dead Time Selection



## Types of Switching Loss

1. Gate Charge Loss
2. Overlap Loss
3. Capacitive Loss
4. Body Diode Conduction
5. Reverse Recovery
6. Parasitic Inductive Losses
7. Anomalous Losses

# Gate Drive Losses



$$E_{loss} = q_{gate} V_{DD}$$

$$P_{sw,g} = E_{loss} f_s$$

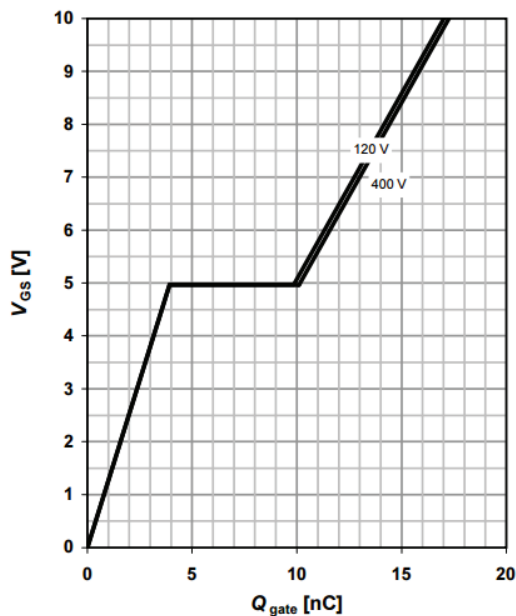
- Gate charge is supplied through driver resistance during switch turn-on
- Gate charge is dissipated in gate driver on switch turn-off

# Gate Charge Loss

## 9 Typ. gate charge

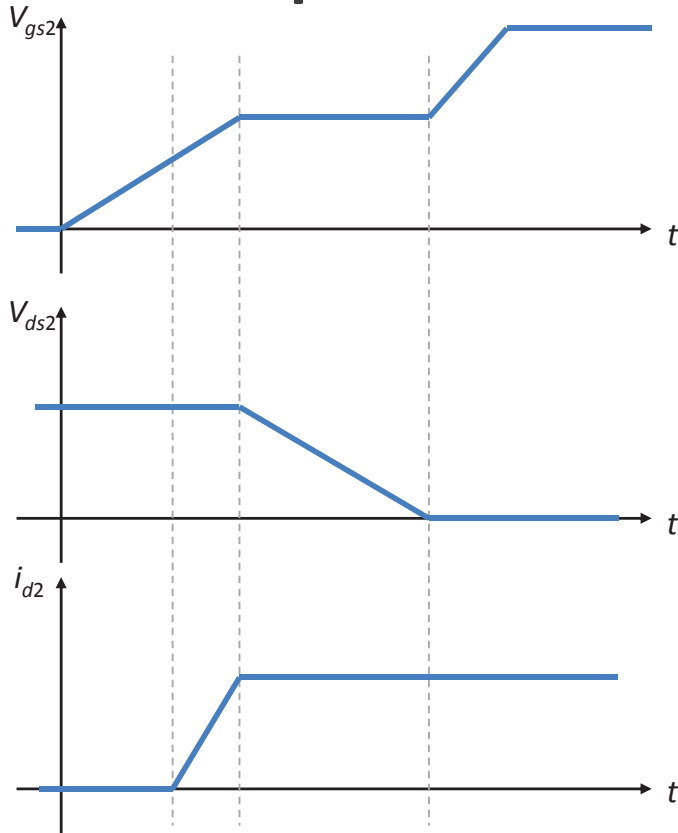
$V_{GS} = f(Q_{gate}); I_D = 5.2 \text{ A pulsed}$

parameter:  $V_{DD}$



$$P_g = Q_g V_{cc} f_s$$

# Overlap Loss

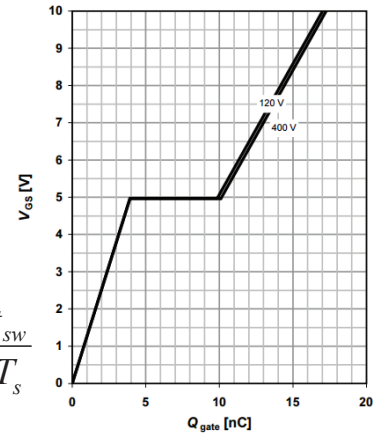


$$P_{overlap} = \frac{1}{2} I_L V \frac{t_{sw}}{T_s}$$

9 Typ. gate charge

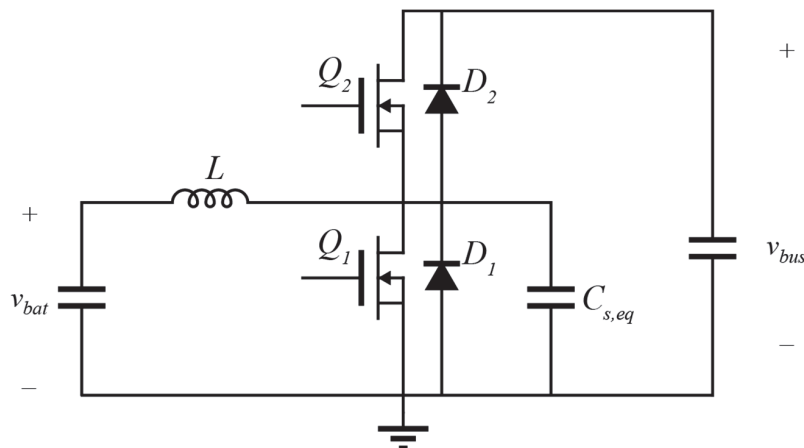
$V_{GS} = f(Q_{gate}); I_D = 5.2 \text{ A pulsed}$

parameter:  $V_{DD}$



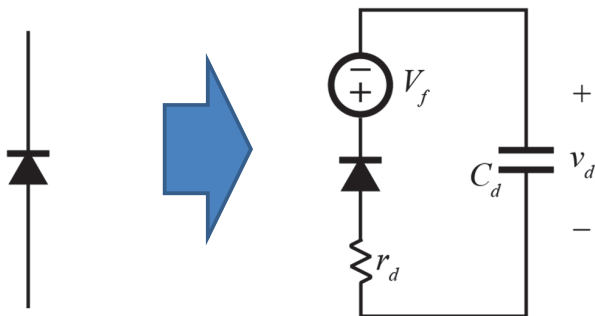
# Lump Switched Node Capacitance

- Consider a single equivalent capacitor at switched node which combines energy storage due to all four semiconductor devices





# Diode Loss Model



- Example loss model includes resistance and forward voltage drop extracted from datasheet

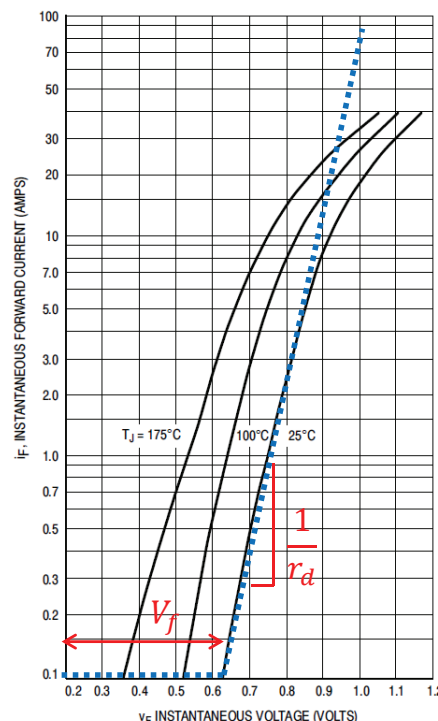
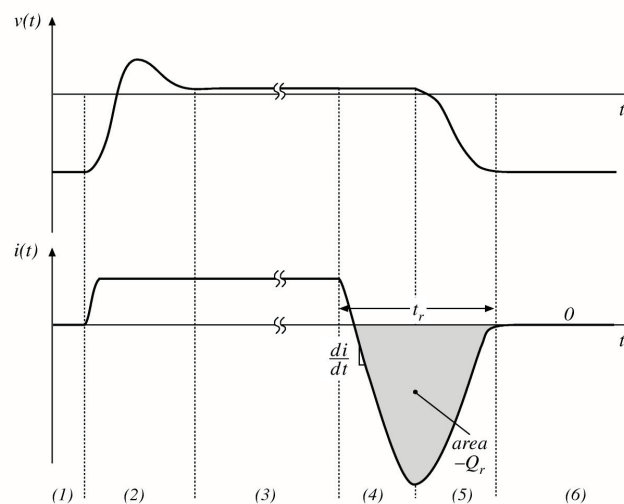


Figure 1. Typical Forward Voltage

# Diode Reverse Recovery

- FET body diodes may turn on during dead time intervals
- Significant reverse recovery losses possible



$$E_{on,rr} = ((I_L - \Delta i_L)t_{rr} + Q_r)V_{bus}$$

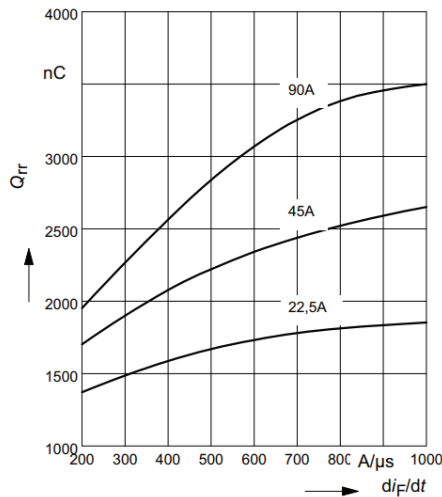
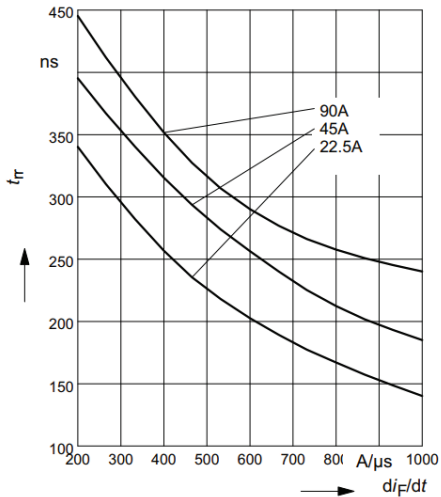
# Reverse Recovery - Datasheet

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Dynamic Characteristics</b>					
Reverse recovery time $V_R=400V, I_F=45A, di_F/dt=1000A/\mu s, T_j=25^\circ C$ $V_R=400V, I_F=45A, di_F/dt=1000A/\mu s, T_j=125^\circ C$ $V_R=400V, I_F=45A, di_F/dt=1000A/\mu s, T_j=150^\circ C$	$t_{rr}$	-	140	-	ns
Reverse recovery charge $V_R=400V, I_F=45A, di_F/dt=1000A/\mu s, T_j=25^\circ C$ $V_R=400V, I_F=45A, di_F/dt=1000A/\mu s, T_j=125^\circ C$ $V_R=400V, I_F=45A, di_F/dt=1000A/\mu s, T_j=150^\circ C$	$Q_{rr}$	-	1400	-	nC

## 5 Typ. reverse recovery time

$$t_{rr} = f(di_F/dt)$$

parameter:  $V_R = 400V, T_j = 125^\circ$

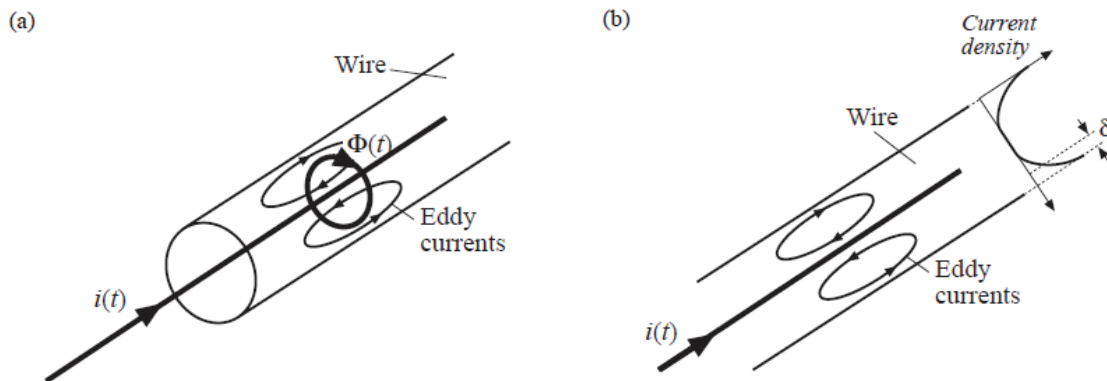


## Reverse Recovery – Rough Approximations

- $E_{rr} \approx E_{rr\_datasheet} \frac{I_F}{I_{F\_datasheet}} \frac{V_{DC}}{V_{DC\_datasheet}}$
- **Rough approximation with  $I_F \ll I_{max}$**

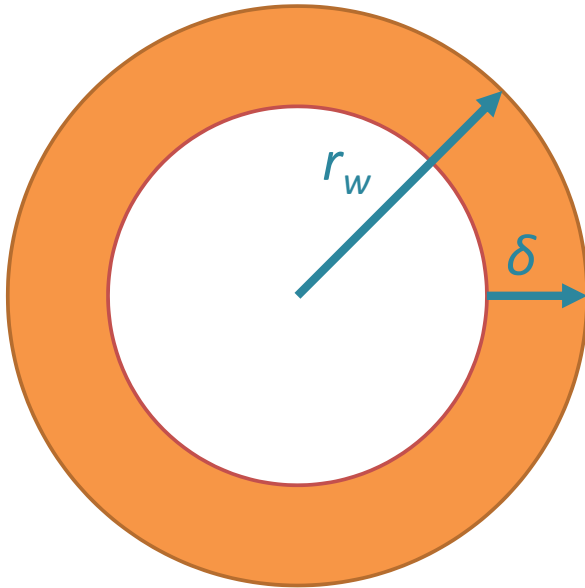
## INDUCTOR AC LOSSES

### Skin Effect in Copper Wire



- Current profile at high frequency is exponential function of distance from center with characteristic length  $\delta$

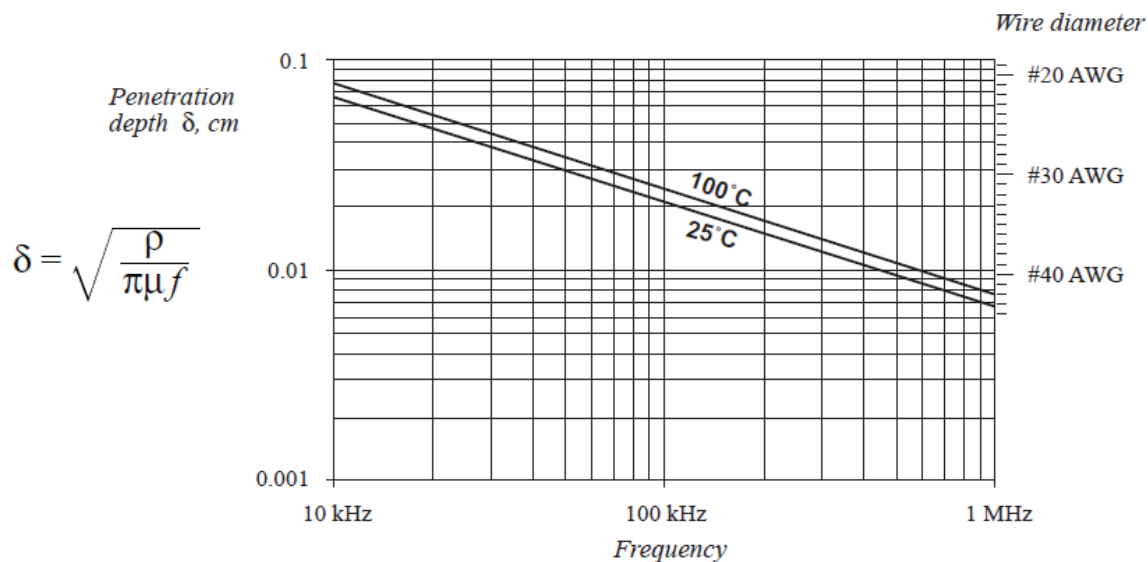
# AC Resistance



$$A_{w,eff} = \pi r_w^2 - \pi (r_w - \delta)^2$$

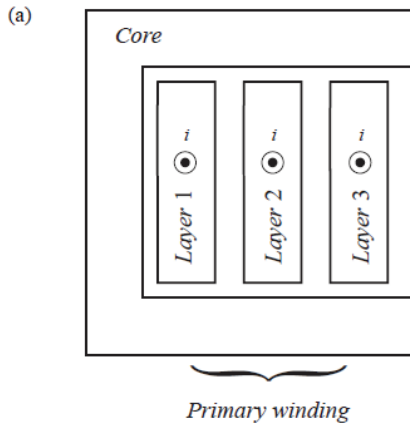
$$R_{ac} = \rho \frac{l_b}{A_{w,eff}}$$

# Skin Depth



$$\delta = \sqrt{\frac{\rho}{\pi \mu f}}$$

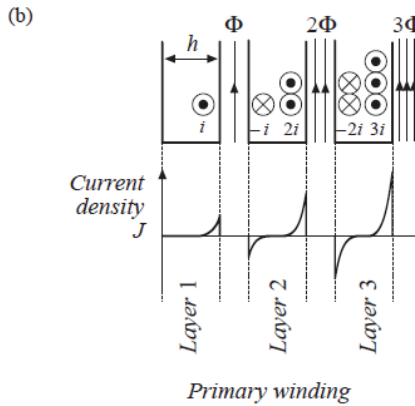
Fig. 13.23 Penetration depth  $\delta$ , as a function of frequency  $f$ , for copper wire.



## Proximity Effect

- In *foil* conductor closely spaced with  $h \gg \delta$ , flux between layers generates additional current according to Lenz's law.

$$P_1 = I_{L,rms}^2 R_{ac}$$



- Power loss in layer 2:

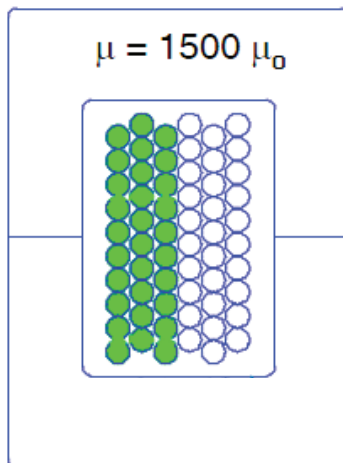
$$P_2 = I_{L,rms}^2 R_{ac} + (2I_{L,rms})^2 R_{ac}$$

$$P_2 = 5P_1$$

- Needs modification for non-foil conductors

See *Fundamentals of Power Electronics*, Section 13.4

## Simulation Example



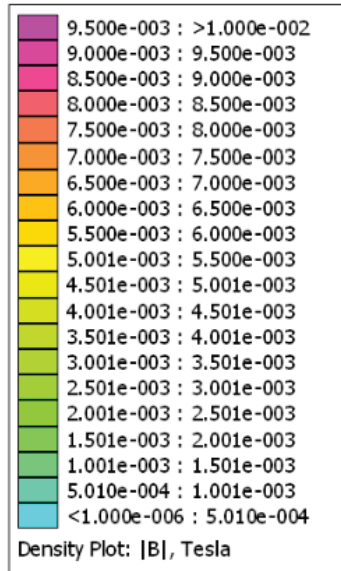
- AWG#30 copper wire
  - Diameter  $d = 0.294$  mm
  - $d = \delta$  at around 50 kHz
- 1:1 transformer
  - Primary and secondary are the same, 30 turns in 3 layers

- Sinusoidal currents,

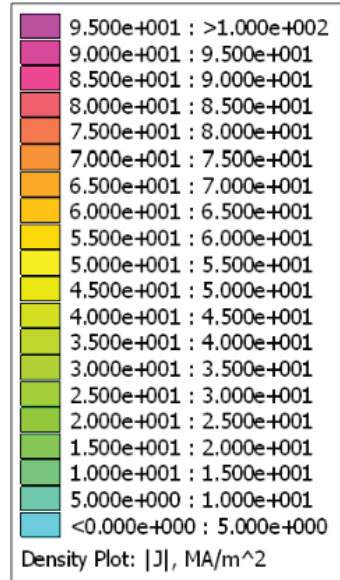
$$I_{1,rms} = I_{2,rms} = 1 \text{ A}$$

Numerical field and current density solutions using FEMM (Finite Element Method Magnetics), a free 2D solver, <http://www.femm.info/wiki/HomePage>

## Flux density magnitude

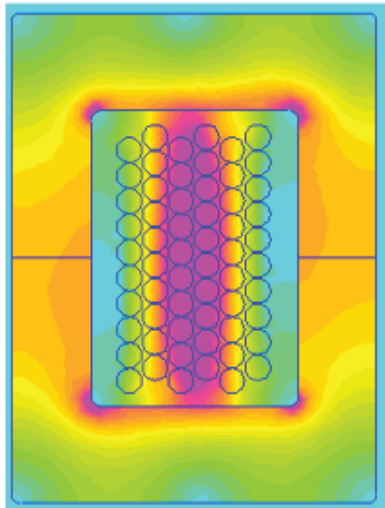


## Current density magnitude

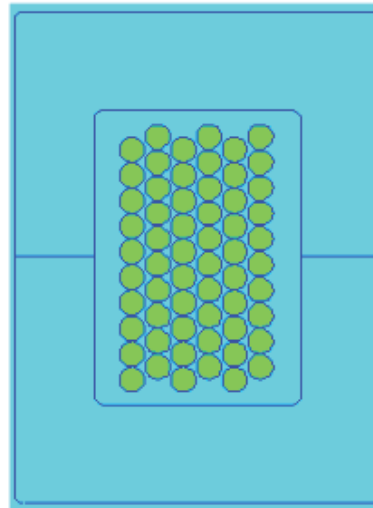


## Frequency: 1 kHz

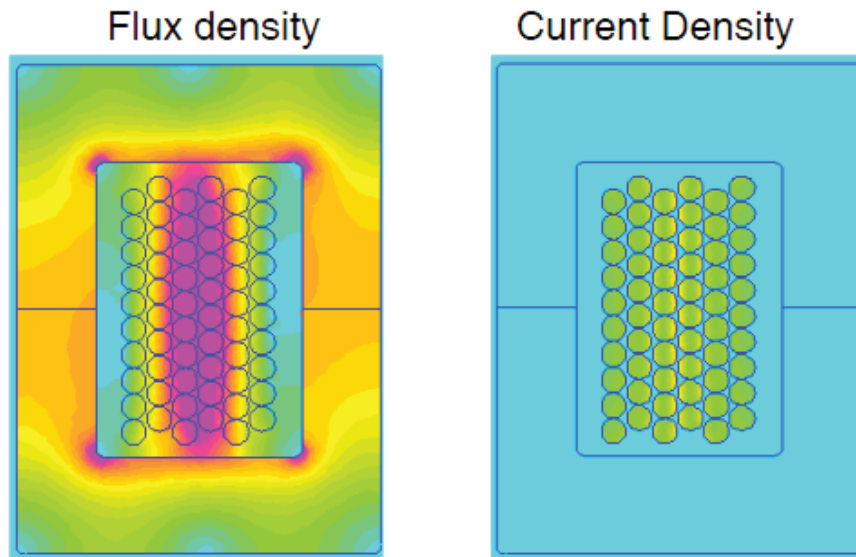
Flux density



Current Density

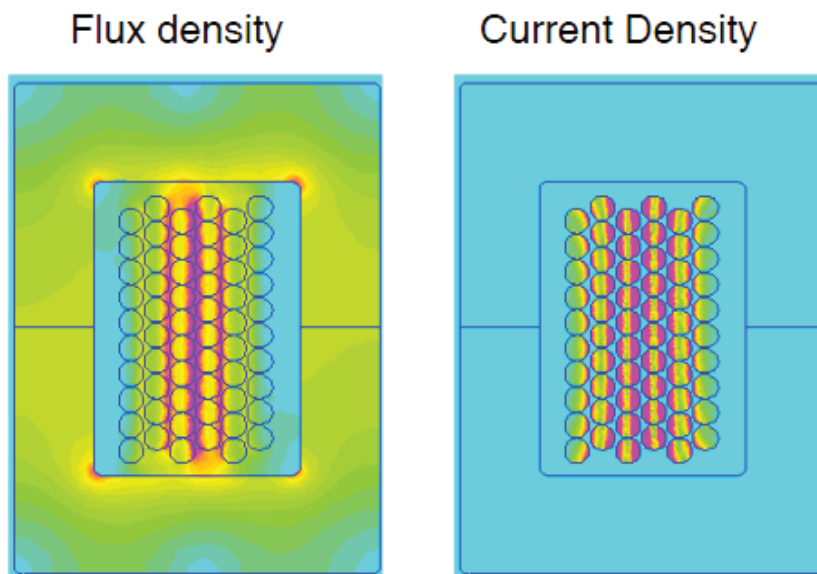


# Frequency: 100 kHz



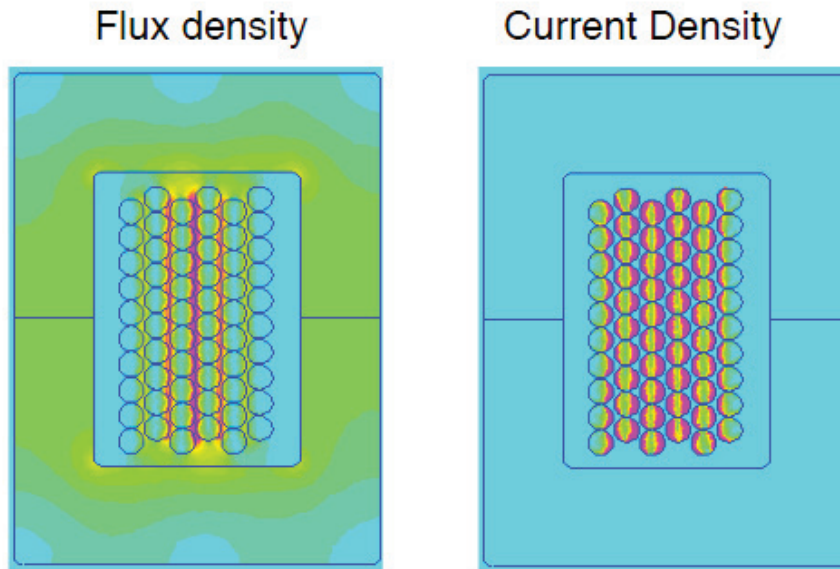
Total copper losses 1.8 larger than at 1 kHz

# Frequency: 1 MHz



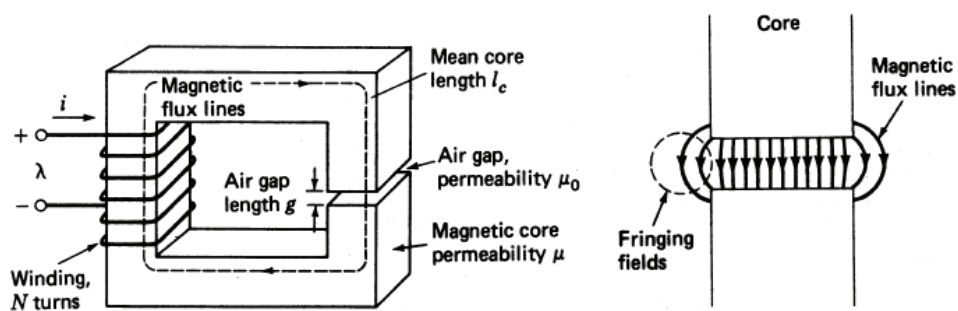
Total copper losses 20 times larger than at 1 kHz

# Frequency: 10 MHz



Very significant proximity effect  
Total copper losses = 65 times larger than at 1 KHz

## Fringing



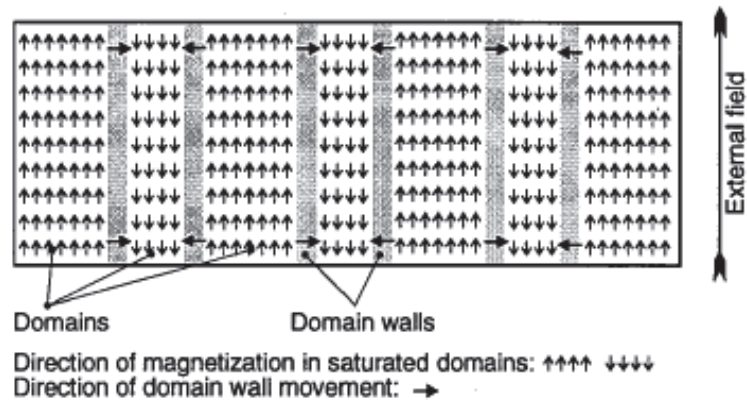
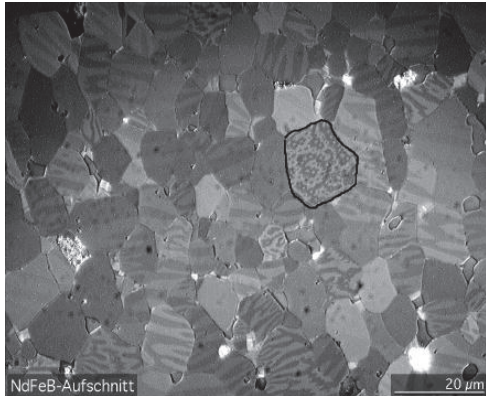
A simple magnetic circuit with an air gap

- Near air gap, flux may bow out significantly, causing additional eddy current losses in nearby conductors



# Physical Origin of Core Loss

- Magnetic material is divided into “domains” of saturated material
- Both Hysteresis and Eddy Current losses occur from domain wall shifting



Reinert, J.; Brockmeyer, A.; De Doncker, R.W.; , "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation,"

## Inductor Core Loss

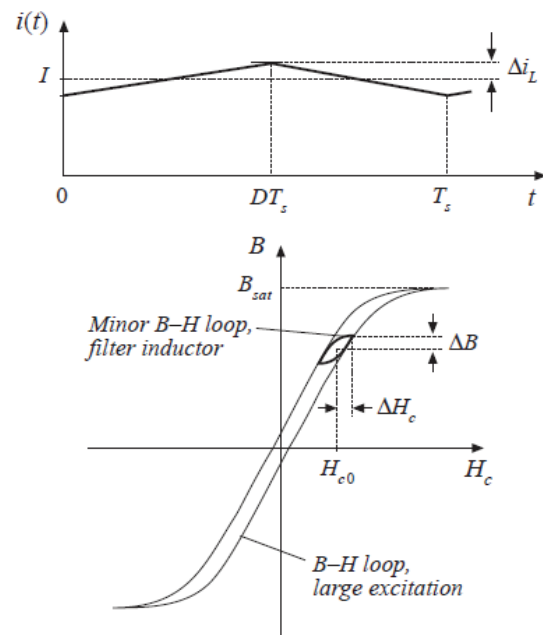
- Governed by Steinmetz Equation:

$$P_v = K_{fe} f_s^\alpha (\Delta B)^\beta \quad [\text{mW}/\text{cm}^3]$$

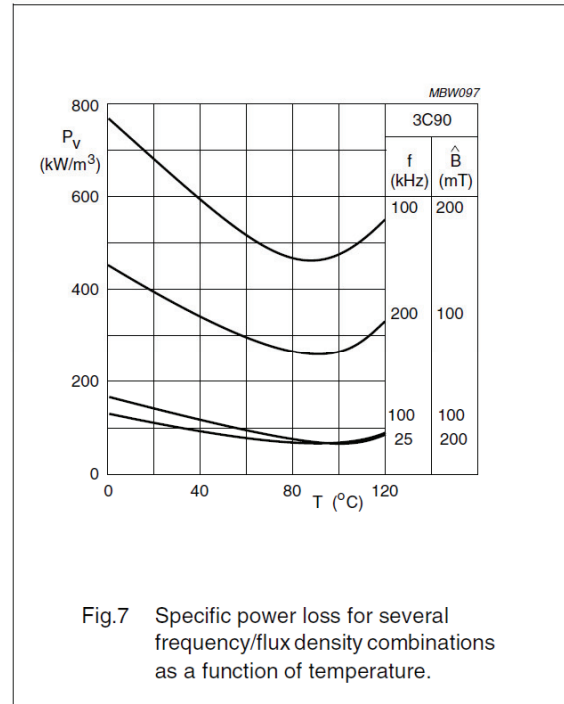
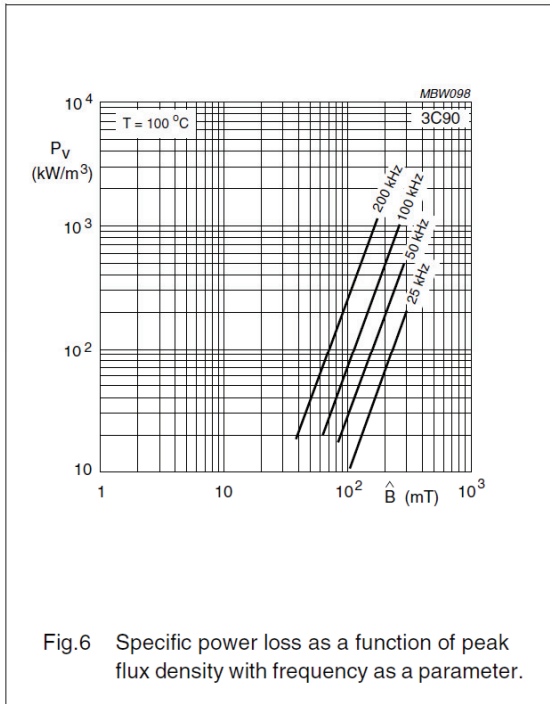
- Parameters  $K_{fe}$ ,  $\alpha$ , and  $\beta$  extracted from manufacturer data

$$P_{fe} = P_v A_c l_m \quad [\text{mW}]$$

- $\Delta B \propto \Delta i_L \rightarrow$  small losses with small ripple



# Steinmetz Parameter Extraction



## Ferroxcube Curve Fit Parameters

Power losses in our ferrites have been measured as a function of frequency ( $f$  in Hz), peak flux density ( $B$  in T) and temperature ( $T$  in  $^{\circ}\text{C}$ ). Core loss density can be approximated <sup>(2)</sup> by the following formula :

$$P_{core} = C_m \cdot f^x \cdot B_{peak}^y \cdot (ct_0 - ct_1 T + ct_2 T^2) \quad [3]$$

$$= C_m \cdot C_T \cdot f^x \cdot B_{peak}^y \quad [\text{mW/cm}^3]$$

ferrite	f (kHz)	$C_m$	x	y	$ct_2$	$ct_1$	$ct_0$
3C30	20-100	$7.13 \cdot 10^{-3}$	1.42	3.02	$3.65 \cdot 10^{-4}$	$6.65 \cdot 10^{-2}$	4
	100-200	$7.13 \cdot 10^{-3}$	1.42	3.02	$4 \cdot 10^{-4}$	$6.8 \cdot 10^{-2}$	3.8
3C90	20-200	$3.2 \cdot 10^{-3}$	1.46	2.75	$1.65 \cdot 10^{-4}$	$3.1 \cdot 10^{-2}$	2.45
3C94	20-200	$2.37 \cdot 10^{-3}$	1.46	2.75	$1.65 \cdot 10^{-4}$	$3.1 \cdot 10^{-2}$	2.45
	200-400	$2 \cdot 10^{-9}$	2.6	2.75	$1.65 \cdot 10^{-4}$	$3.1 \cdot 10^{-2}$	2.45
3F3	100-300	$0.25 \cdot 10^{-3}$	1.63	2.45	$0.79 \cdot 10^{-4}$	$1.05 \cdot 10^{-2}$	1.26
	300-500	$2 \cdot 10^{-5}$	1.8	2.5	$0.77 \cdot 10^{-4}$	$1.05 \cdot 10^{-2}$	1.28
	500-1000	$3.6 \cdot 10^{-9}$	2.4	2.25	$0.67 \cdot 10^{-4}$	$0.81 \cdot 10^{-2}$	1.14
3F4	500-1000	$12 \cdot 10^{-4}$	1.75	2.9	$0.95 \cdot 10^{-4}$	$1.1 \cdot 10^{-2}$	1.15
	1000-3000	$1.1 \cdot 10^{-11}$	2.8	2.4	$0.34 \cdot 10^{-4}$	$0.01 \cdot 10^{-2}$	0.67

Table 1: Fit parameters to calculate the power loss density

# NSE/iGSE

$$P_{NSE} = \left(\frac{\Delta B}{2}\right)^{\beta-\alpha} \frac{k_N}{T} \int_0^T \left|\frac{dB}{dt}\right|^\alpha dt$$

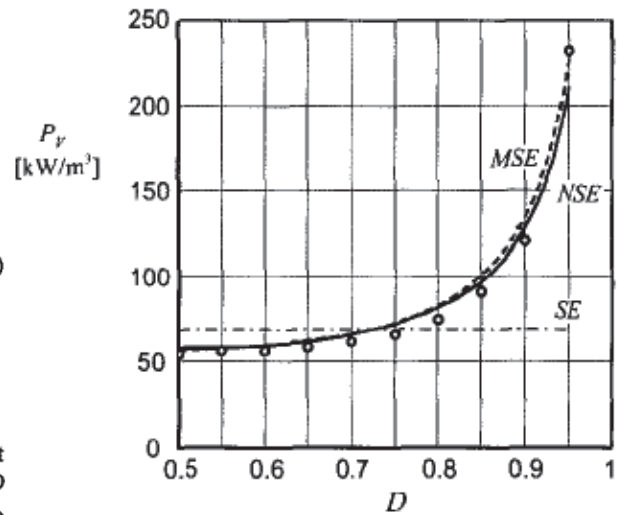
$$k_N = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^\alpha d\theta}$$

## Simple Formula for Square-wave voltages:

$$P_{NSE} = k_N (2f)^\alpha (\Delta B)^\beta (D^{1-\alpha} + (1-D)^{1-\alpha}) \quad (10)$$

where  $f$  is the operating frequency;  
 $\Delta B / 2$  is the peak induction;  
 $D$  is the duty ratio of the square wave voltage.

*Note:* The second and third harmonics are dominant at moderate values of duty ratio  $D$ . For extreme values of  $D$  (95%), a higher value of  $\alpha$  could give better matching to the actual losses.



Van den Bossche, A.; Valchev, V.C.; Georgiev, G.B.; , "Measurement and loss model of ferrites with non-sinusoidal waveforms,"  
 K. Venkatachalam; C. R. Sullivan; T. Abdallah; H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only  
 Steinmetz parameters"

## INDUCTOR DESIGN

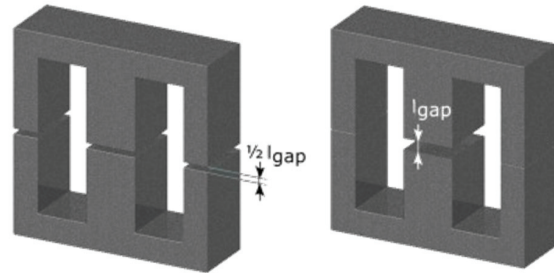
# Inductor Design

## Freedoms:

1. Core Size and Material
2. Number of turns and wire gauge
3. Length of Air Gap

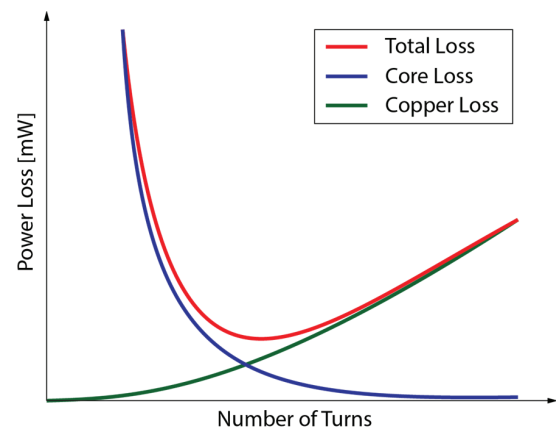
## Constraints:

1. Obtain Designed  $L$
2. Prevent Saturation
3. Minimize Losses



## Minimization of Losses

- For given core, number of turns can be used to index possible designs, with air gap solved after (and limited) to get correct inductance
- A minimum sum of the two exists and can be solved
- Design always subject to constraint  $B_{max} < B_{sat}$



# Spreadsheet Design

The spreadsheet displays the following key parameters and results:

- Fixed Design Params:**  $V_g$  [V] = 25,  $V_{out}$  [V] = 50,  $dV$  [V] = 2,  $u_0$  =  $1.257E-06$ ,  $\rho$  [Ohm] =  $1.68E-06$ ,  $TA$  [C] = 25.
- Design Choice:**  $P_{max}$  [W] = 250,  $L$  [uH] = 250,  $f_s$  [kHz] =  $2.00E+01$ .
- Gate Driver:**  $V_{dr}$  [V] = 12,  $dt$  [ns] = 500,  $R_{g\_on}$  [Ohm] = 10,  $R_{g\_off}$  [Ohm] = 2.
- Current Stresses:**  $I_{out}$  [A] = 5.00,  $I_L$  [A] = 10.00,  $dI$  [A] = 1.25,  $I_{max}$  [A] = 11.25,  $I_{min}$  [A] = 8.75,  $I_{rms}$  [A] = 10.03,  $I_{q1,rms}$  [A] = 0.72,  $I_{q2,rms}$  [A] = 7.09,  $I_{rms}$  [A] = 7.09,  $I_{l,rms}$  [A] = 5.03.
- MOSFET Losses:**  $t_{sw,on}$  [ns] = 175,  $t_{sw,off}$  [ns] = 35,  $P_{rr}$  = 1.16,  $P_{q1,ov}$  = 1.18,  $P_{q2,bd}$  = 0.32,  $P_{q1,Coss}$  = 0.00,  $P_{q1,Cond}$  = 0.12,  $P_{q2,Cond}$  = 0.12.
- Total Losses:**  $P_{I,DC}$  [mOhm] = 4.71,  $P_{I,AC}$  [mOhm] = 10.05,  $P_{I,copper}$  = 0.48,  $P_{I,core}$  = 0.06,  $P_{I,W}$  = 0.54,  $P_{q1[W]}$  = 2.48,  $P_{q2[W]}$  = 0.44, **Ploss** = 3.44.
- Efficiency:** **Eff** = 98.64.
- Core Geometry:** Core = ETD43-3C90,  $A_c$  [mm<sup>2</sup>] = 211,  $W_a$  [mm<sup>2</sup>] = 273,  $V_e$  [mm<sup>3</sup>] = 24000,  $MLT$  [mm] = 85.
- Core Material Parameters:**  $\mu_i$  = 2300,  $B_{sat}$  [mT] = 470,  $C_m$  = 0.0032,  $\alpha$  = 1.46,  $\beta$  = 2.75,  $\alpha_2$  = 0.000165,  $\alpha_1$  = 0.031,  $\alpha_0$  = 2.45.
- Inductor Design:**  $\Delta B$  [T] = 0.05,  $B_{max}$  [mT] = 0.44,  $l_g$  [mm] = 0.95,  $A_w$  [mm<sup>2</sup>] = 3.1,  $n_w$  [mm] = 1.70,  $SkinDepth$  [mm] = 0.48.
- Other Parameters:**  $R_{on}$  [mOhm] = 2.3,  $Q_g$  [nC] = 210,  $V_f$  [V] = 2,  $Q_{rr}$  [nC] = 287,  $C_{oss}$  [pF] = 4000,  $t_{rr}$  [ns] = 100,  $C$  [uF] = 31.25,  $R_{th}$  [K/W] = 3,  $T_{Q1}[C]$  = 32.4,  $T_{Q2}[C]$  = 28.3,  $Desig\ G$  = 16.64.

**Warnings:** Wire significantly thicker than one skin depth, AC losses may be significant.

- Use of spreadsheet permits simple iteration of design
- Can easily change core, switching frequency, loss constraints, etc.

# Matlab (Programmatic) Design

```

1 function [n, lg, Pq1, Pq2, Pl, eta, Cmin] = TestBoostDesign(Pmax, fs, L, dt, core_geom, core_mat, MOSFET)
2 %TestBoostDesign calculate boost conveter efficiency and temperature rise
3 %for various designs
4 % fs = switching frequency (in Hz)
5 % L = inductance (in Henries)
6 % n = number of turns on inductor
7 % dt = switching dead time (in seconds)
8 % core_geom = core geometry, chosen from 'EFD25', 'ETD29', 'ETD39', 'ETD44', or 'ETD49'
9 % core_mat = core material, chosen from '3F3', '3C90', or '3F4'
10 % MOSFET = MOSFET selection, chosen from 'AOT', 'FDP', 'IPP2', 'IRF',
11 % 'CSD' or 'IPP0'
12
13 Vg = 25;
14 Vout = 50;
15 Iout = Pmax/Vout;
16 Ts = 1/fs;
17 D = 1-Vg/Vout;
18 dVout = 2;
19 Vdr = 12;
20
21 Rgon = 10;
22 Rgoff = 2;
23
24 rho = 1.724e-6; %ohms*cm
25 u0 = 4*pi*1e-7;
26
27 %% Inductor Datasheet Parameters
28 switch core_geom
29 case 'EFD25'
30     MLT = 46.4; %mm
31     Ac = 58; %mm^2
32     Ve = 3300; %mm^3
33     Wa = 40.2; %mm^2

```

- Matlab, or similar, permits more powerful iteration and plotting/insight into design variation

# Closed-Form Design Methods

- **Fundamentals of Power Electronics Ch 13-15**
  - Step-by-Step design methods
  - Simplified, and may require additional calculations

## $K_g$ and $K_{gfe}$ Methods

- Two closed-form methods to solve for the optimal inductor design *under certain constraints/assumptions*
- Neither method considers losses other than DC copper and (possibly) Steinmetz core loss
- Both methods particularly well suited to spreadsheet/iterative design procedures

	$K_g$	$K_{gfe}$
Losses	DC Copper (specified)	DC Copper, SE Core Loss (optimized)
Saturation	Specified	Checked After
$B_{max}$	Specified	Optimized

# $K_g$ Method

- Method useful for filter inductors where  $\Delta B$  is small
- Core loss is not included, but may be significant particularly if large ripple is present
- Copper loss is specified through a set target resistance
- The desired  $B_{max}$  is given as a constraint
- Method does not check feasibility of design; must ensure that air gap is not extremely large or wire size excessively small
- Simple first-cut design technique; useful for determining approximate core size required
- Step-by-step design procedure included on website

The following quantities are specified, using the units

Wire resistivity	$\rho$	( $\Omega$ -cm)
Peak winding current	$I_{max}$	(A)
Inductance	$L$	(H)
Winding resistance	$R$	( $\Omega$ )
Winding fill factor	$K_u$	
Core maximum flux density	$B_{max}$	(T)

The core dimensions are expressed in cm:

Core cross-sectional area	$A_c$	( $\text{cm}^2$ )
Core window area	$W_A$	( $\text{cm}^2$ )
Mean length per turn	$MLT$	(cm)

$$K_g \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u} 10^8 \quad (\text{cm}^5)$$

$$\ell_g = \frac{\mu_0 L I_{max}^2}{B_{max}^2 A_c} 10^4 \quad (\text{m})$$

$$n = \frac{L I_{max}}{B_{max} A_c} 10^4$$

$$A_w \leq \frac{K_u W_A}{n} \quad (\text{cm}^2)$$

$$R = \frac{\rho n (MLT)}{A_w} \quad (\Omega)$$



# $K_{gfe}$ Method

- Method useful for cases when core loss and copper loss are expected to be significant
- Saturation is not included in the method, rather it must be checked afterward
- Enforces a design where the sum of core and copper is minimized

# $K_{gfe}$ Procedure

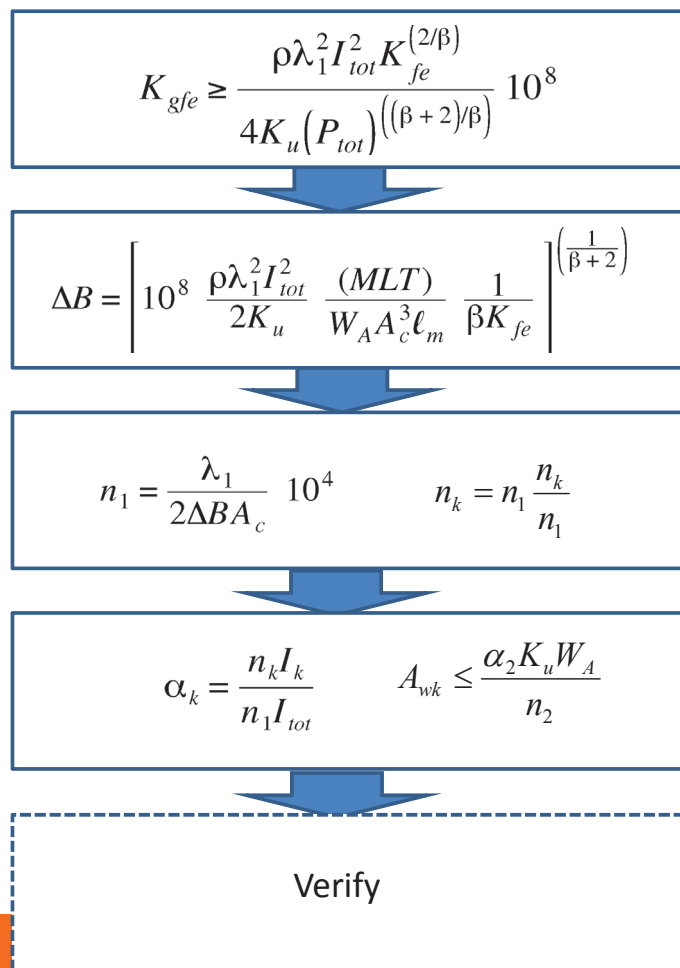
The following quantities are specified, using the units noted:

Wire effective resistivity	$\rho$	( $\Omega$ -cm)
Total rms winding current, ref to pri	$I_{tot}$	(A)
Desired turns ratios	$n_2/n_1, n_3/n_1, \text{ etc.}$	
Applied pri volt-sec	$\lambda_1$	(V-sec)
Allowed total power dissipation	$P_{tot}$	(W)
Winding fill factor	$K_u$	
Core loss exponent	$\beta$	
Core loss coefficient	$K_{fe}$	(W/cm <sup>3</sup> T <sup><math>\beta</math></sup> )

Other quantities and their dimensions:

Core cross-sectional area	$A_c$	(cm <sup>2</sup> )
Core window area	$W_A$	(cm <sup>2</sup> )
Mean length per turn	$MLT$	(cm)
Magnetic path length	$\ell_e$	(cm)
Wire areas	$A_{w1}, \dots$	(cm <sup>2</sup> )
Peak ac flux density	$\Delta B$	(T)





## $K_{gfe}$ Method: Summary

- Method enforces an operating  $\Delta B$  in which core and copper losses are minimized
- Only takes into account losses from standard Steinmetz equation; not correct unless waveforms are sinusoidal
- Does not consider high frequency losses
- Step-by-step design procedure included on website