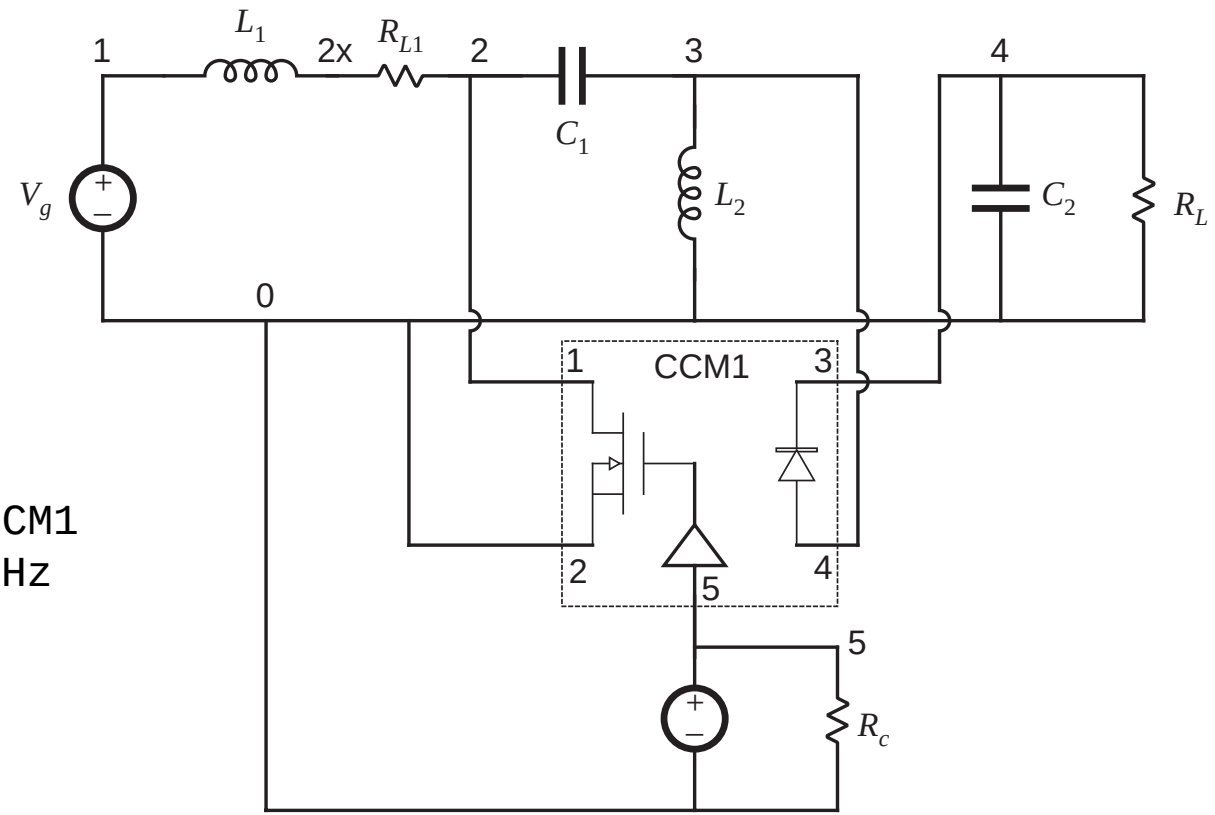
Basic CCM SEPIC Example
Frequency Response

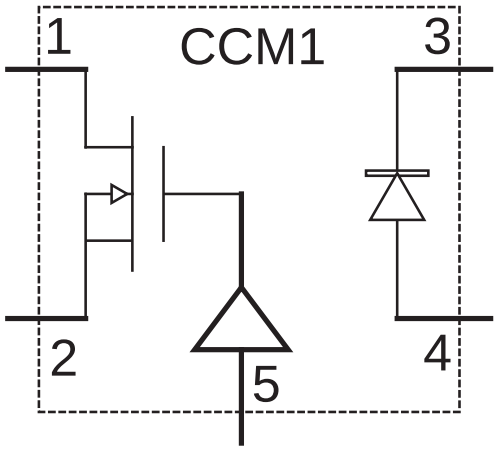
```
Ideal SEPIC frequency response
.lib switch.lib
Vg 1 0 dc 120V
L1 1 2x 800uH
RL1 2x 2 1U
C1 2 3 100uF
L2 3 0 100uH
C2 4 0 100uF
RL 4 0 40
Vc 5 0 dc 0.4 ac 1
Rc 5 0 1M
Xswitch 2 0 4 3 5 CCM1
.ac DEC 201 10 100kHz
.PROBE
.end
```



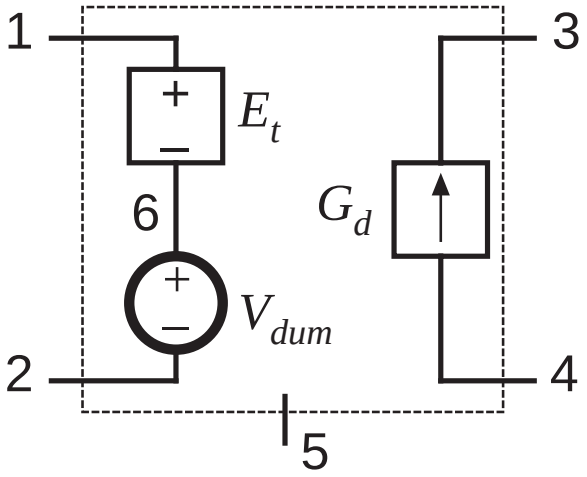
Switch Library File

```
.subckt CCM1 1 2 3 4 5
Et 1 6 value={(1-v(5))*v(3,4)/v(5)}
Vdum 6 2 0
Gd 4 3 value={(1-v(5))*i(Vdum)/v(5)}
.ends
```

Symbol



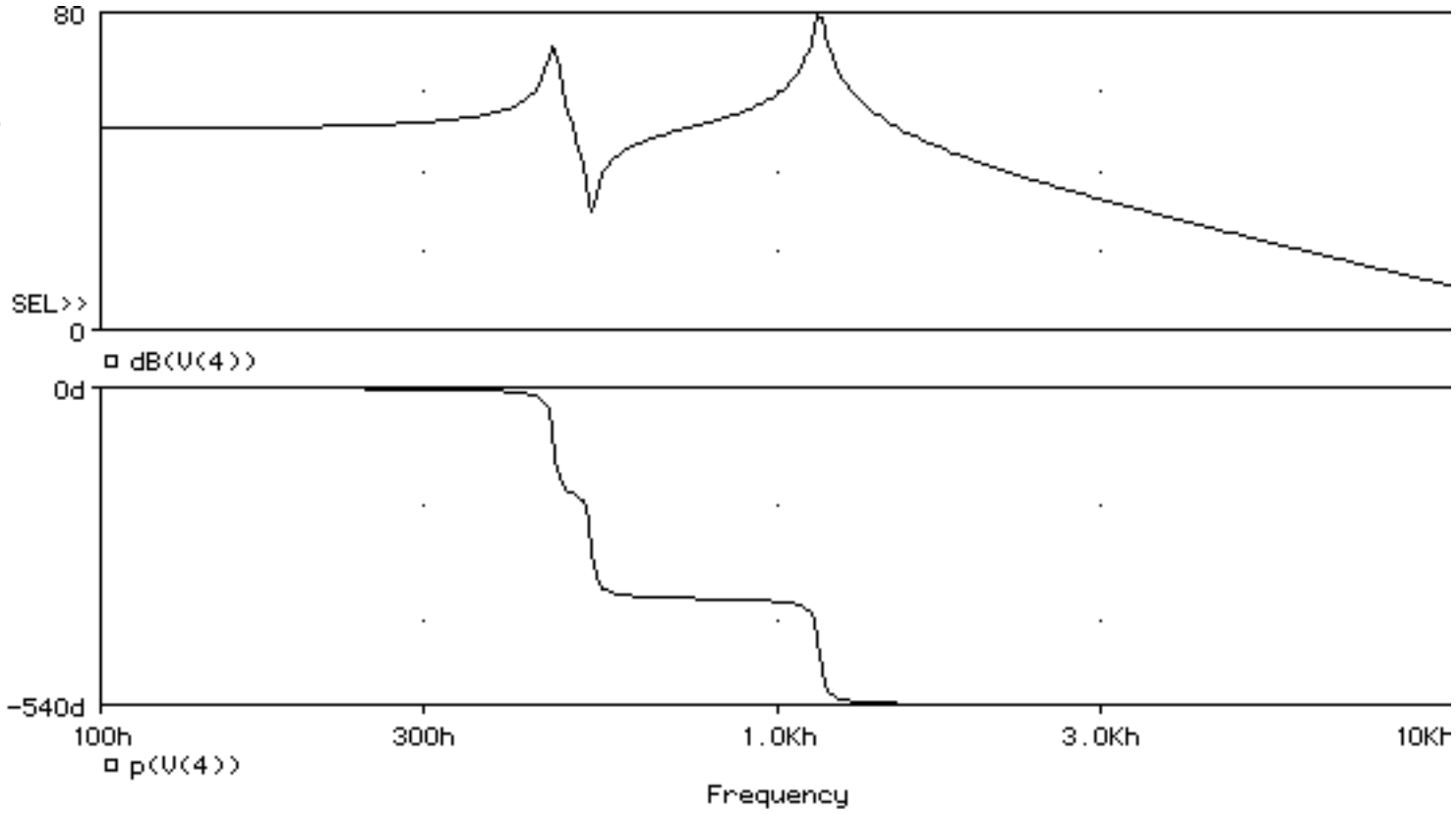
Subcircuit



PROBE Output
SEPIC Example: Control-to-output transfer function

Magnitude

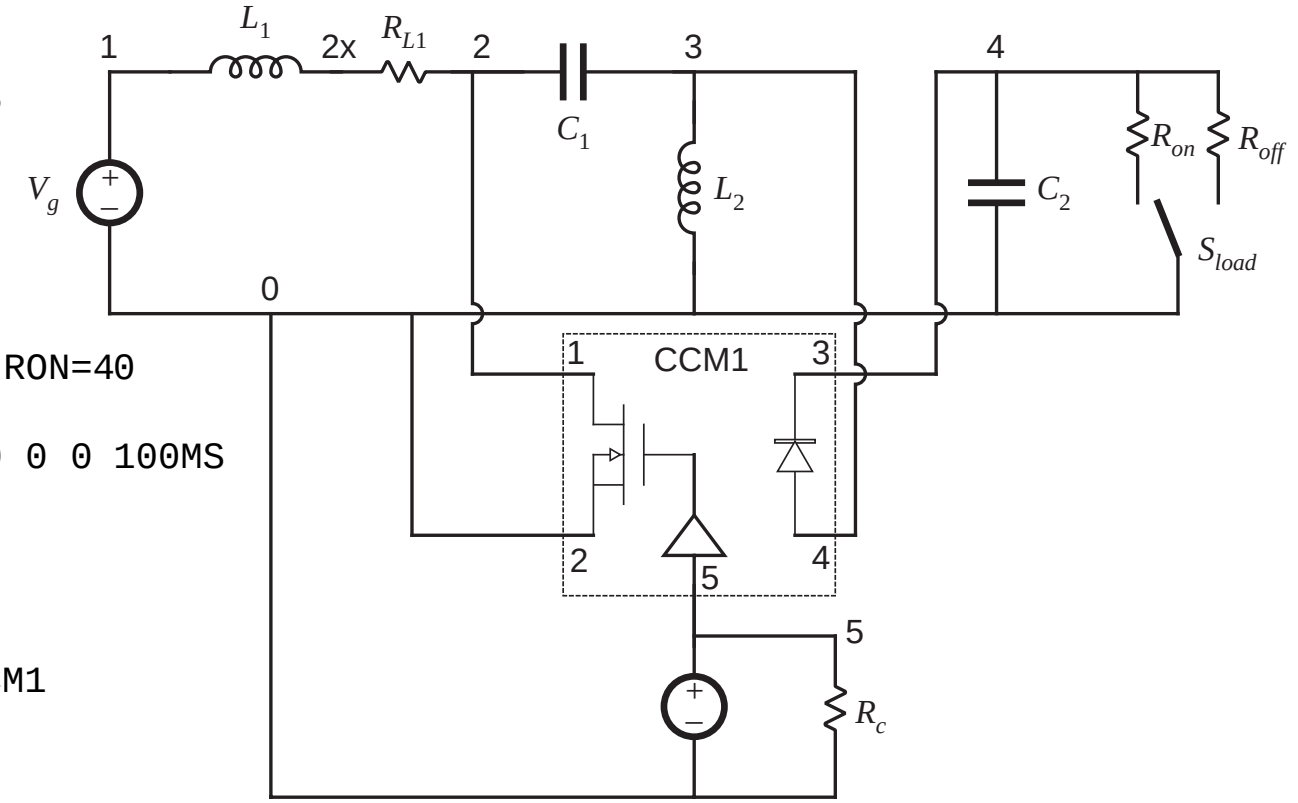
Phase



Transient response

Step change in load resistance

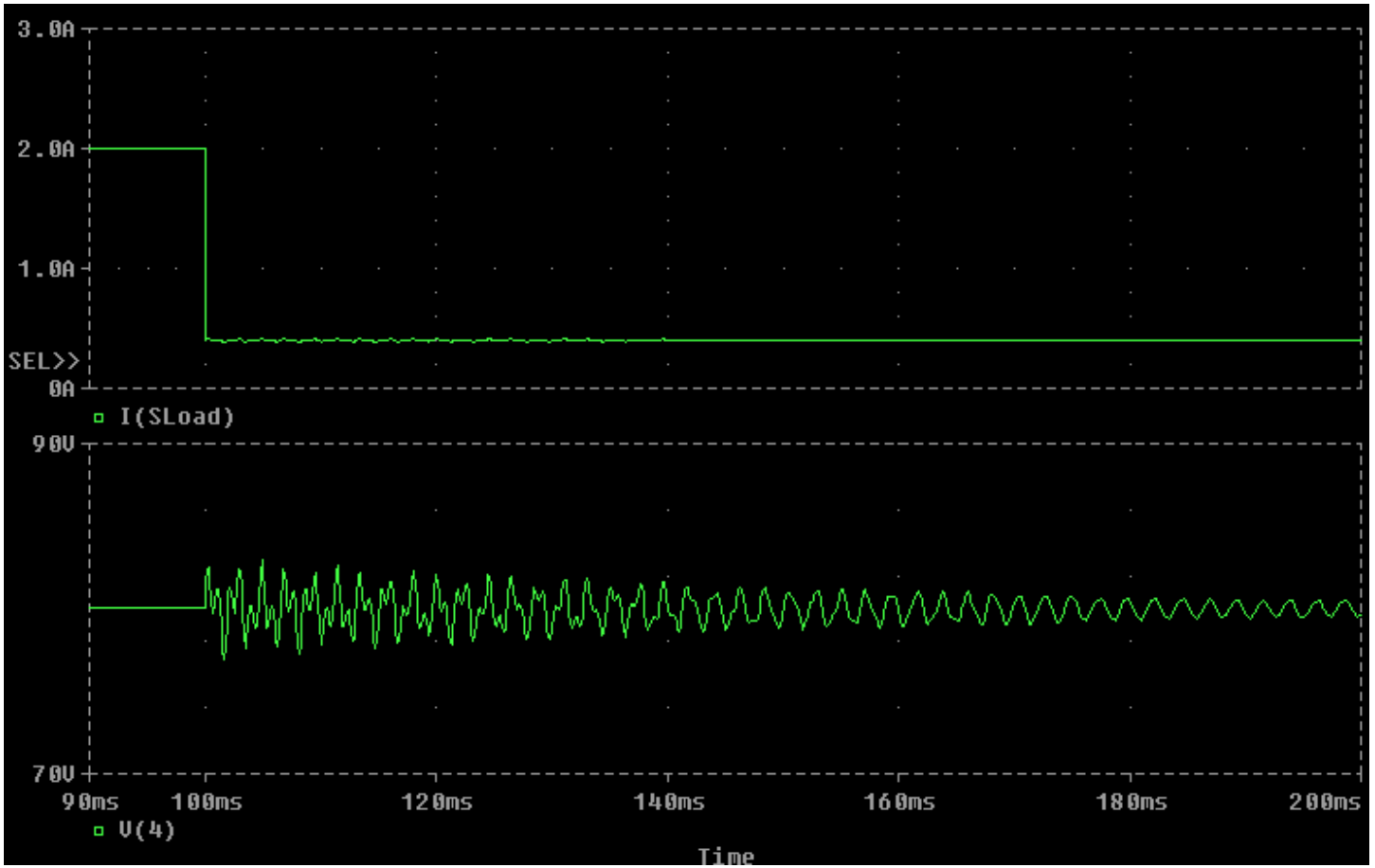
```
Ideal SEPIC transient response
.lib switch.lib
Vg 1 0 dc 120V
L1 1 2x 800uH IC=1.5
RL1 2x 2 1U
C1 2 3 100uF IC=120
L2 3 0 100uH IC=2
C2 4 0 100uF IC=80
SLoad 4 0 6 0 load
.MODEL load VSWITCH RON=40
  ROFF=200
VLC 6 0 PULSE(-2 2 0 0 0 100MS
  200MS)
RLC 6 0 1M
Vc 5 0 dc 0.4 ac 1
Rc 5 0 1M
Xswitch 2 0 4 3 5 CCM1
.tran 5US 200MS UIC
.PROBE
.end
```



Transient simulation: PROBE output
SEPIC example

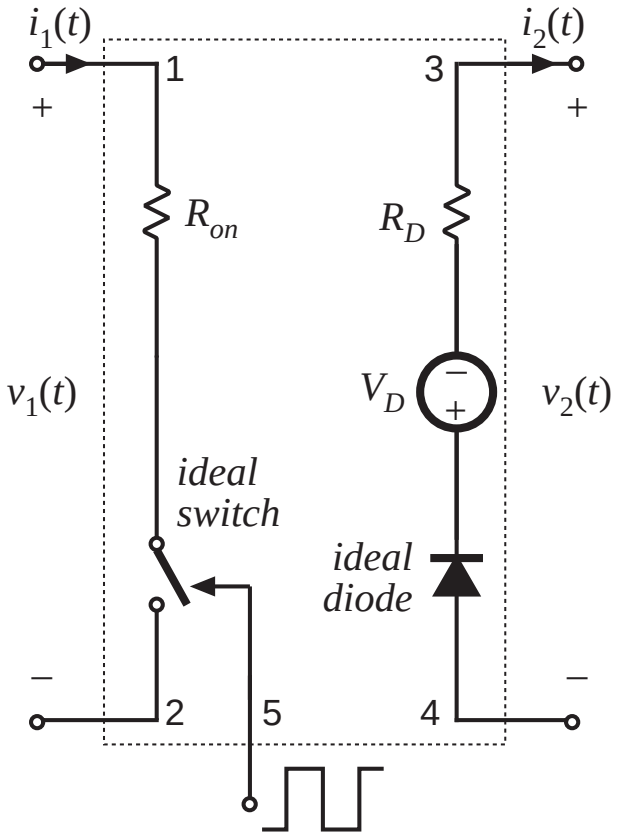
Load current

Output voltage



Inclusion of switch ON-resistance

Circuit:

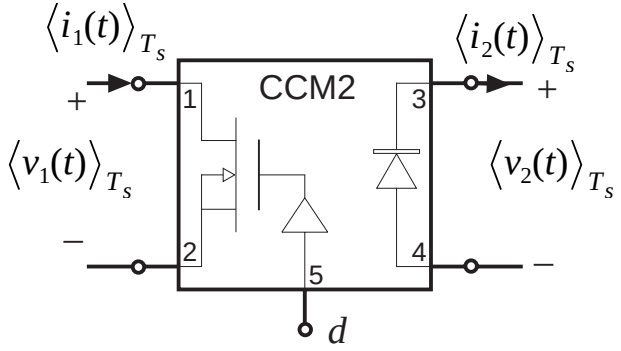


Averaged equations:

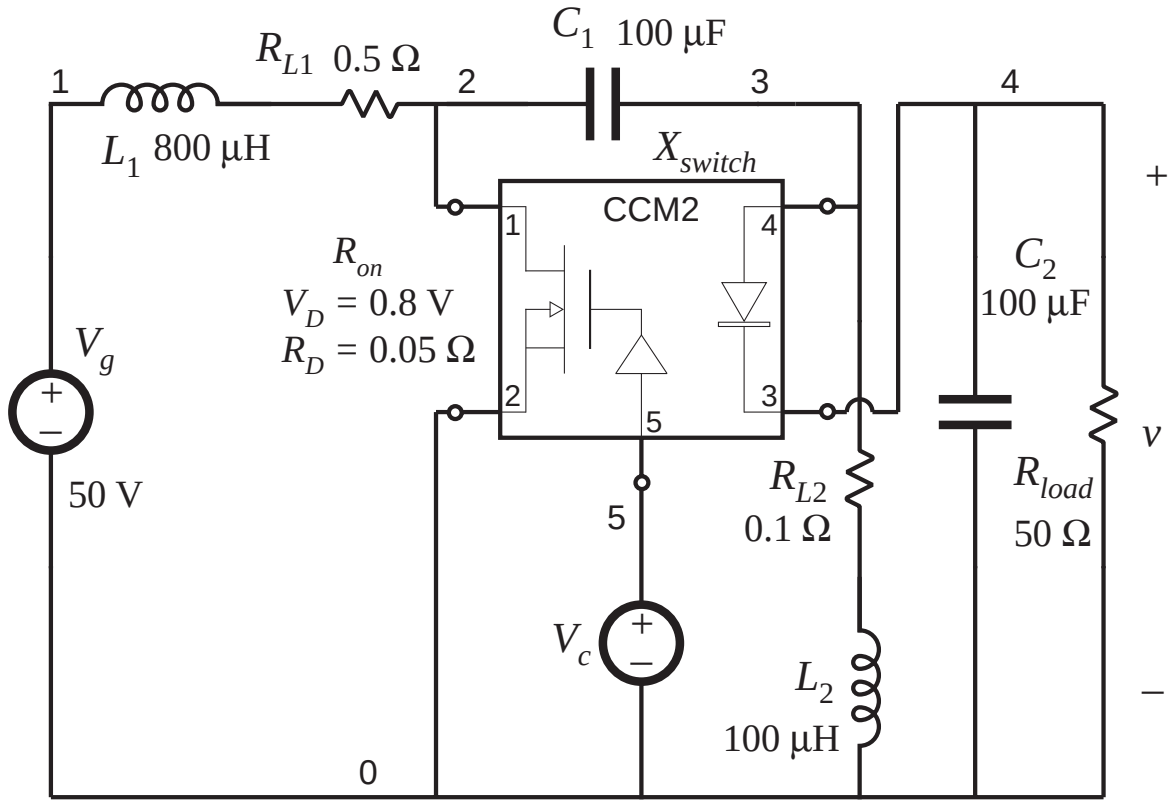
$$\left\langle v_1(t)\right\rangle_{T_s} = \left(\frac{R_{on}}{d(t)} + \frac{d'(t)R_D}{d^2(t)}\right)\left\langle i_1(t)\right\rangle_{T_s} + \frac{d'(t)}{d(t)}\left(\left\langle v_2(t)\right\rangle_{T_s} + V_D\right)$$

$$\left\langle i_2(t)\right\rangle_{T_s} = \frac{d'(t)}{d(t)}\left\langle i_1(t)\right\rangle_{T_s}$$

Subcircuit model:



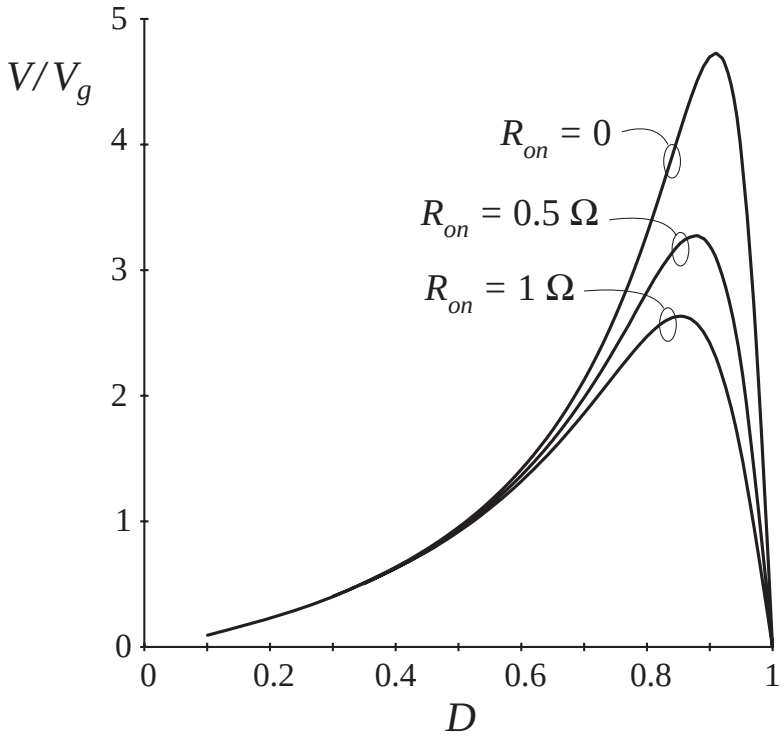
Modeling losses in SEPIC example

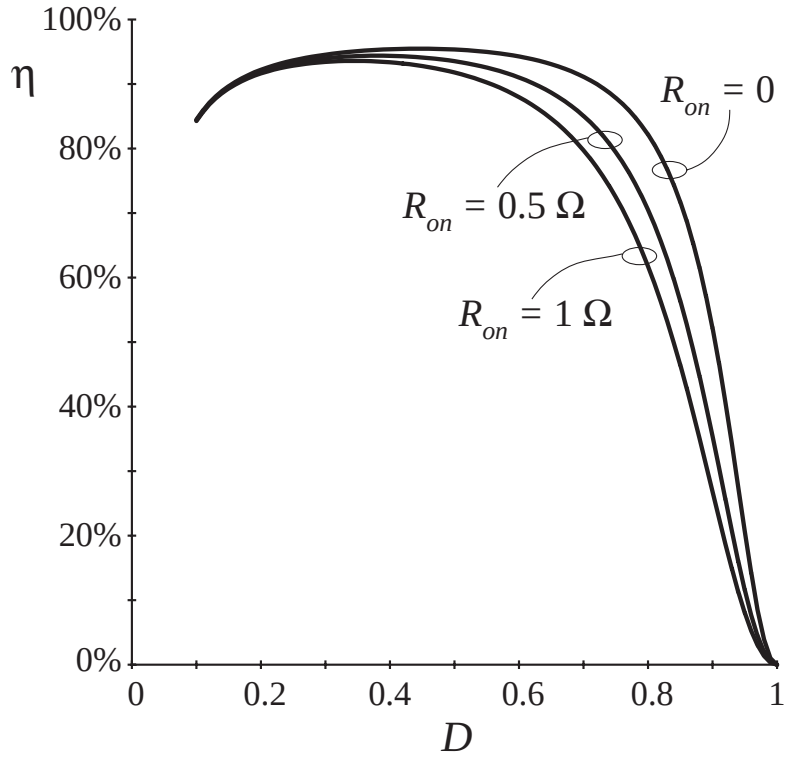


see Fig. B.4 for netlist

—DC analysis with stepped on-resistance parameter

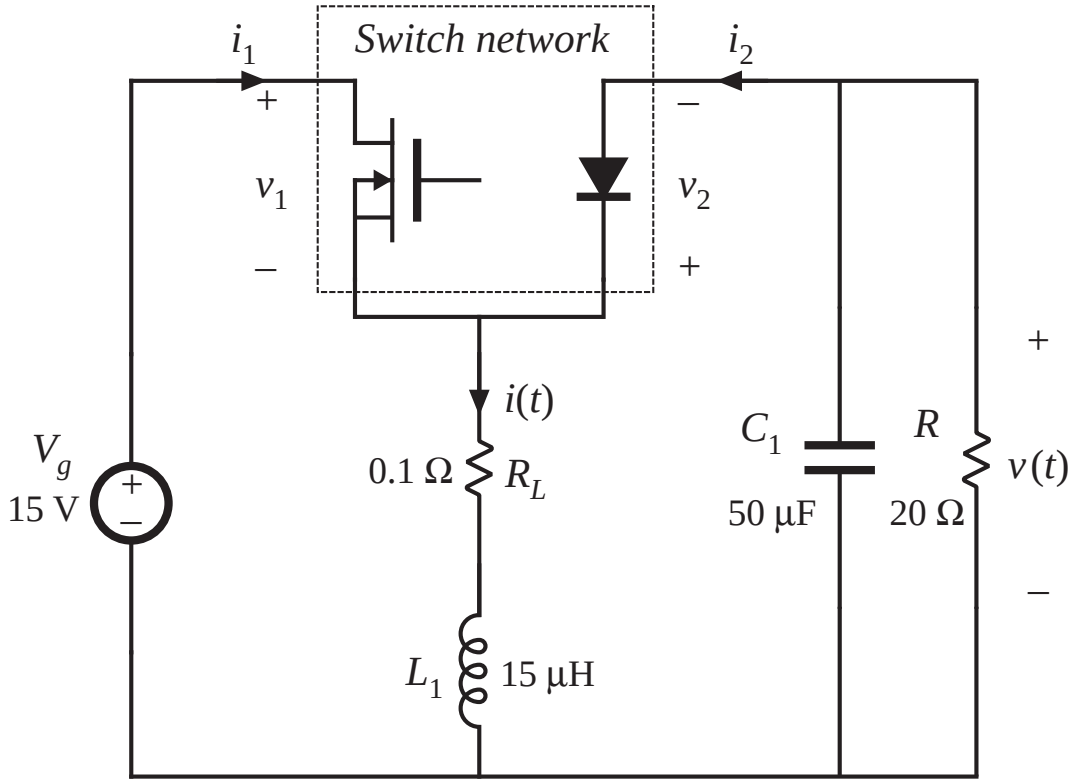
Results
Conduction losses in SEPIC





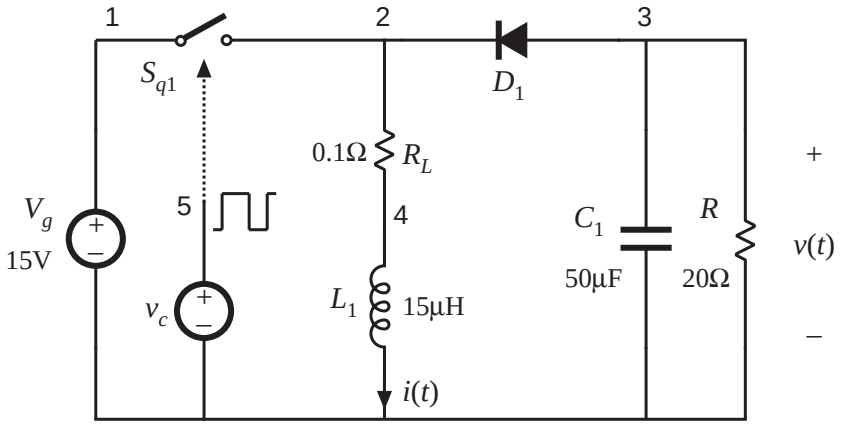
Comparison of simulation approaches
Transient response

Buck-boost example

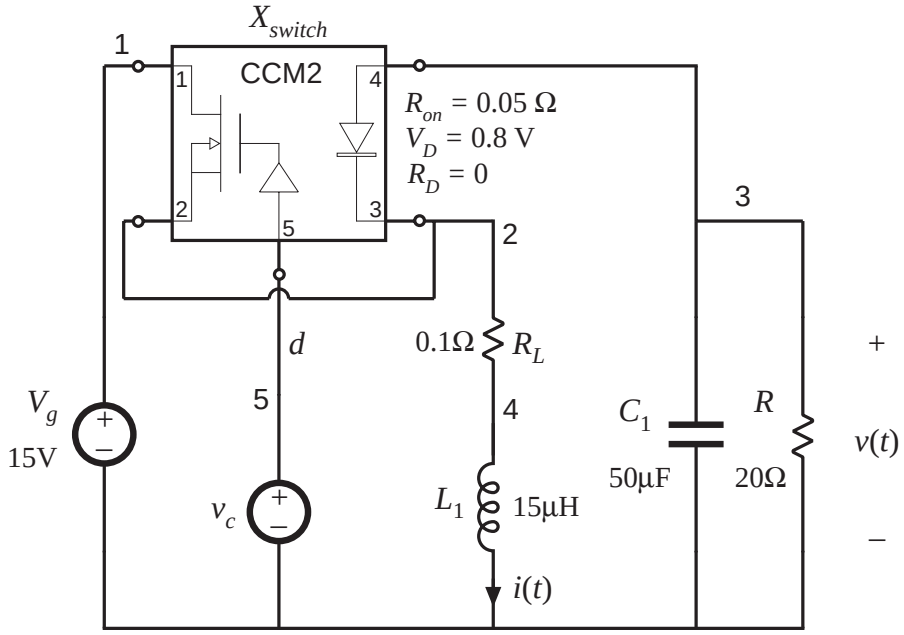


Two approaches

Using ideal switch



Using averaged model



Results of simulations
Turn-on transient