connections; use these as a starting point for your PCB design. As you select new components for this lab, include the schematic symbols and PCB footprints that you create in these libraries for better organization. **Do not** rely on the connections, footprints, or design in these starter files without reviewing to ensure they meet your needs.

## III.    Motor Driver Implementation

The motor driver must consist of a three phase inverter with each leg comprised by a transistor half-bridge. Additionally, relevant high- and low-side transistor drivers should be selected so that the devices may be switched on and off. Your driver circuit implementation must be capable of switching each half bridge into one of three states. The states are given in Table I; the circuit must be able to hold each half bridge independently in any one of the three states for an arbitrary time (i.e. an adjustable dead time alone is not sufficient to implement State 0).

TABLE I: HALF BRIDGE STATES IN DRIVE TRAIN INVERTER

| State | High Side Device | Low side Device |
|-------|------------------|-----------------|
| 0     | Off              | Off             |
| 1     | Off              | On              |
| 2     | On               | Off             |

In the starter files, three example motor drive implementations are given. You may select to start your design from one of these three, or change it entirely.

## IV.    Circuit Connections and Protection

Figs. 3 and 4 detail the electric bicycle platform to which you will attach your completed power converter drivetrain PCB, as well as the included circuit protection devices.
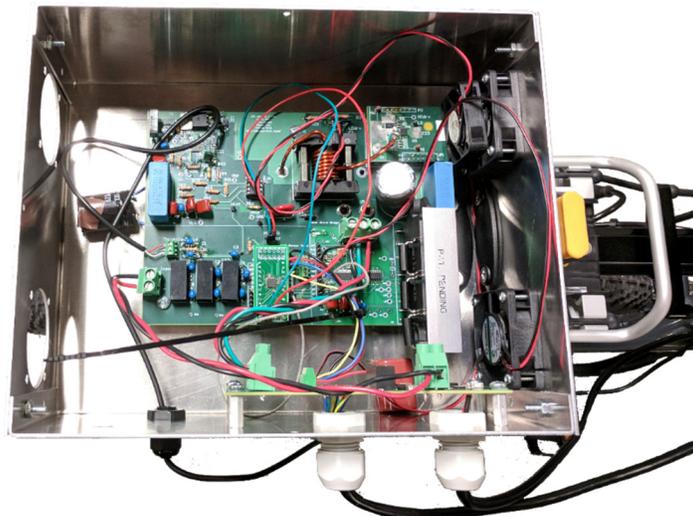


**Figure 3**: Circuit enclosure and protection board (example student PCB included

For all parts that the teams are requesting to be ordered, teams must submit immediately actionable resources for ordering. For vendors including Digikey and Mouser, this can be achieved by links to carts. For other vendors, quote documentation with ordering information will suffice.

## VI.    Design Completion

All circuit boards will be ordered with Sierra Circuits' NoTouch, 4-layer specifications. Details are given at https://www.protoexpress.com/NoTouch-pcb/product-specs.jsp, except as specified below. Each group will receive two (2) copies of their PCB layout. Prior to submission, each layout must successfully pass the AFV check here: https://www.protoexpress.com/orderProc/noTouchNew.jsp, with no issues found. The quote should be specified with

- 4-day turn
- 5 mil minimum trace/space
- 15 mil hole size

- 2 board quantity
- (up to) 4 layers

*Note: Sierra Circuits' AFV process may be unable to complete outside of business hours if the board has issues that cannot be resolved in an automated manner. Plan to complete your layout well before the deadline to ensure that an error-free AFV can be submitted before the deadline.*

Teams must submit, by e-mail to the instructor, one .zip archive of the completed PCB layout. The layout must successfully pass Sierra Circuits' AFV check prior to submission. The zip archive should contain the following file types from the Altium project:

1.    PrjPcb
2.    SchDoc
3.    SchLib

4.    PcbLib
5.    PcbDoc
6.    BOM

In your e-mail include your username and password (make sure to change your password to something not used for any other personal account) to the Sierra Circuits webpage. Prior to submission, move all quotes *except* the one final board which has passed AFV to your old/hidden folder.

## VII.    Deliverables

You will not complete a lab report for this experiment. Instead, you will turn in the following, as a compressed archive submitted through Canvas

1. Direct, actionable purchasing links/materials for all components
2. Sierra Circuits login information to your account, with **only** your final design in the "Main Folder" of the No Touch / AFV Status Page
3. Final .zip file of all gerber and NC drill files which passed DFM, along with your board dimensions.
4. A .zip file of your Altium project. Include only Schematics, Layout, Project file, Schematic and Footprint libraries, and BOM

5.  A short summary of redesign you have made relative to your Experiment 2-4 converter, including calculations justifying the changes (replaces prelab)

Be aware that excessive component cost will not be permissible; new purchases must be justified with analysis showing why the benefits outweigh the additional costs.  Your grade for this lab will be based on the timely completion of an errorless PCB layout which exhibits good layout practices, as discussed in lecture/notes, and proper implementation of system modification as developed in the prelab assignment.