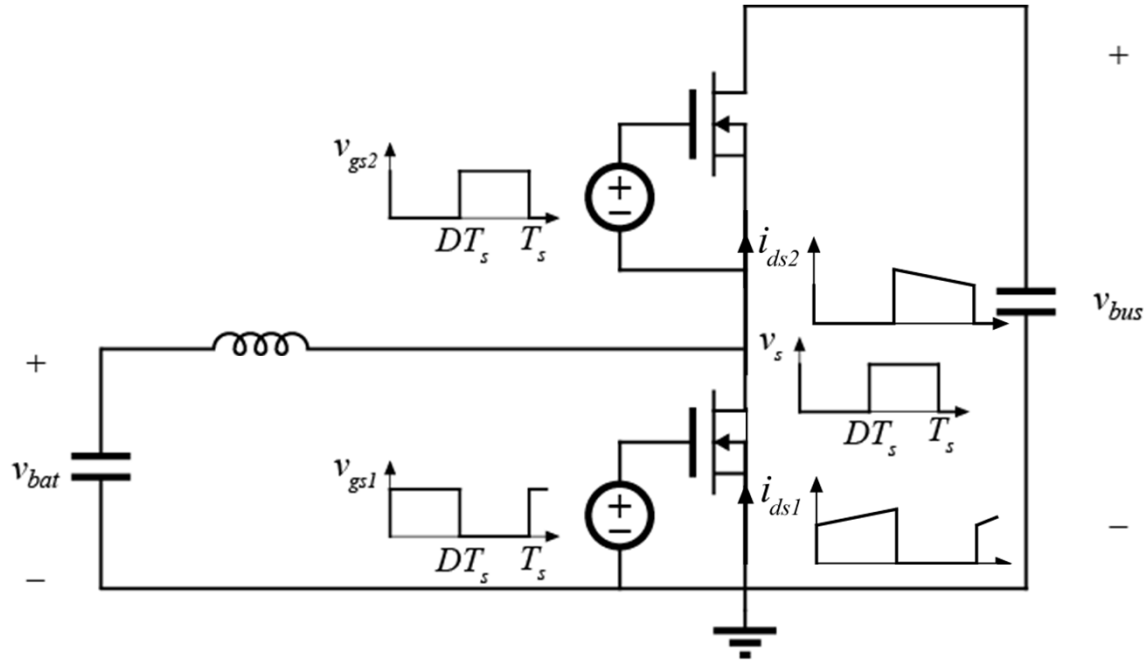
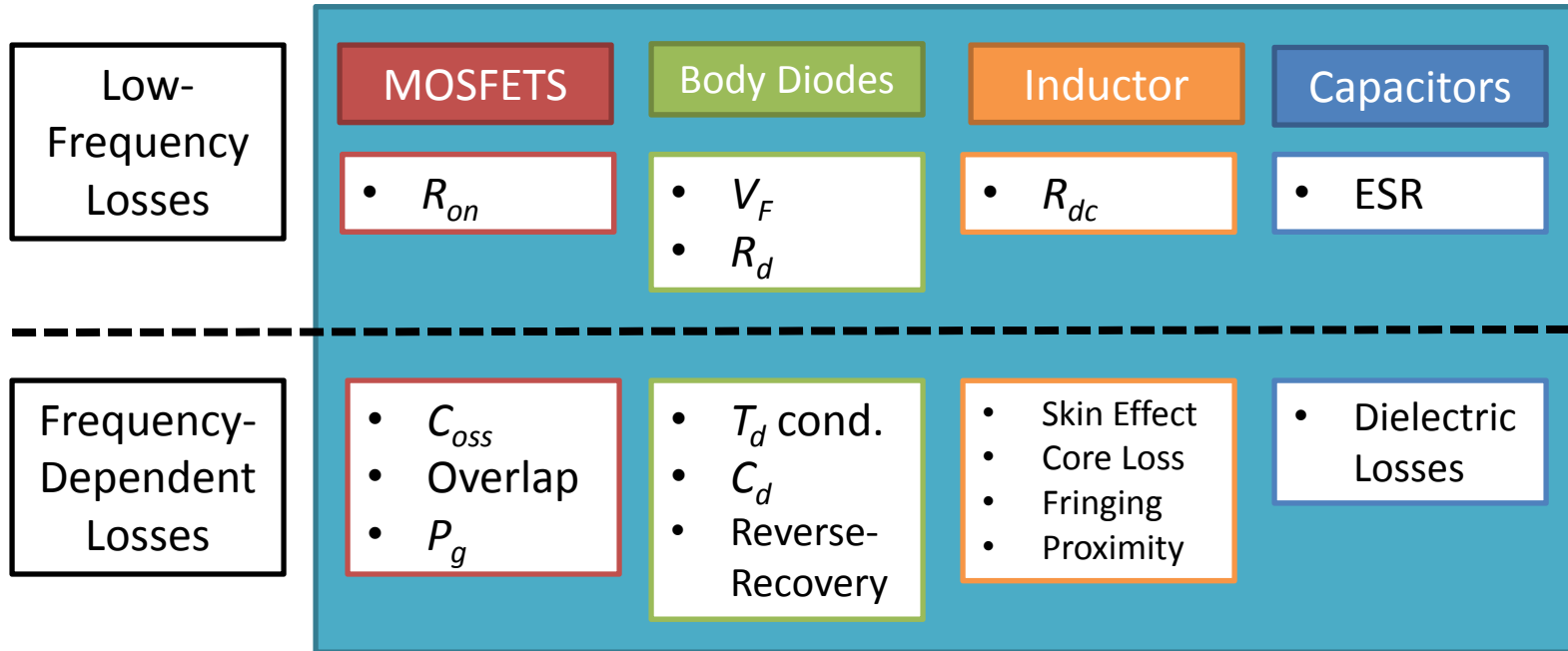


Boost Converter Loss Analysis



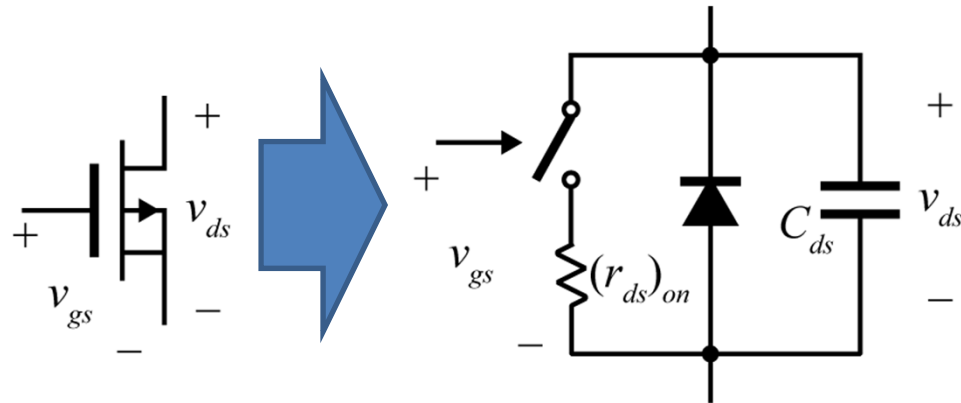
- Begin by solving important waveforms throughout converter assuming lossless operation

Power Stage Losses



LOW FREQUENCY CONDUCTION LOSSES

MOSFET Equivalent Circuit



- Considering only power stage losses (gate drive neglected)
- MOSFET operated as power switch
- Intrinsic body diode behaviors considered using normal diode analysis

Datasheet Interpretation

Drain-source on-state resistance

$R_{DS(on)}$

$V_{GS}=10\text{ V}, I_D=50\text{ A}$

-

16

20

$m\Omega$

$V_{GS}=8\text{ V}, I_D=25\text{ A}$

-

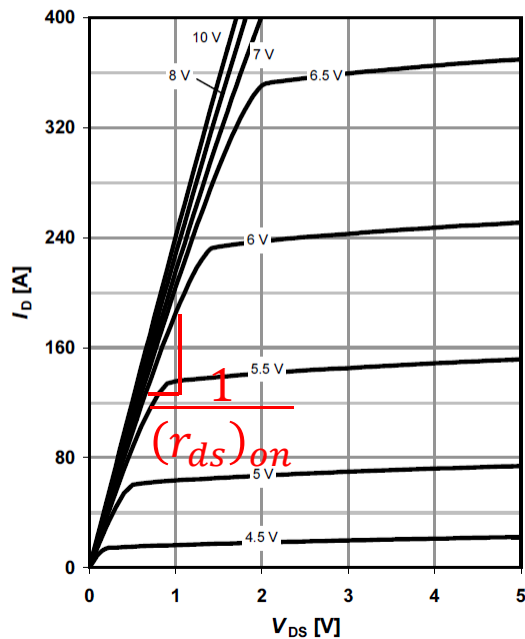
16

20

5 Typ. output characteristics

$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C}$

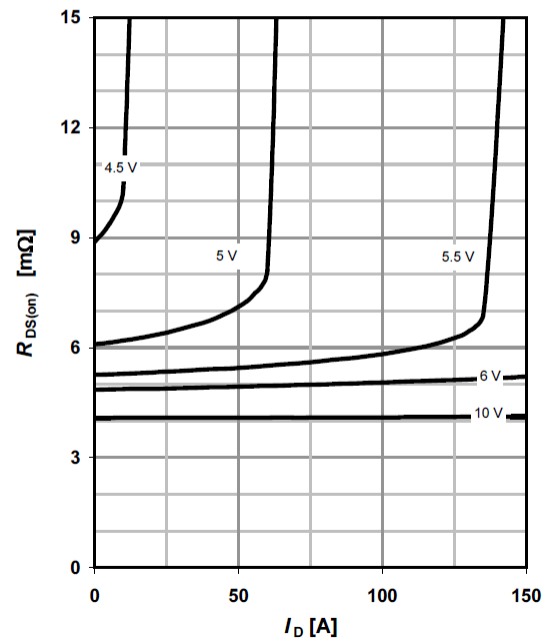
parameter: V_{GS}



6 Typ. drain-source on resistance

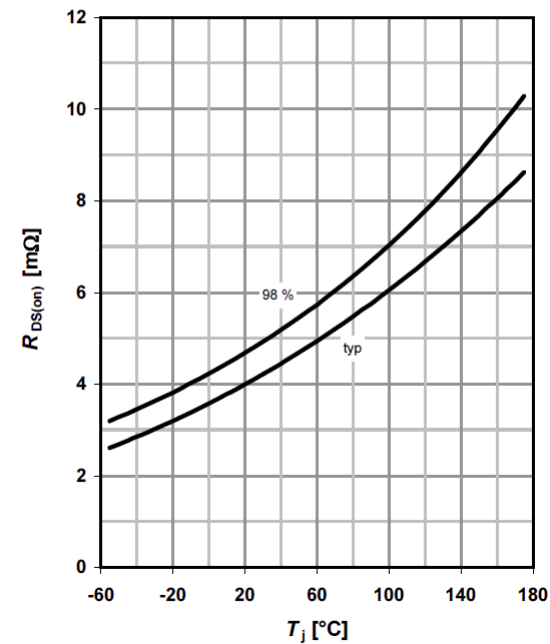
$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C}$

parameter: V_{GS}



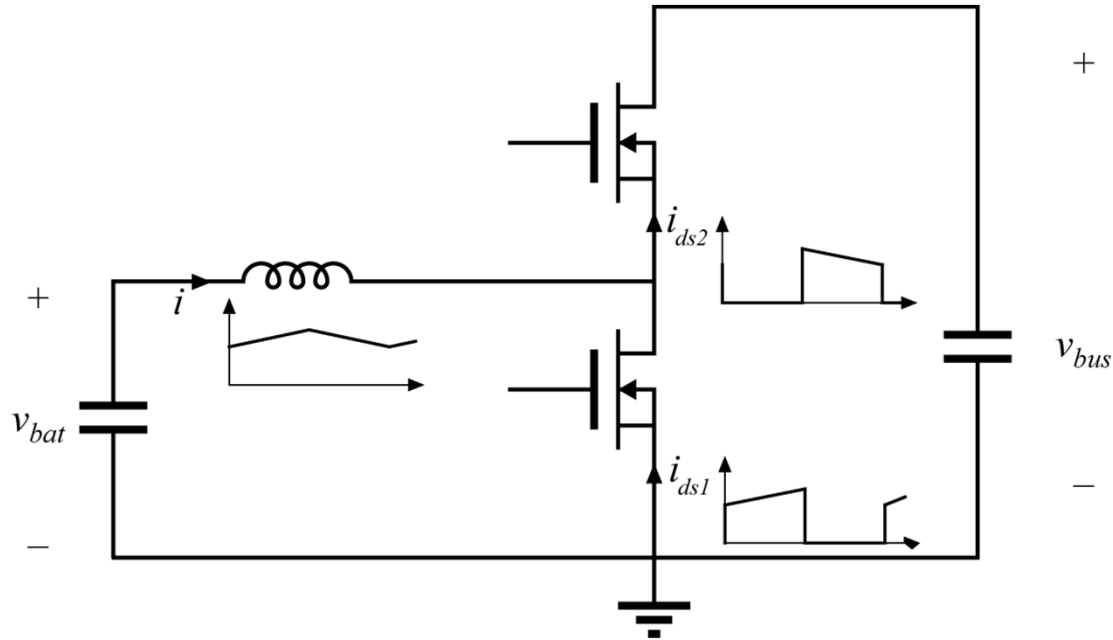
9 Drain-source on-state resistance

$R_{DS(on)}=f(T_j); I_D=100\text{ A}; V_{GS}=10\text{ V}$



- On resistance extracted from datasheet waveforms
- Significantly dependent on V_{gs} amplitude, temperature

Boost Converter RMS Currents



- MOSFET conduction losses due to $(r_{ds})_{on}$ depend given as

$$P_{cond,FET} = I_{di,rms}^2 (r_{ds})_{on}$$

MOSFET Conduction Losses

Pulsating waveform with linear ripple, Fig. A.6:

$$rms = I\sqrt{D} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i}{I}\right)^2} \quad (\text{A.6})$$

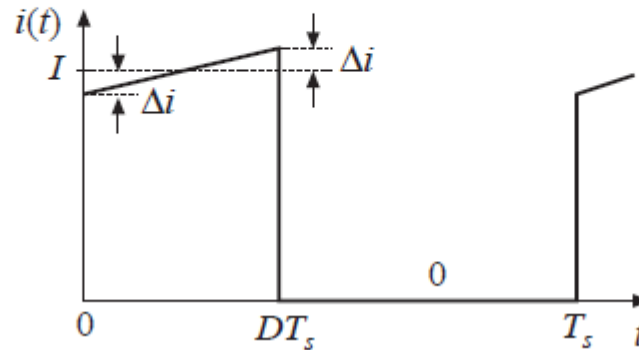
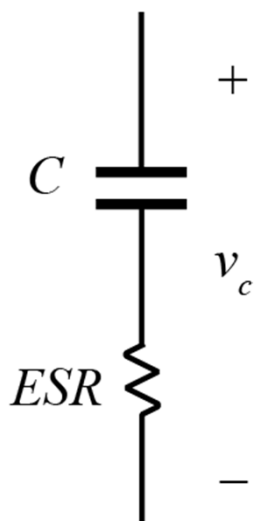


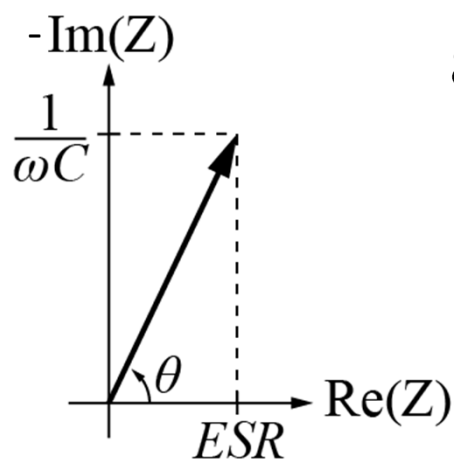
Fig. A.6

- RMS values of commonly observed waveforms appendix from Power Book

Capacitor Loss Model

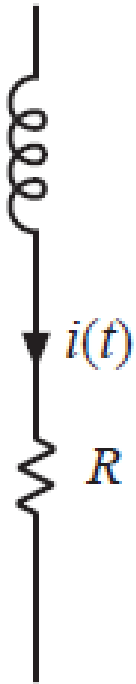


- Operation well below resonance
- All loss mechanisms in a capacitor are generally lumped into an empirical loss model
- Equivalent Series Resistance (ESR) is *highly* frequency dependent
- Datasheets may give effective impedance at a frequency, or loss factor:



$$\delta = \frac{\pi}{2} - \theta$$
$$D = \tan(\delta)$$

DC Inductor Resistance



- DC Resistance given by

$$R_{DC} = \rho \frac{l_b}{A_w}$$

- At room temp, $\rho = 1.724 \cdot 10^{-6} \Omega\text{-cm}$
- At 100°C, $\rho = 2.3 \cdot 10^{-6} \Omega\text{-cm}$
- Losses due to DC current:

$$P_{cu,DC} = I_{L,rms}^2 R_{DC}$$

Inductor Conduction Losses

DC plus linear ripple, Fig. A.2:

$$rms = I \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i}{I} \right)^2} \quad (\text{A.2})$$

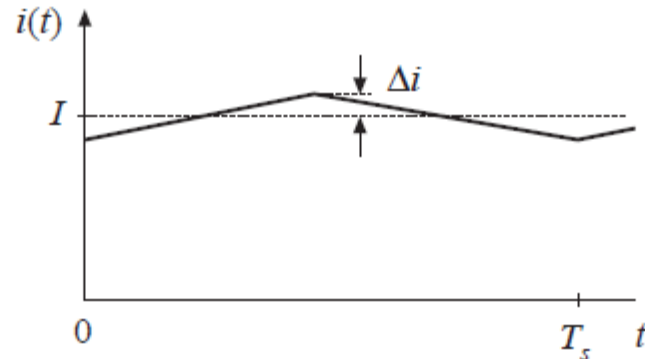
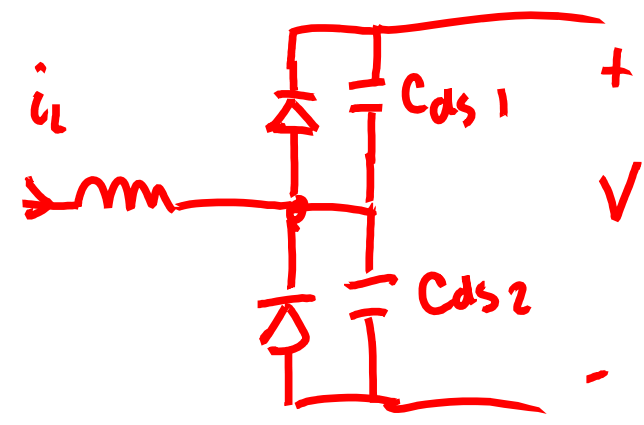
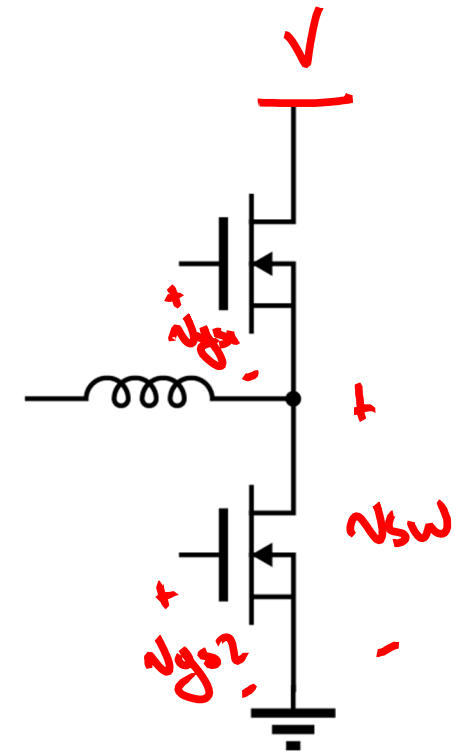
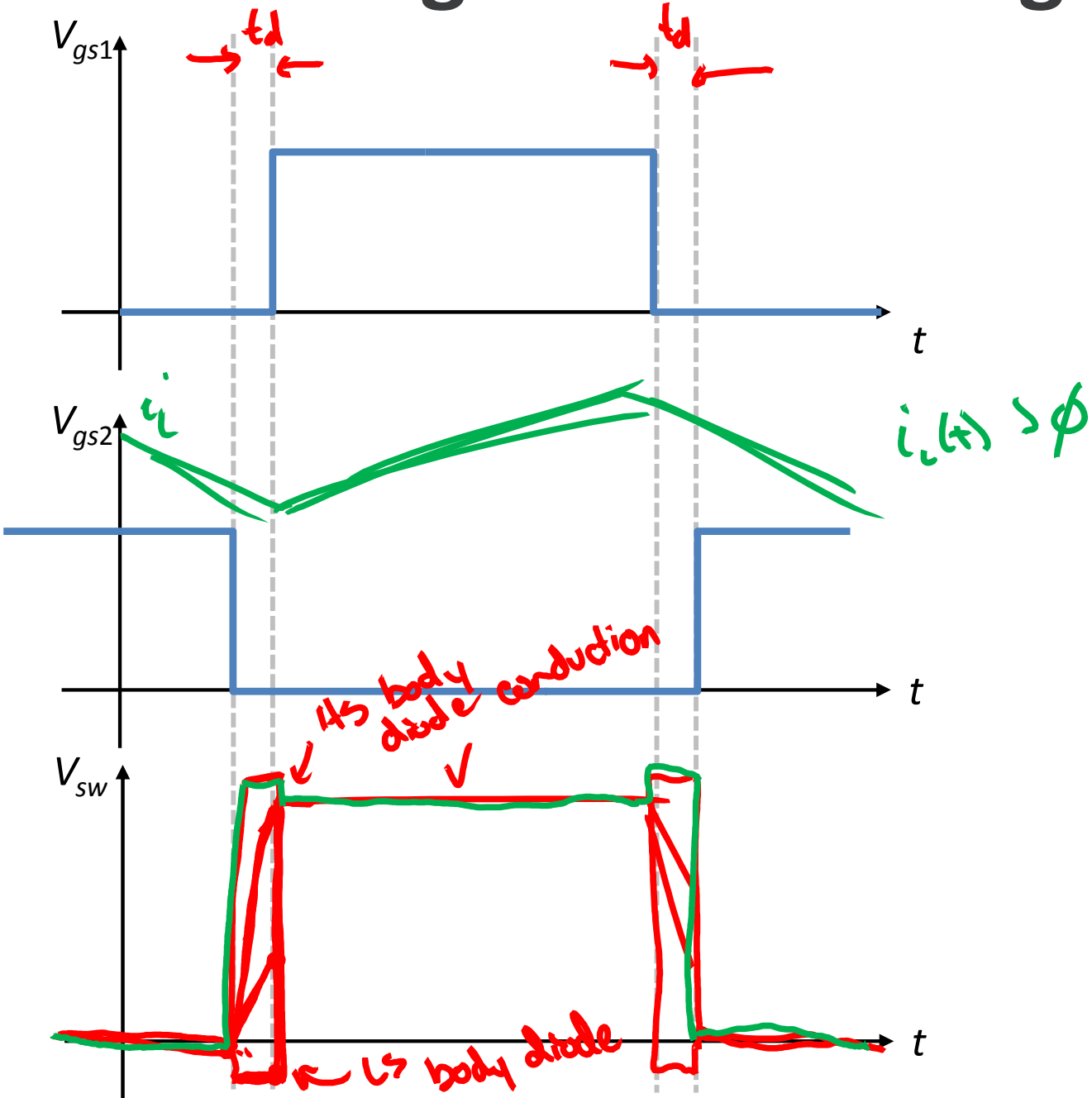


Fig. A.2

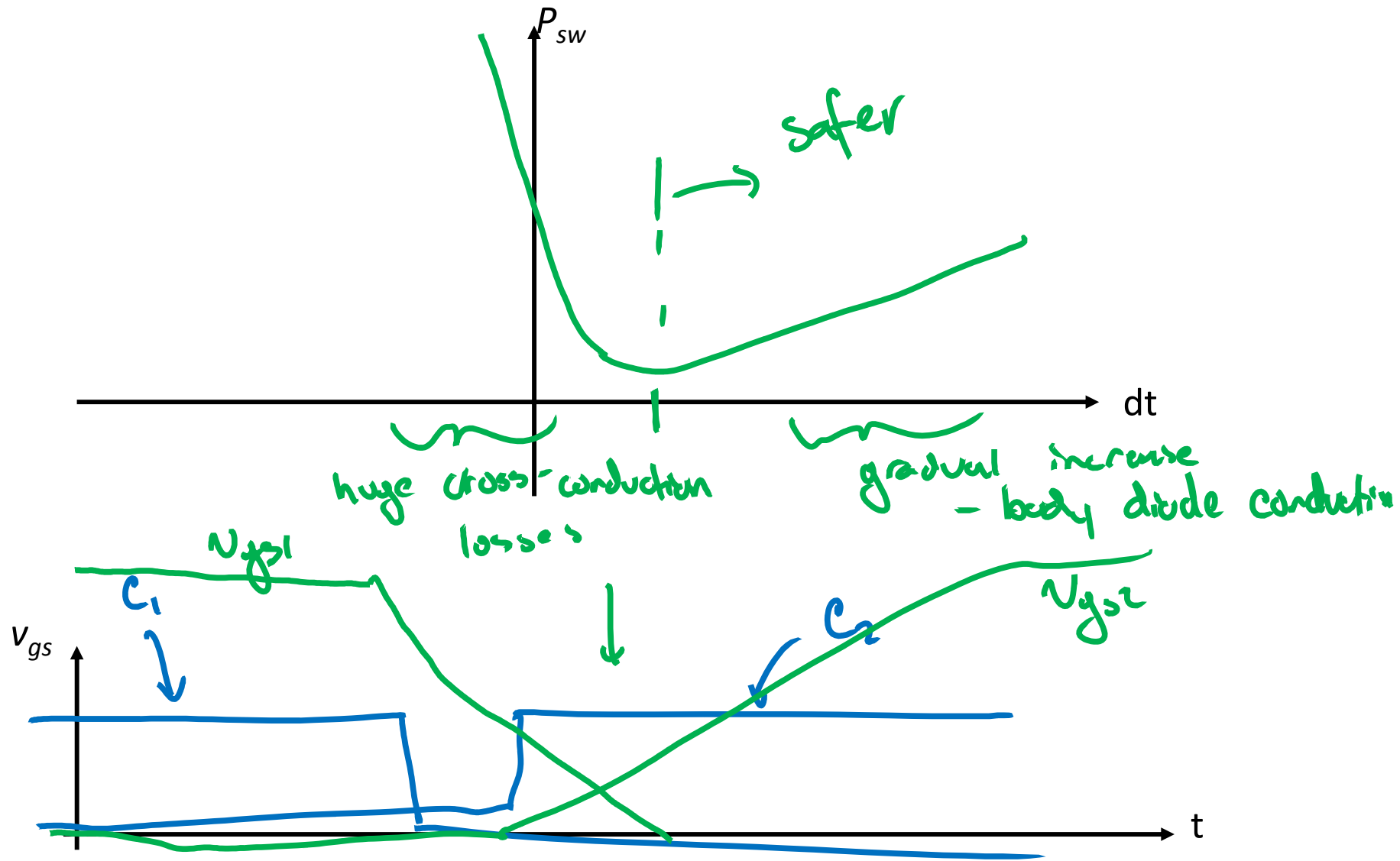
- Conduction losses dependent on RMS current through inductor

Switching Loss

Switching Loss Modeling



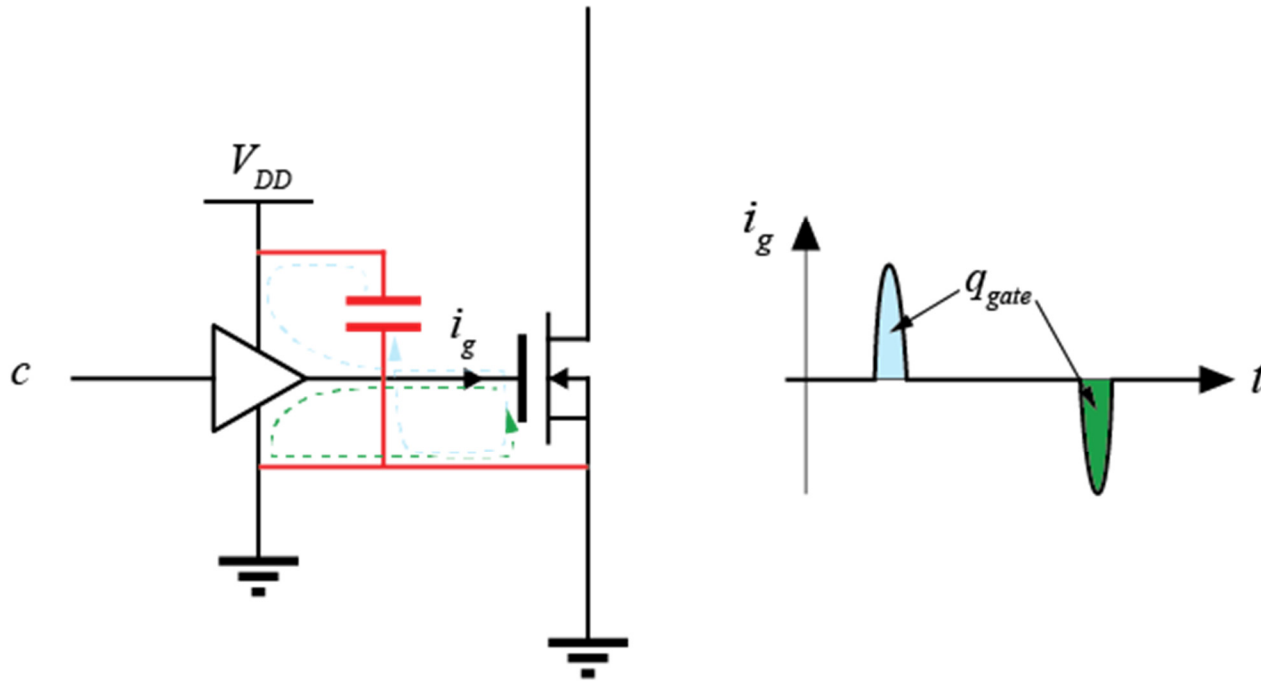
Dead Time Selection



Types of Switching Loss

1. Gate Charge Loss
2. Overlap Loss
3. Capacitive Loss
4. Body Diode Conduction
5. Reverse Recovery
6. Parasitic Inductive Losses
7. Anomalous Losses

Gate Drive Losses



$$E_{loss} = q_{gate} V_{DD}$$

$$P_{sw,g} = E_{loss} f_s$$

comes from V_{DD} .
not from V_g

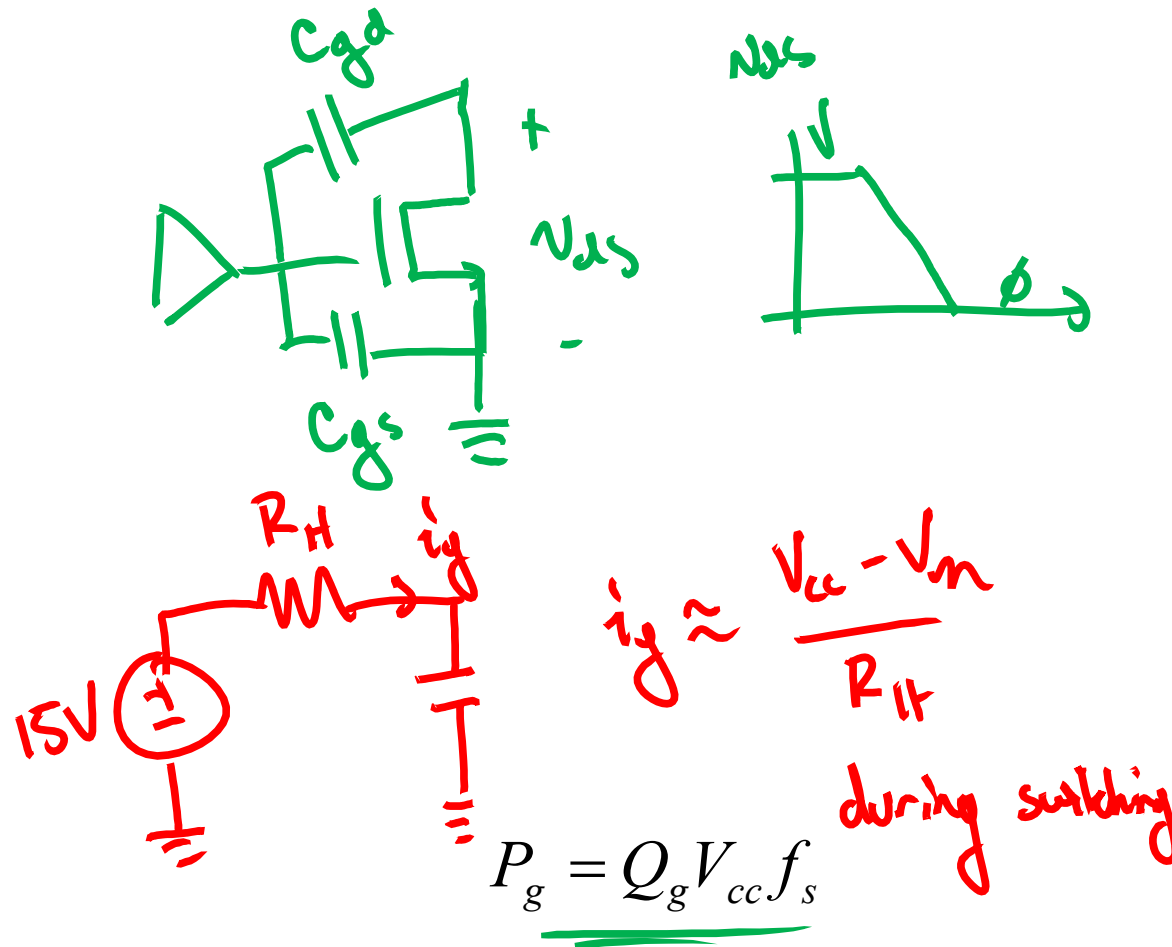
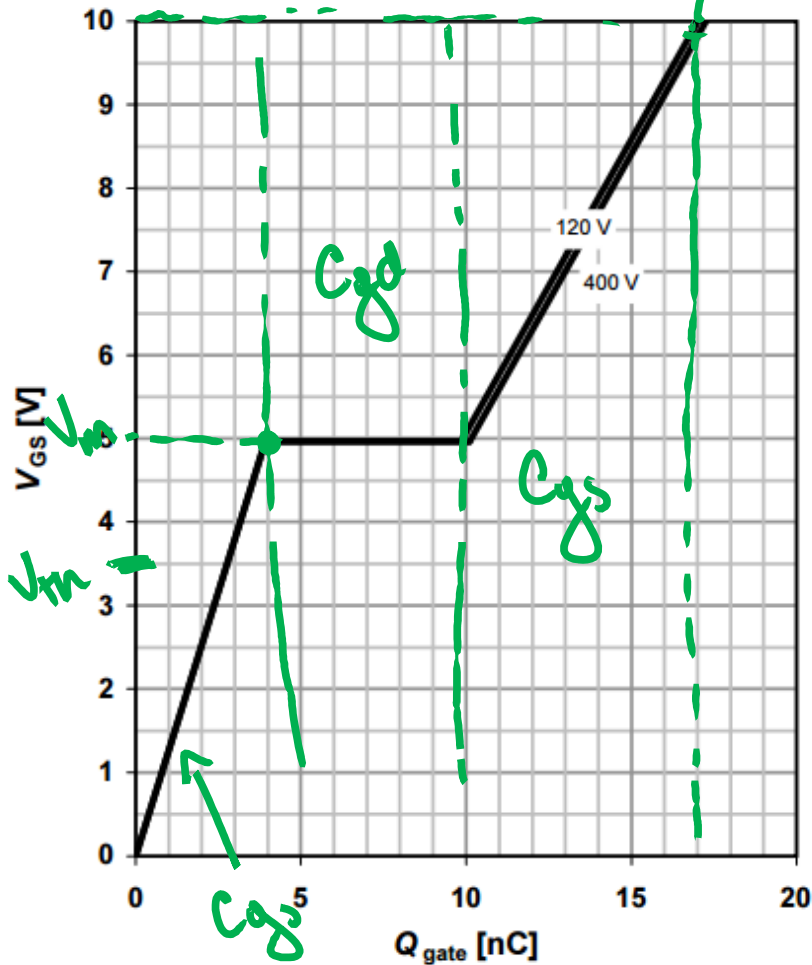
- Gate charge is supplied through driver resistance during switch turn-on
- Gate charge is dissipated in gate driver on switch turn-off

Gate Charge Loss

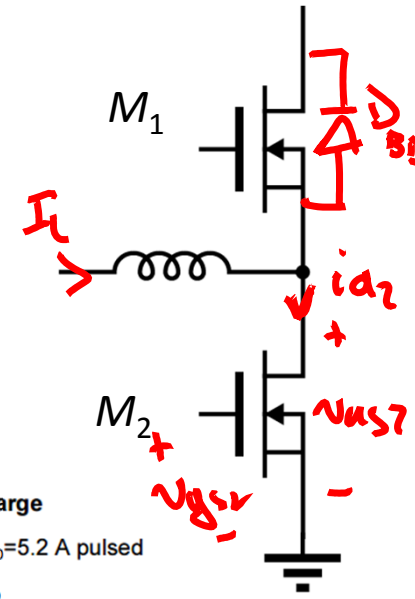
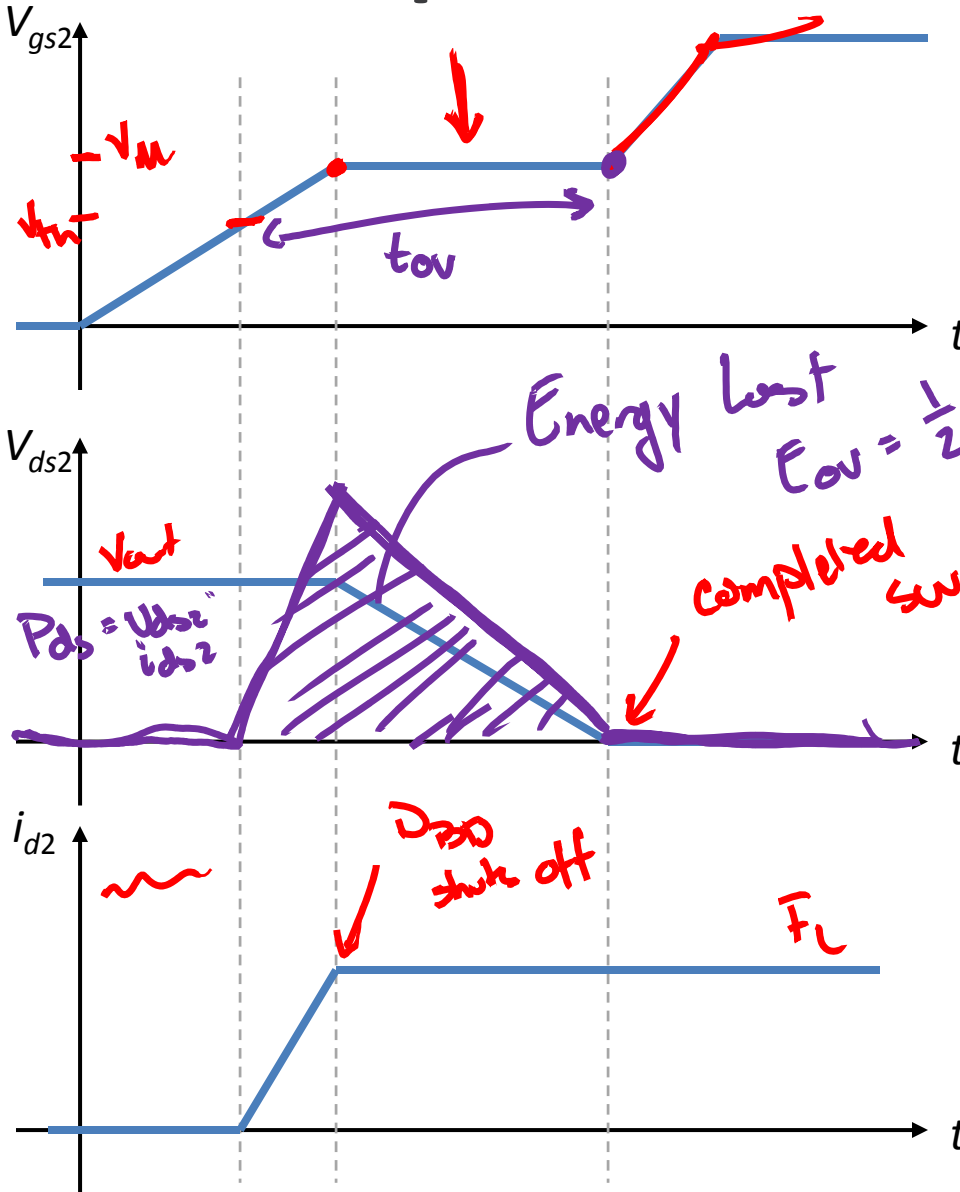
9 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = 5.2 \text{ A pulsed}$

parameter: V_{DD}



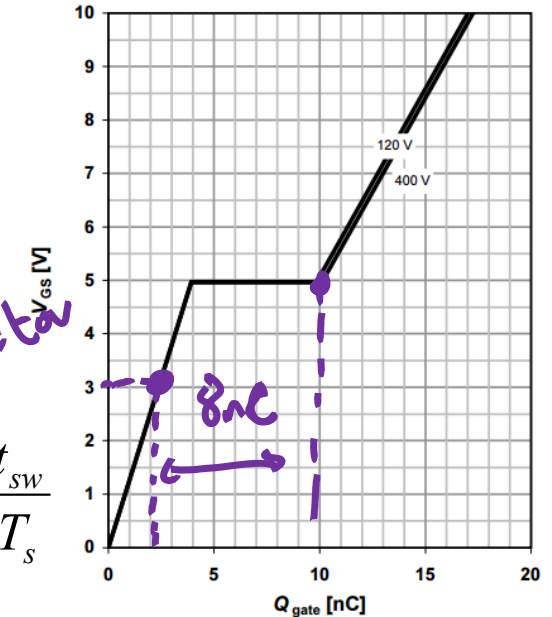
Overlap Loss



9 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 5.2$ A pulsed

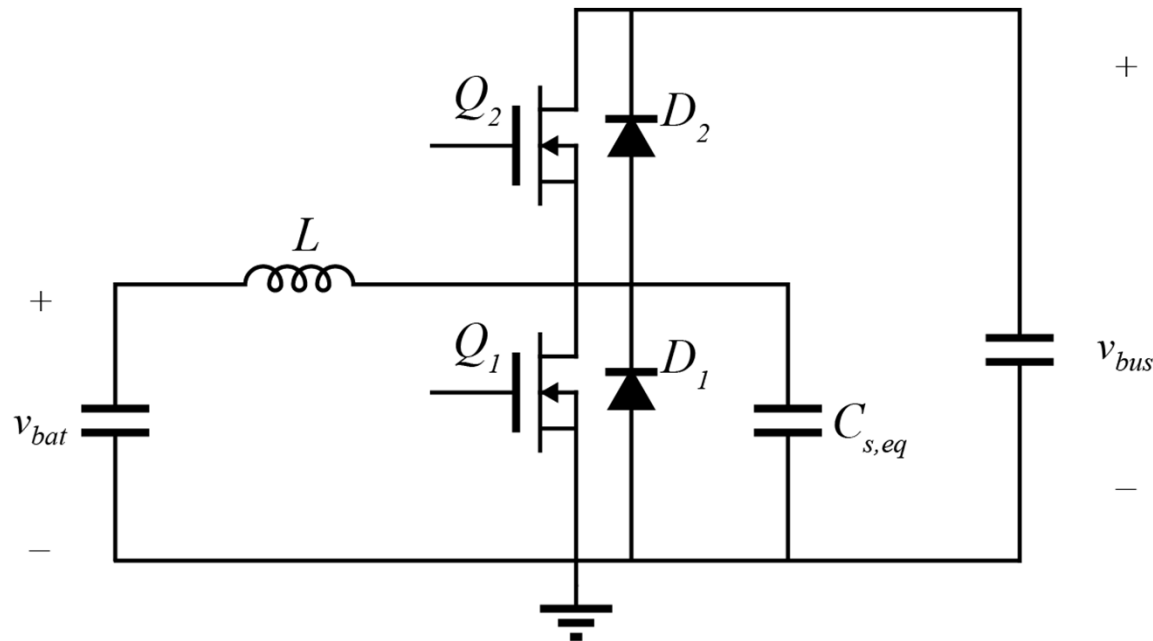
parameter: V_{DD}



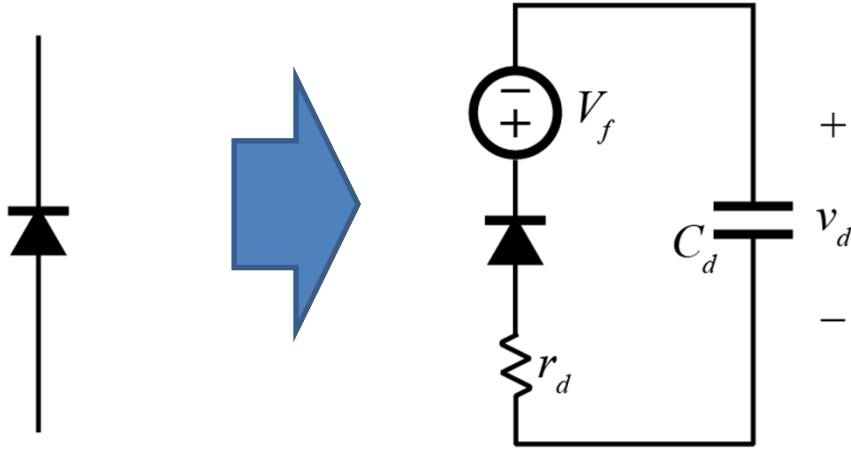
$$P_{overlap} = \frac{1}{2} I_L V \frac{t_{sw}}{T_s}$$

Lump Switched Node Capacitance

- Consider a single equivalent capacitor at switched node which combines energy storage due to all four semiconductor devices



Diode Loss Model



- Example loss model includes resistance and forward voltage drop extracted from datasheet

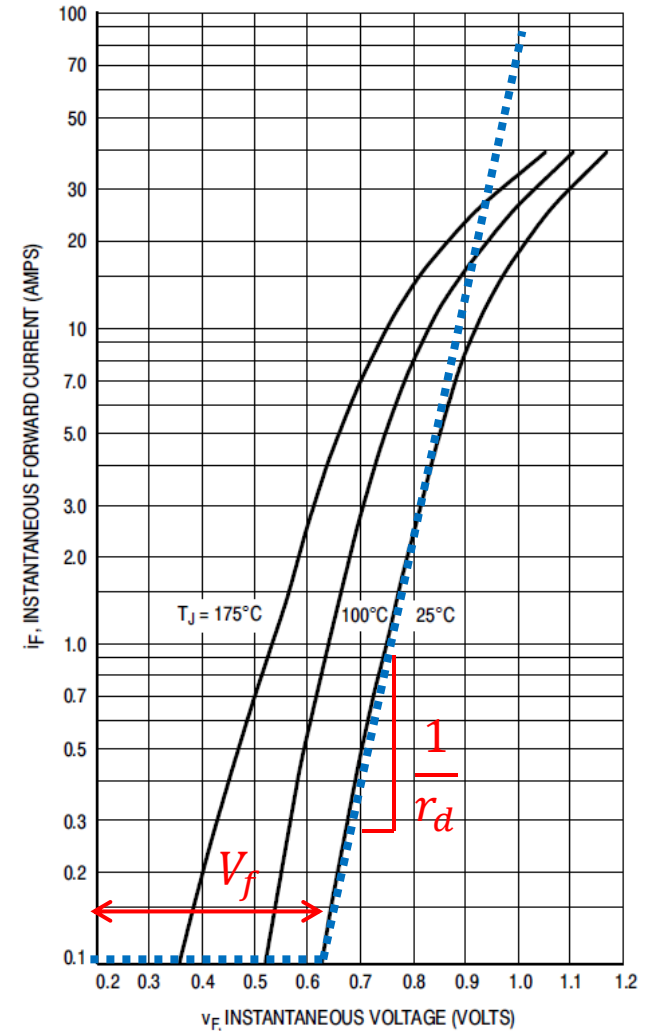
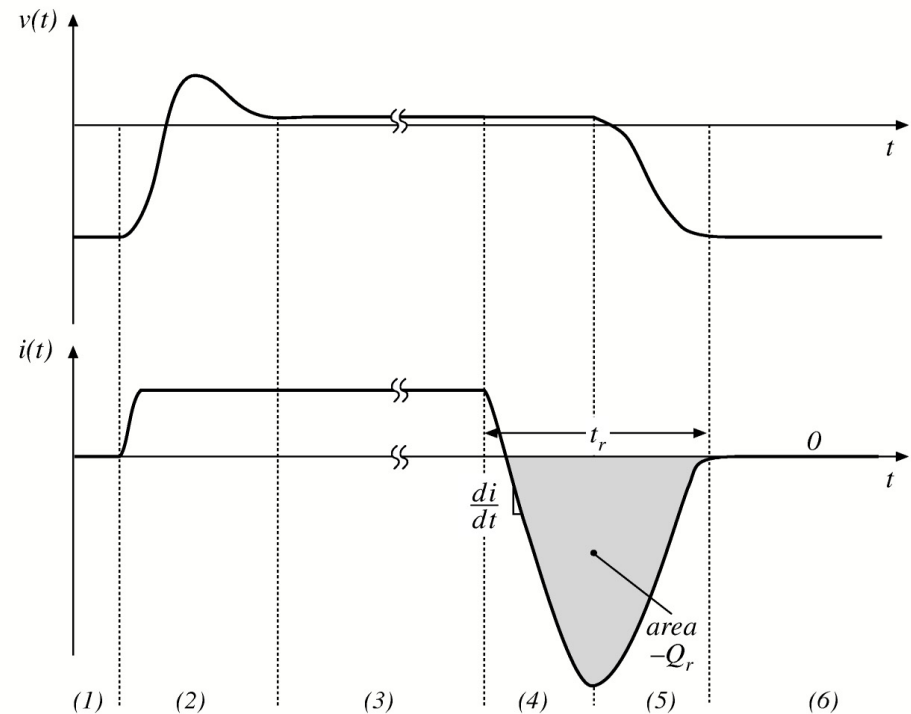


Figure 1. Typical Forward Voltage

Diode Reverse Recovery

- FET body diodes may turn on during dead time intervals
- Significant reverse recovery losses possible



$$E_{on,rr} = ((I_L - \Delta i_L)t_{rr} + Q_{rr})V_{bus}$$

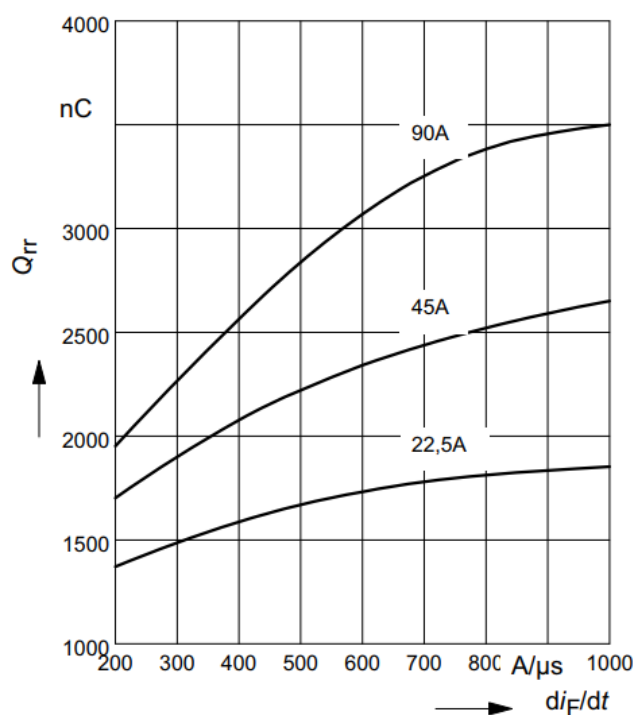
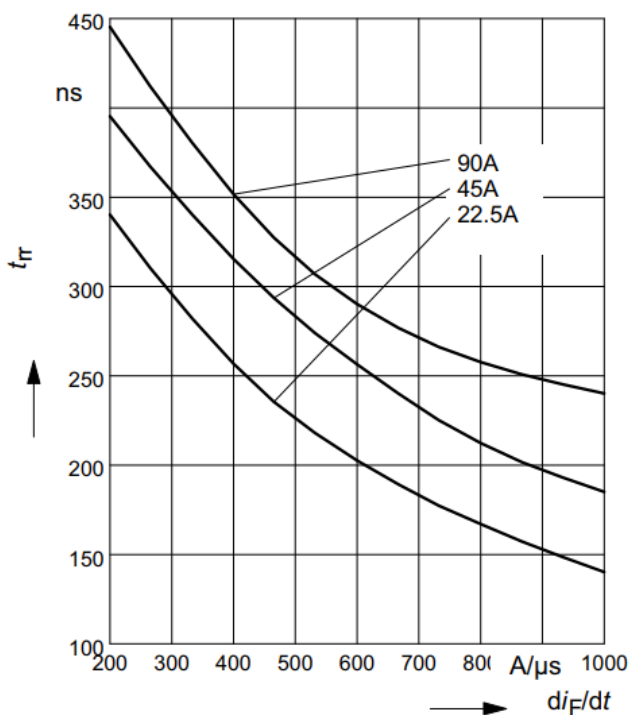
Reverse Recovery - Datasheet

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Dynamic Characteristics					
Reverse recovery time	t_{rr}				ns
$V_R=400V, I_F=45A, di_F/dt=1000A/\mu s, T_j=25^\circ C$		-	140	-	
$V_R=400V, I_F=45A, di_F/dt=1000A/\mu s, T_j=125^\circ C$		-	185	-	
$V_R=400V, I_F=45A, di_F/dt=1000A/\mu s, T_j=150^\circ C$		-	195	-	
Reverse recovery charge	Q_{rr}				nC
$V_R=400V, I_F=45A, di_F/dt=1000A/\mu s, T_j=25^\circ C$		-	1400	-	
$V_R=400V, I_F=45A, di_F/dt=1000A/\mu s, T_j=125^\circ C$		-	2650	-	
$V_R=400V, I_F=45A, di_F/dt=1000A/\mu s, T_j=150^\circ C$		-	2900	-	

5 Typ. reverse recovery time

$$t_{rr} = f(di_F/dt)$$

parameter: $V_R = 400V, T_j = 125^\circ C$



Reverse Recovery – Rough Approximations

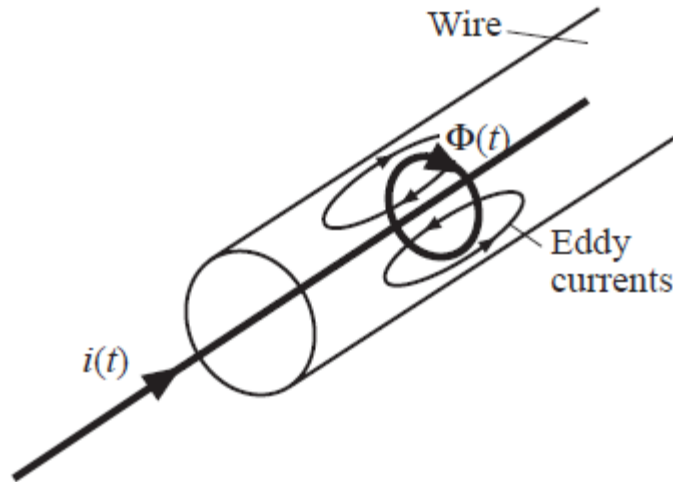
- $E_{rr} \approx E_{rr_datasheet} \frac{I_F}{I_{F_datasheet}} \frac{V_{DC}}{V_{DC_datasheet}}$
- **Rough** approximation with $I_F \ll I_{max}$



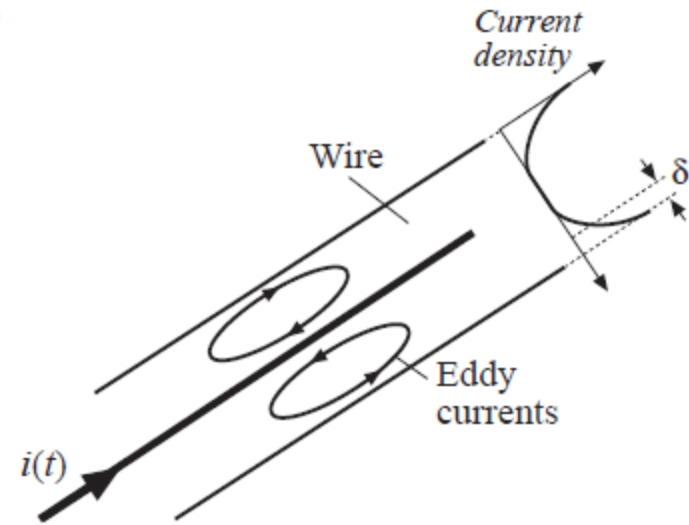
INDUCTOR AC LOSSES

Skin Effect in Copper Wire

(a)

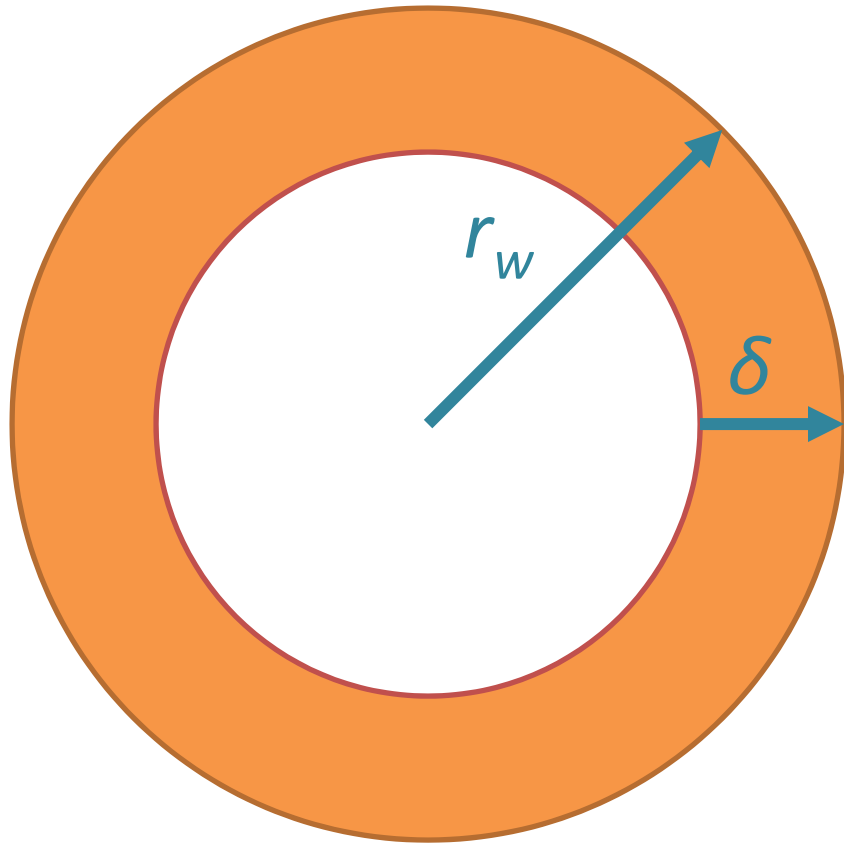


(b)



- Current profile at high frequency is exponential function of distance from center with characteristic length δ

AC Resistance



$$A_{w,eff} = \pi r_w^2 - \pi (r_w - \delta)^2$$

$$R_{ac} = \rho \frac{l_b}{A_{w,eff}}$$

Skin Depth

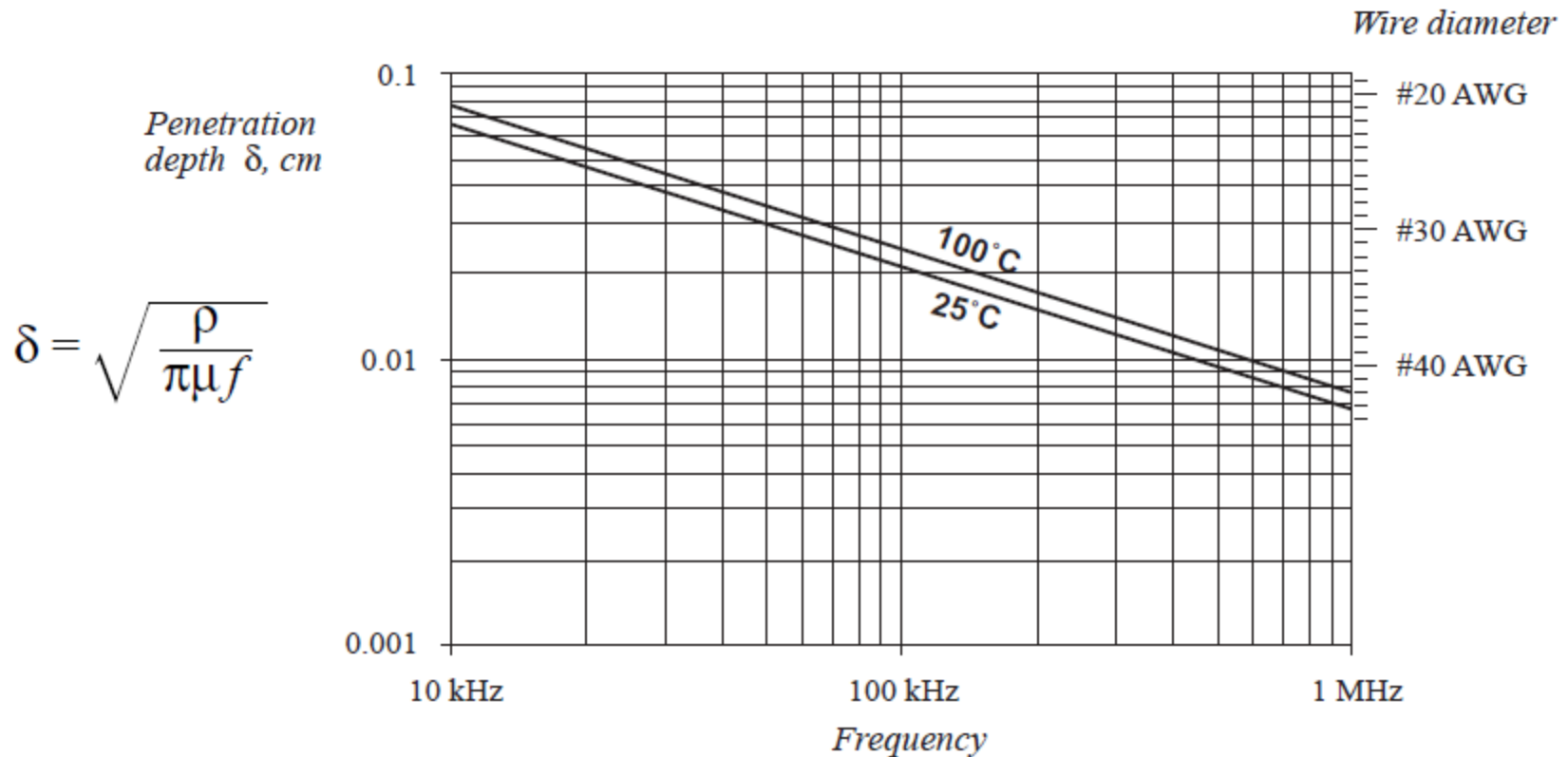
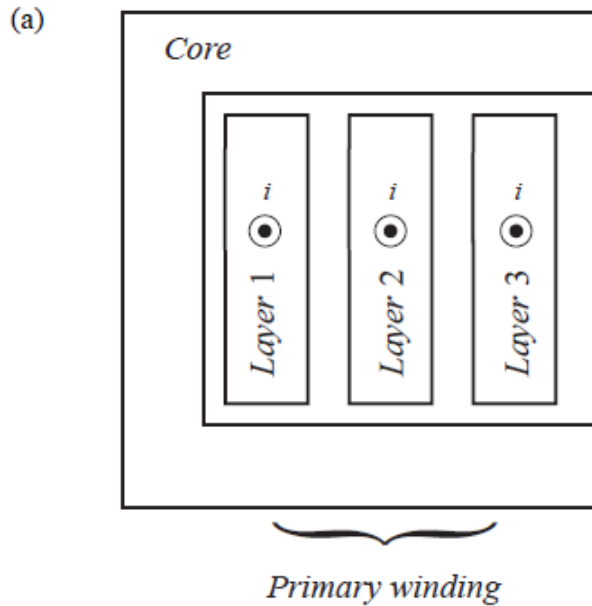


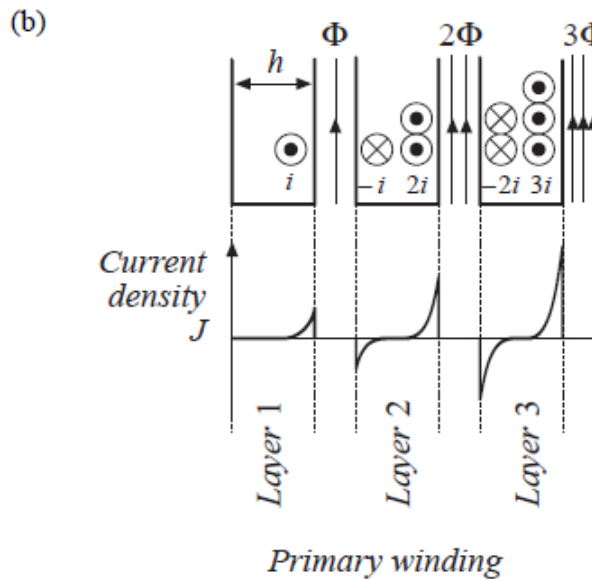
Fig. 13.23 Penetration depth δ , as a function of frequency f , for copper wire.



Proximity Effect

- In *foil* conductor closely spaced with $h \gg \delta$, flux between layers generates additional current according to Lenz's law.

$$P_1 = I_{L,rms}^2 R_{ac}$$



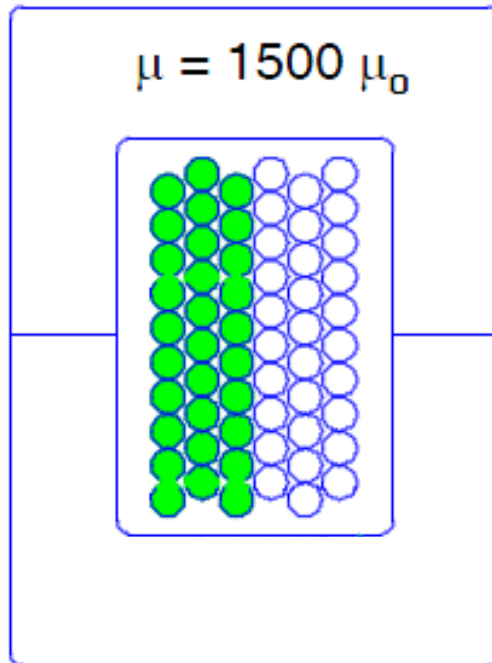
- Power loss in layer 2:

$$P_2 = I_{L,rms}^2 R_{ac} + (2I_{L,rms})^2 R_{ac}$$

$$P_2 = 5P_1$$

- Needs modification for non-foil conductors

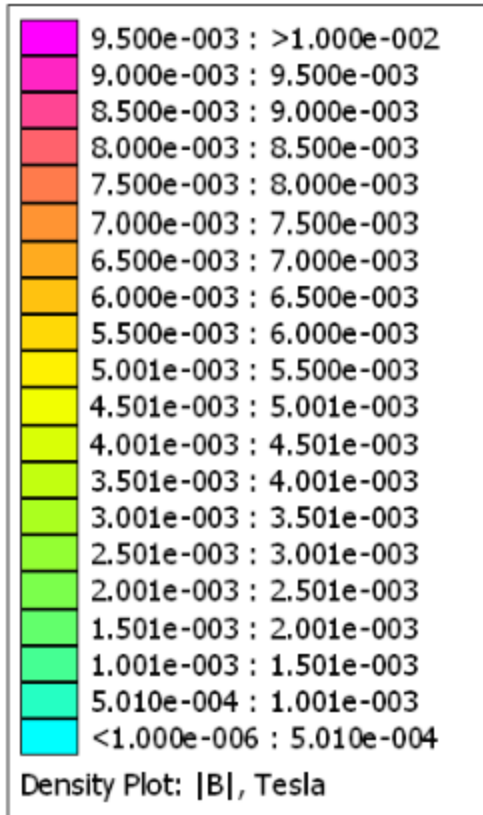
Simulation Example



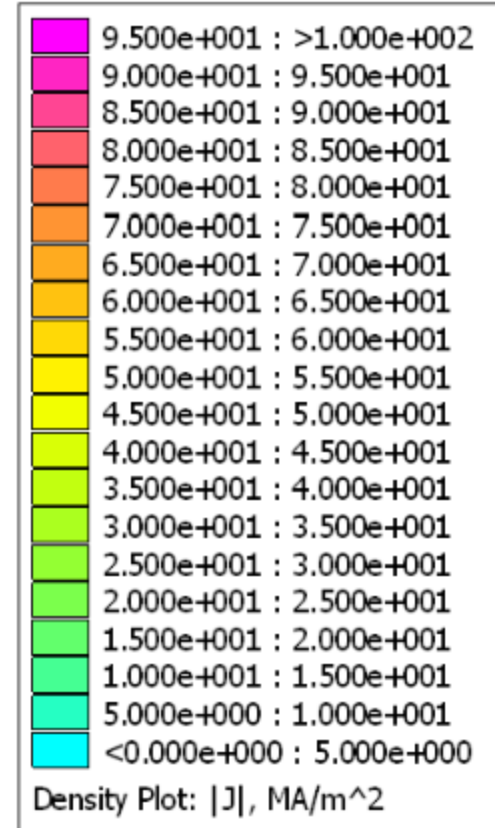
- AWG#30 copper wire
 - Diameter $d = 0.294$ mm
 - $d = \delta$ at around 50 kHz
- 1:1 transformer
 - Primary and secondary are the same, 30 turns in 3 layers
- Sinusoidal currents,
 $I_{1rms} = I_{2rms} = 1$ A

Numerical field and current density solutions using FEMM (Finite Element Method Magnetics), a free 2D solver, <http://www.femm.info/wiki/HomePage>

Flux density magnitude

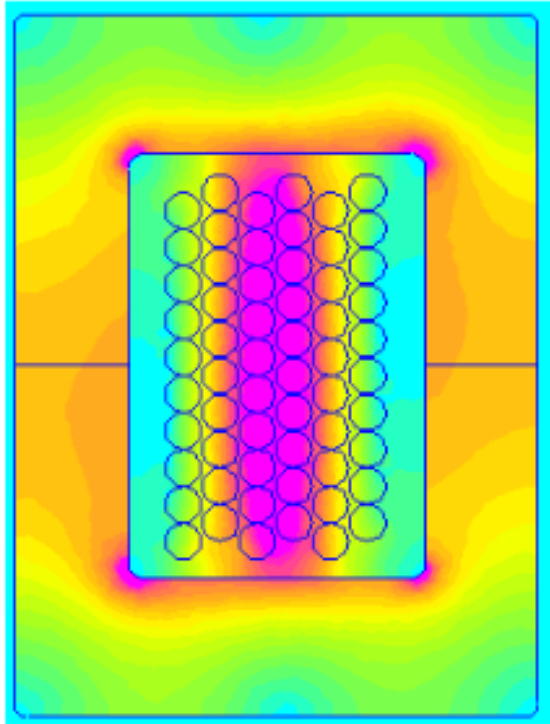


Current density magnitude

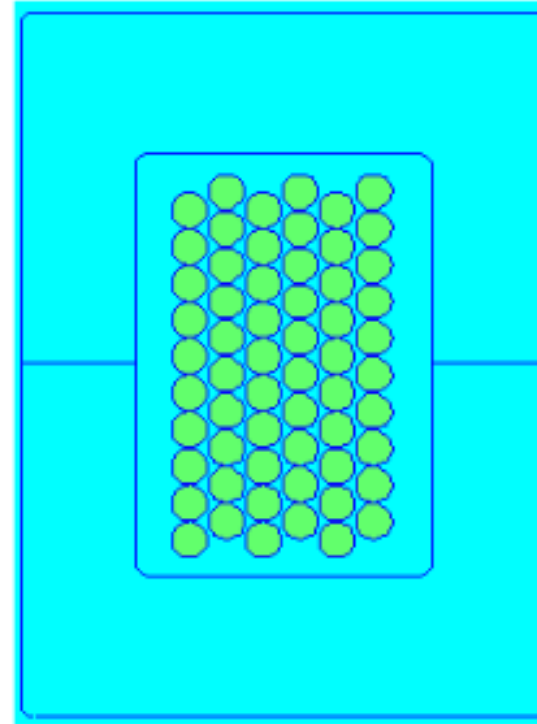


Frequency: 1 kHz

Flux density

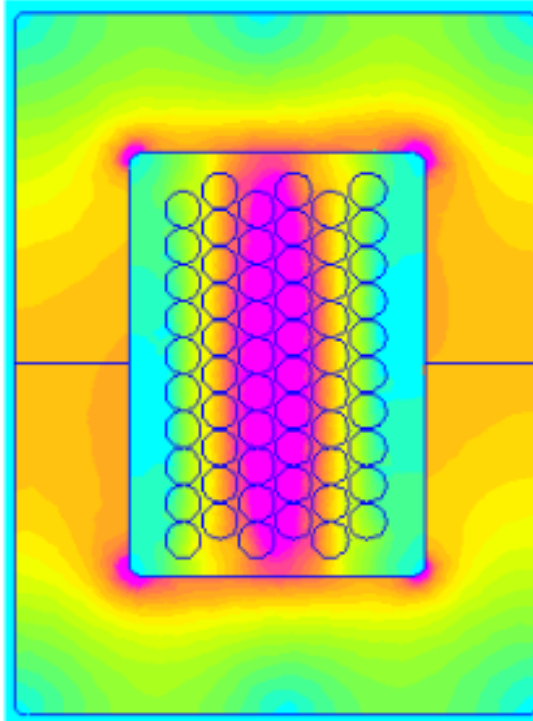


Current Density

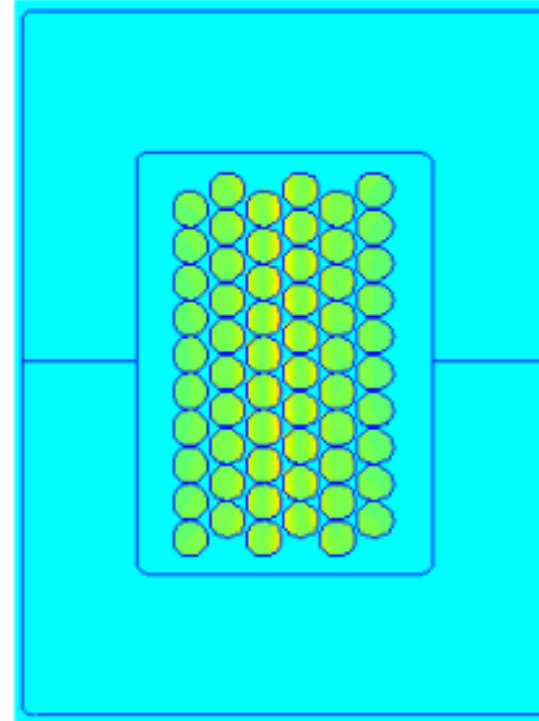


Frequency: 100 kHz

Flux density



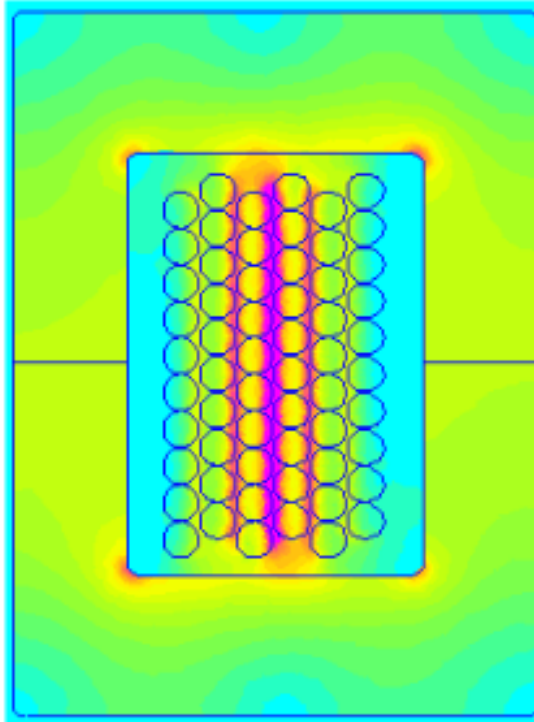
Current Density



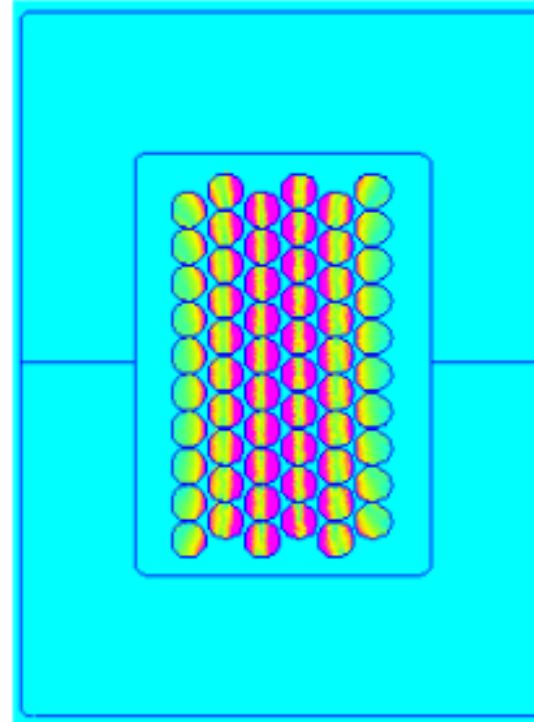
Total copper losses 1.8 larger than at 1 kHz

Frequency: 1 MHz

Flux density



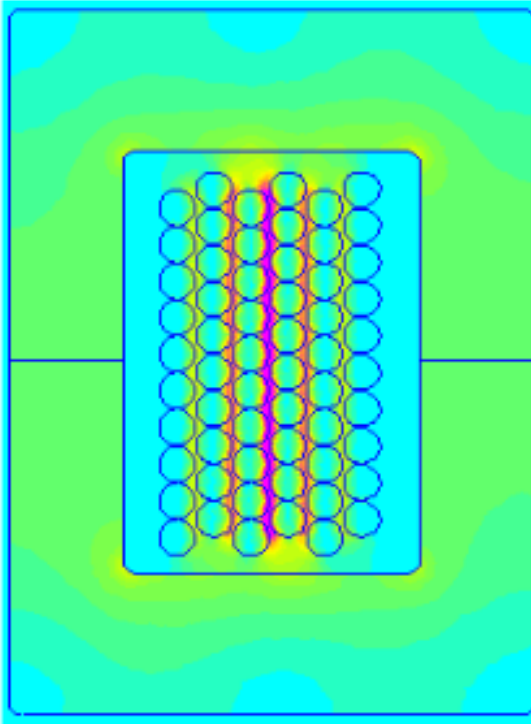
Current Density



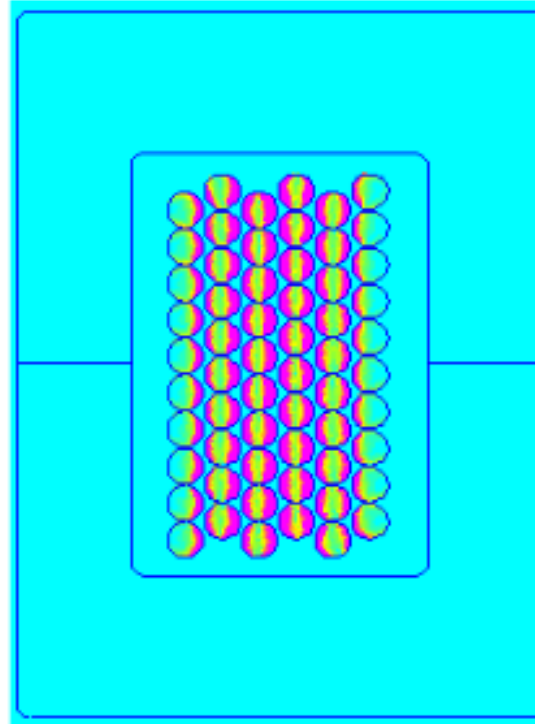
Total copper losses 20 times larger than at 1 kHz

Frequency: 10 MHz

Flux density

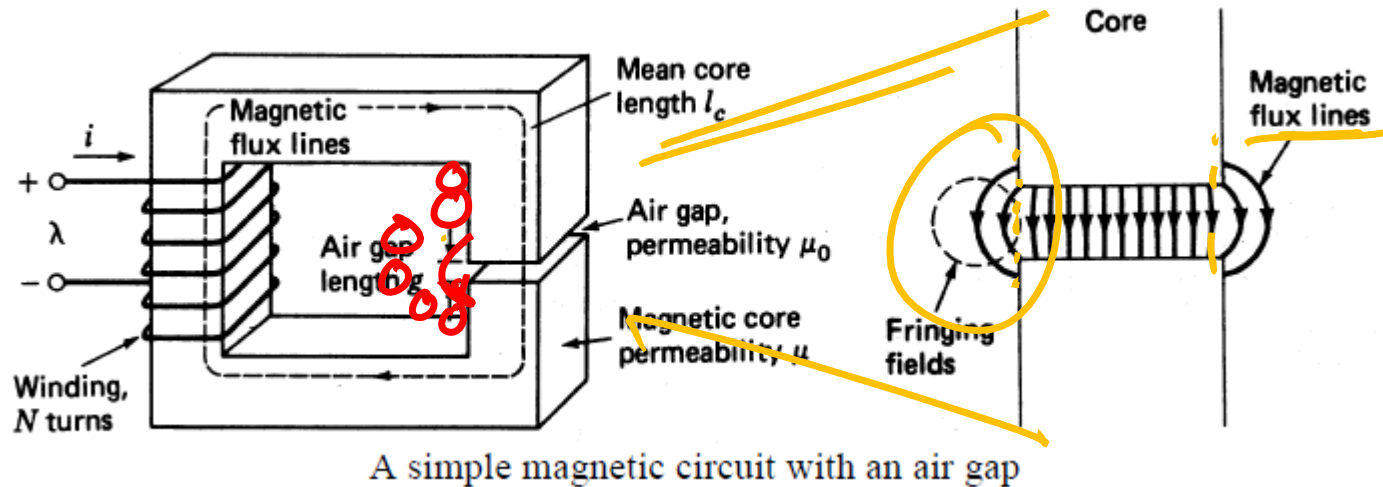


Current Density



Very significant proximity effect
Total copper losses = 65 times larger than at 1 KHz

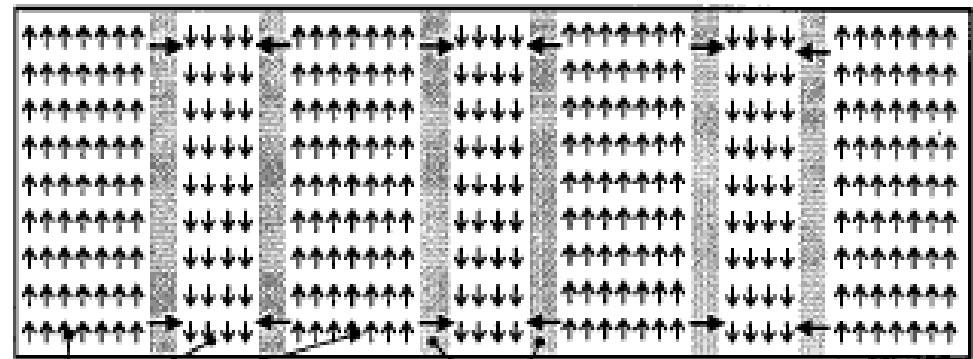
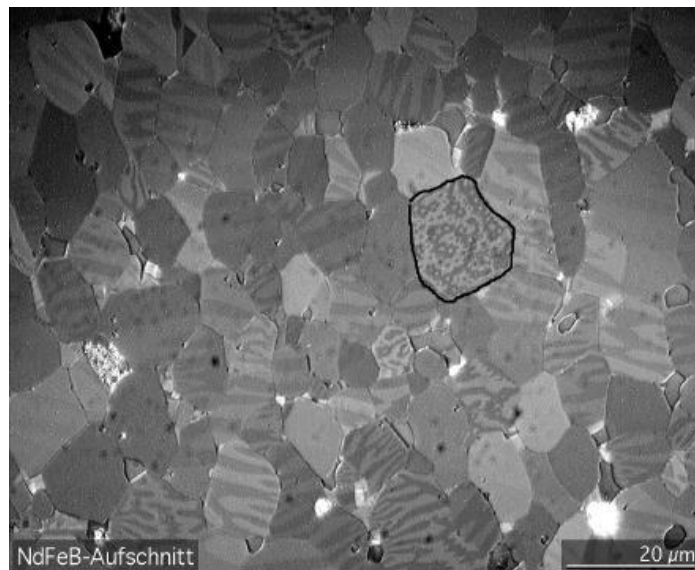
Fringing



- Near air gap, flux may bow out significantly, causing additional eddy current losses in nearby conductors

Physical Origin of Core Loss

- Magnetic material is divided into “domains” of saturated material
- Both Hysteresis and Eddy Current losses occur from domain wall shifting



Domains

Domain walls

Direction of magnetization in saturated domains: ↑↑↑↑ ↓↓↓↓

Direction of domain wall movement: →

Inductor Core Loss

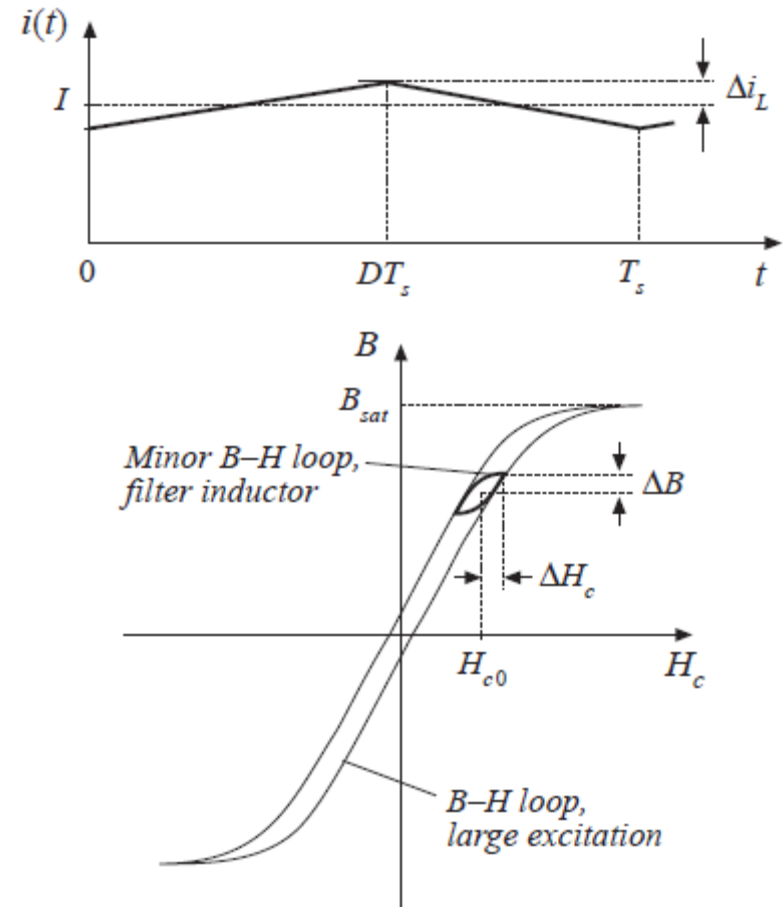
- Governed by Steinmetz Equation:

$$P_v = K_{fe} f_s^\alpha (\Delta B)^\beta \quad [\text{mW/cm}^3]$$

- Parameters K_{fe} , α , and β extracted from manufacturer data

$$P_{fe} = P_v A_c l_m \quad [\text{mW}]$$

- $\Delta B \propto \Delta i_L \rightarrow$ small losses with small ripple



Steinmetz Parameter Extraction

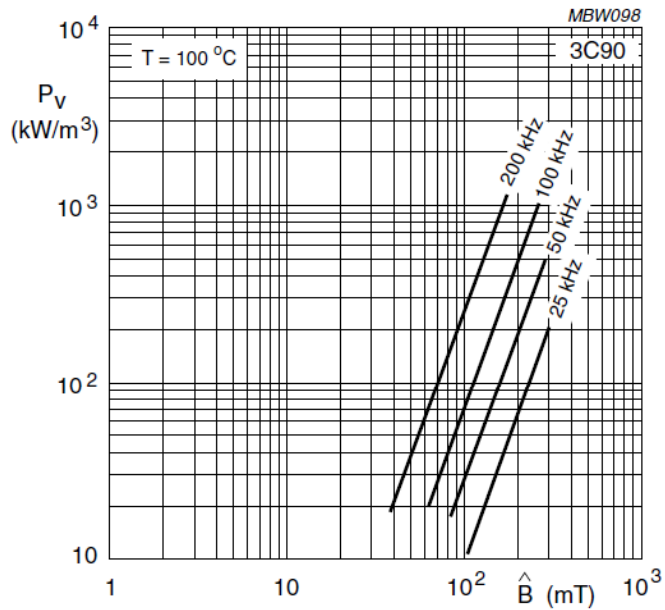


Fig.6 Specific power loss as a function of peak flux density with frequency as a parameter.

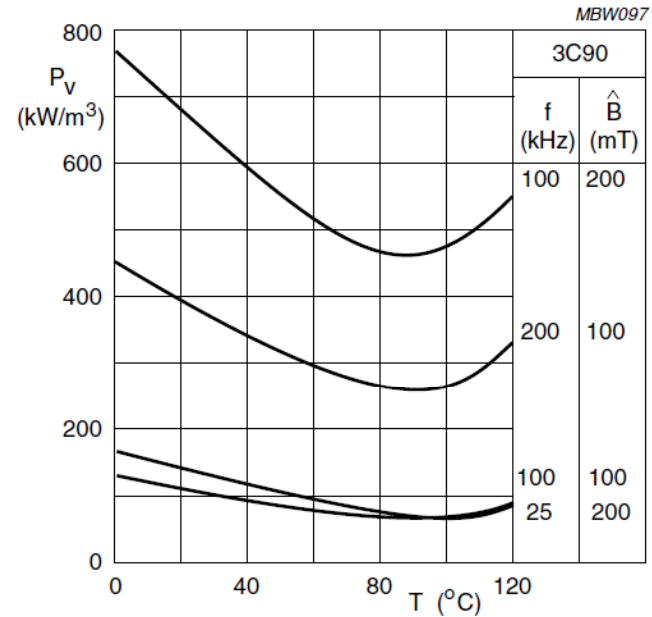


Fig.7 Specific power loss for several frequency/flux density combinations as a function of temperature.

Ferroxcube Curve Fit Parameters

Power losses in our ferrites have been measured as a function of frequency (f in Hz), peak flux density (B in T) and temperature (T in °C). Core loss density can be approximated ⁽²⁾ by the following formula :

$$P_{\text{core}} = C_m \cdot f^x \cdot B_{\text{peak}}^y (ct_0 - ct_1 T + ct_2 T^2) \quad [3]$$

$$= C_m \cdot C_T \cdot f^x \cdot B_{\text{peak}}^y \quad [\text{mW/cm}^3]$$

ferrite	f (kHz)	Cm	x	y	ct ₂	ct ₁	ct ₀
3C30	20-100	7.13.10 ⁻³	1.42	3.02	3.65.10 ⁻⁴	6.65.10 ⁻²	4
	100-200	7.13.10 ⁻³	1.42	3.02	4.10 ⁻⁴	6.8 .10 ⁻²	3.8
3C90	20-200	3.2.10 ⁻³	1.46	2.75	1.65.10 ⁻⁴	3.1.10 ⁻²	2.45
3C94	20-200	2.37.10 ⁻³	1.46	2.75	1.65.10 ⁻⁴	3.1.10 ⁻²	2.45
	200-400	2.10 ⁻⁹	2.6	2.75	1.65.10 ⁻⁴	3.1.10 ⁻²	2.45
3F3	100-300	0.25.10 ⁻³	1.63	2.45	0.79.10 ⁻⁴	1.05.10 ⁻²	1.26
	300-500	2.10 ⁻⁵	1.8	2.5	0.77.10 ⁻⁴	1.05.10 ⁻²	1.28
	500-1000	3.6.10 ⁻⁹	2.4	2.25	0.67.10 ⁻⁴	0.81.10 ⁻²	1.14
3F4	500-1000	12.10 ⁻⁴	1.75	2.9	0.95.10 ⁻⁴	1.1.10 ⁻²	1.15
	1000-3000	1.1.10 ⁻¹¹	2.8	2.4	0.34.10 ⁻⁴	0.01.10 ⁻²	0.67

Table 1: Fit parameters to calculate the power loss density

NSE/iGSE

$$P_{NSE} = \left(\frac{\Delta B}{2}\right)^{\beta-\alpha} \frac{k_N}{T} \int_0^T \left|\frac{dB}{dt}\right|^\alpha dt$$

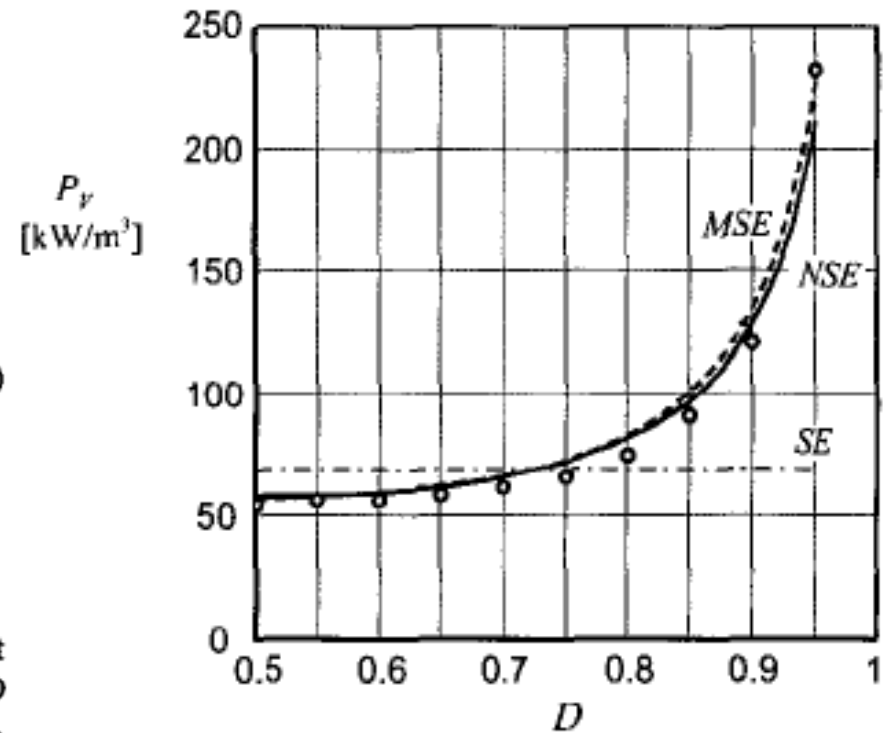
$$k_N = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^\alpha d\theta}$$

Simple Formula for Square-wave voltages:

$$P_{NSE} = k_N (2f)^\alpha (\Delta B)^\beta (D^{1-\alpha} + (1-D)^{1-\alpha}) \quad (10)$$

where f is the operating frequency;
 $\Delta B / 2$ is the peak induction;
 D is the duty ratio of the square wave voltage.

Note: The second and third harmonics are dominant at moderate values of duty ratio D . For extreme values of D (95%), a higher value of α could give better matching to the actual losses.



INDUCTOR DESIGN

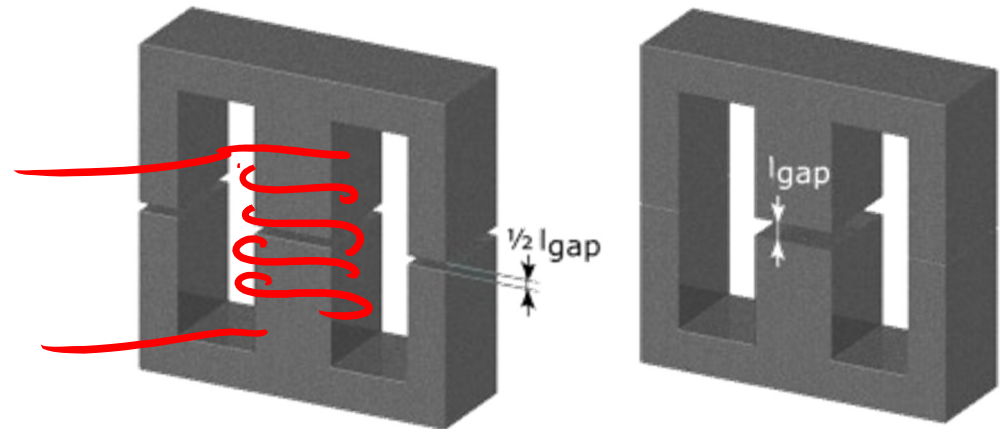
Inductor Design

Freedoms:

1. Core Size and Material
2. Number of turns and wire gauge
3. Length of Air Gap

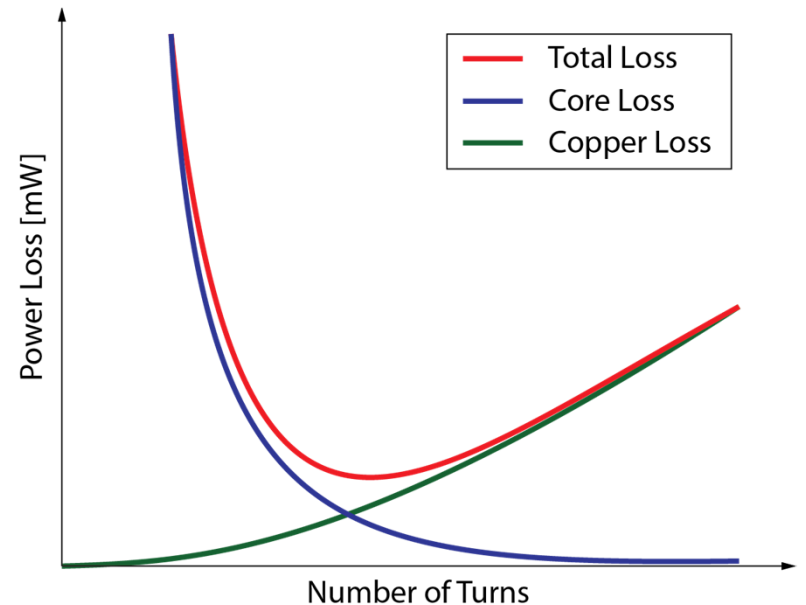
Constraints:

1. Obtain Designed L
2. Prevent Saturation
3. Minimize Losses



Minimization of Losses

- For given core, number of turns can be used to index possible designs, with air gap solved after (and limited) to get correct inductance
- A minimum sum of the two exists and can be solved
- Design always subject to constraint $B_{max} < B_{sat}$



Spreadsheet Design

	A	B	C	D	E	F	G	H	I	J	K	L	M
1													
2	Fixed Design Params	Vg [V]	25	Design Choice	Pmax [W]	250	Gate Driver	Vdr [V]	12				
3		Vout [V]	50		L [uH]	250		dt [ns]	500				
4		dV [V]	2		fs [kHz]	2.00E+01		Rg_on [Ω]	10				
5		u0	1.257E-06					Rg_off [Ω]	2				
6		rho [Ohm]	1.68E-06										
7		TA [C]	25										
8													
9													
10	Current Stresses	D	0.50	MOSFET Losses	tsw_on [ns]	175	Total Losses	Rl,DC [mOhm]	4.71	Warnings			
11		Iout [A]	5.00		tsw_off [ns]	35		Pl,AC [mOhm]	10.05				
12		IL [A]	10.00		Prr	1.16		Pl,copper	0.48				
13		dil [A]	1.25		Pq1,ov	1.18		Pl,core	0.06				
14		Imax [A]	11.25		Pq2,bd	0.32		PL [w]	0.54				
15		lmin [A]	8.75		Pq1,Coss	0.00		Pq1 [w]	2.46				
16		Ilrms [A]	10.03		Pq1,Cond	0.12		Pq2 [w]	0.44				
17		Irip,rms [A]	0.72		Pq2,Cond	0.12		Ploss	3.44				
18		Iq1,rms [A]	7.09										
19		Iq2,rms [A]	7.09										
20	Ic,rms [A]	5.03											
21													
22	Core Geometry	Inductor n	10	MOSFET	Eff	98.64	OP. Temp			Warnings			
23		Core	ETD49-3C90		Ron [mOhm]	2.3		Rth [K/W]	3				
24		Ac [mm2]	211		Qg [nC]	210							
25		Wa [mm2]	273		Vr [V]	2							
26		Ve [mm3]	24000		Qrr [nC]	287							
27		MLT [mm]	85		Coss [pF]	4000		TQ1 [C]	32.4				
28					trr [ns]	100		TQ2 [C]	26.3				
29													
30													
31		Core Material Parameters	ui		2300	C [uF]		31.25					
32	Bsat [mT]		470	Desgin G	16.64								
33	Cm		0.0032										
34	x		1.46										
35	y		2.75										
36	ct2		0.000165										
37	ct1		0.031										
38													
39	Inductor Design	DeltaB [T]	0.05										
40		Bmax [mT]	0.44										
41		lg [mm]	0.95										
42		Aw [mm^2]	9.1										
43		rw [mm]	1.70										
44	Skin Depth [mm]	0.46											
45													

- Use of spreadsheet permits simple iteration of design
- Can easily change core, switching frequency, loss constraints, etc.

Matlab (Programmatic) Design

```
1 function [n, lg, Pq1, Pq2, Pl, eta, Cmin ] = TestBoostDesign(Pmax, fs, L, dt, core_geom, core_mat, MOSFET)
2 %TestBoostDesign calculate boost conveter efficiency and temperature rise
3 %for various designs
4 % fs = switching frequency (in Hz)
5 % L = inductance (in Henries)
6 % n = number of turns on inductor
7 % dt = switching dead time (in seconds)
8 % core_geom = core geometry, chosen from 'EFD25', 'ETD29', 'ETD39', 'ETD44', or 'ETD49'
9 % core_mat = core material, chosen from '3F3', '3C90', or '3F4'
10 % MOSFET = MOSFET selection, chosen from 'AOT', 'FDP', 'IPP2', 'IRF',
11 % 'CSD' or 'IPPO'
12
13 - Vg = 25;
14 - Vout = 50;
15 - Iout = Pmax/Vout;
16 - Ts = 1/fs;
17 - D = 1-Vg/Vout;
18 - dVout = 2;
19 - Vdr = 12;
20
21 - Rgon = 10;
22 - Rgoff = 2;
23
24 - rho = 1.724e-6; %ohms*cm
25 - u0 = 4*pi*1e-7;
26
27 %% Inductor Datasheet Parameters
28 - switch core_geom
29 - case 'EFD25'
30 -     MLT = 46.4; %mm
31 -     Ac = 58; %mm^2
32 -     Ve = 3300; %mm^3
33 -     Wa = 40.2; %mm^2
```

- Matlab, or similar, permits more powerful iteration and plotting/insight into design variation

Closed-Form Design Methods

- **Fundamentals of Power Electronics Ch 13-15**
 - Step-by-Step design methods
 - Simplified, and may require additional calculations

K_g and K_{gfe} Methods

- Two closed-form methods to solve for the optimal inductor design *under certain constraints/assumptions*
- Neither method considers losses other than DC copper and (possibly) steinmetz core loss
- Both methods particularly well suited to spreadsheet/iterative design procedures

	K_g	K_{gfe}
Losses	DC Copper (specified)	DC Copper, SE Core Loss (optimized)
Saturation	Specified	Checked After
B_{max}	Specified	Optimized

K_g Method

- Method useful for filter inductors where ΔB is small
- Core loss is not included, but may be significant particularly if large ripple is present
- Copper loss is specified through a set target resistance
- The desired B_{max} is given as a constraint
- Method does not check feasibility of design; must ensure that air gap is not extremely large or wire size excessively small
- Simple first-cut design technique; useful for determining approximate core size required
- Step-by-step design procedure included on website

$$K_g \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u} 10^8 \quad (\text{cm}^5)$$

The following quantities are specified, using the units

Wire resistivity	ρ	(Ω -cm)
Peak winding current	I_{max}	(A)
Inductance	L	(H)
Winding resistance	R	(Ω)
Winding fill factor	K_u	
Core maximum flux density	B_{max}	(T)

$$\ell_g = \frac{\mu_0 L I_{max}^2}{B_{max}^2 A_c} 10^4 \quad (\text{m})$$

The core dimensions are expressed in cm:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)

$$n = \frac{L I_{max}}{B_{max} A_c} 10^4$$

$$A_w \leq \frac{K_u W_A}{n} \quad (\text{cm}^2)$$

$$R = \frac{\rho n (MLT)}{A_w} \quad (\Omega)$$

K_{gfe} Method

- Method useful for cases when core loss and copper loss are expected to be significant
- Saturation is not included in the method, rather it must be checked afterward
- Enforces a design where the sum of core and copper is minimized

K_{gfe} Procedure

The following quantities are specified, using the units noted:

Wire effective resistivity	ρ	(Ω -cm)
Total rms winding current, ref to pri	I_{tot}	(A)
Desired turns ratios	$n_2/n_1, n_3/n_1, \text{etc.}$	
Applied pri volt-sec	λ_1	(V-sec)
Allowed total power dissipation	P_{tot}	(W)
Winding fill factor	K_u	
Core loss exponent	β	
Core loss coefficient	K_{fe}	(W/cm ³ T ^{β})

Other quantities and their dimensions:

Core cross-sectional area	A_c	(cm ²)
Core window area	W_A	(cm ²)
Mean length per turn	MLT	(cm)
Magnetic path length	ℓ_e	(cm)
Wire areas	A_{w1}, \dots	(cm ²)
Peak ac flux density	ΔB	(T)

$$K_{gfe} \geq \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{(2/\beta)}}{4K_u (P_{tot})^{((\beta+2)/\beta)}} 10^8$$

$$\Delta B = \left[10^8 \frac{\rho \lambda_1^2 I_{tot}^2}{2K_u} \frac{(MLT)}{W_A A_c^3 \ell_m} \frac{1}{\beta K_{fe}} \right]^{(\frac{1}{\beta+2})}$$

$$n_1 = \frac{\lambda_1}{2\Delta B A_c} 10^4 \quad n_k = n_1 \frac{n_k}{n_1}$$

$$\alpha_k = \frac{n_k I_k}{n_1 I_{tot}} \quad A_{wk} \leq \frac{\alpha_2 K_u W_A}{n_2}$$

Verify

K_{gfe} Method: Summary

- Method enforces an operating ΔB in which core and copper losses are minimized
- Only takes into account losses from standard Steinmetz equation; not correct unless waveforms are sinusoidal
- Does not consider high frequency losses
- Step-by-step design procedure included on website