PCB Layout for Experiment 5

- Include test points for voltages/currents to aid debugging
- Where possible, give yourself “backup options”
- Include option for heatsink
- Fans available, but consider power consumption
- Make sure parts you select are available and have sufficient stock
  - even if some get ordered in the interim

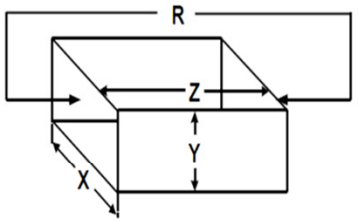
Basic PCB Layout Concepts

- Kelvin Connection
- Parasitic Capacitances and Decoupling
- Loop Inductances / Complete Routing
- Decoupling
- Ground Plane / Return Currents
- Partitioning

Trace Parasitics

$$R = \frac{\rho Z}{XY}$$

ρ = RESISTIVITY



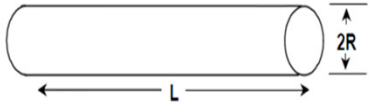
SHEET RESISTANCE CALCULATION FOR
1 OZ. COPPER CONDUCTOR:

ρ = 1.724 X 10-6 Ωcm, Y = 0.0036cm

$$R = 0.48 \frac{Z}{X} m\Omega$$

$\frac{Z}{X}$ = NUMBER OF SQUARES

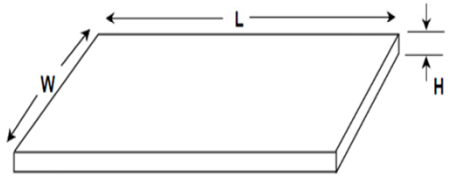
R = SHEET RESISTANCE OF 1 SQUARE (Z=X)
= 0.48mΩ/SQUARE



L, R in mm

$$\text{WIRE INDUCTANCE} = 0.0002L\left[\ln\left(\frac{2L}{R}\right) - 0.75\right] \mu H$$

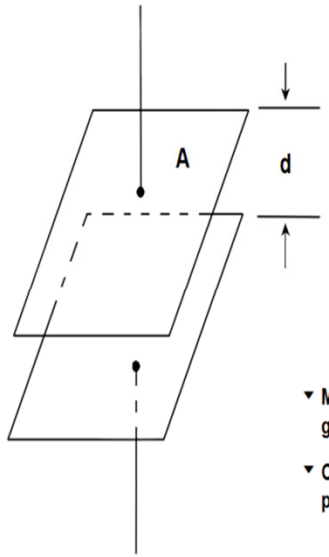
EXAMPLE: 1cm of 0.5mm o.d. wire has an inductance of 7.26nH
(2R = 0.5mm, L = 1cm)



$$\text{STRIP INDUCTANCE} = 0.0002L\left[\ln\left(\frac{2L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right] \mu H$$

EXAMPLE: 1cm of 0.25 mm PC track has an inductance of 9.59 nH
(H = 0.038mm, W = 0.25mm, L = 1cm)

Figure 12.18: *Wire and Strip Inductance Calculations*



$$C = \frac{0.00885\ E_r\ A}{d}\ pF$$

A = plate area in mm^2

d = plate separation in mm

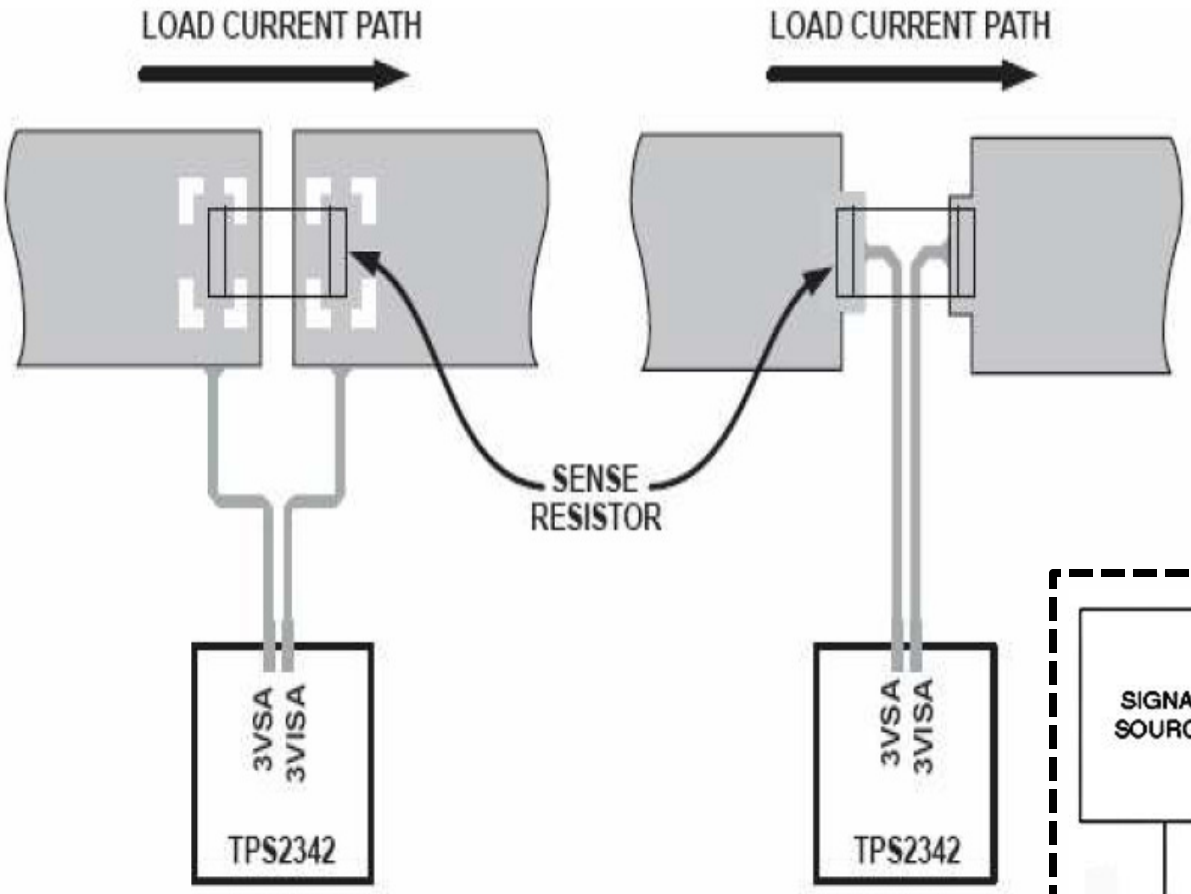
E_r = dielectric constant relative to air

- Most common PCB type uses 1.5mm glass-fiber epoxy material with E_r = 4.7
- Capacitance of PC track over ground plane is roughly 2.8 pF/cm^2

Figure 12.24: *Capacitance of two parallel plates*

Figure 12.2: *Calculation of Sheet Resistance and Linear Resistance for Standard Copper PCB Conductors*

Kelvin Connection



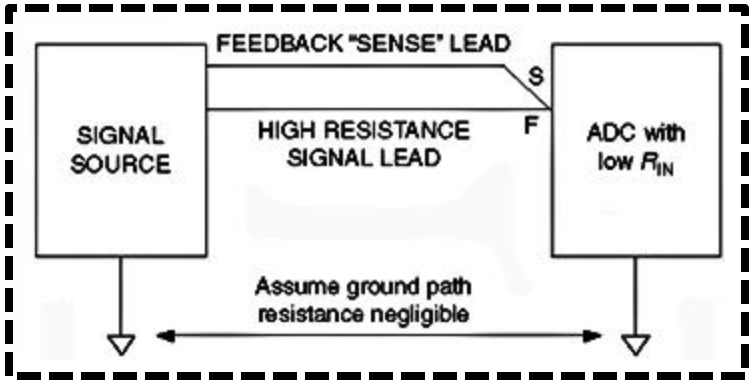


Figure 1. Kelvin Connection

Texas Instruments, "LMP8640/-Q1/HV Precision High Voltage Current Sense Amplifiers"

Decoupling

- Always add bypass capacitor at power supply for any IC/reference
- Use small-valued (~100nf), low ESR and ESL capacitors (ceramic)
- Limit loop for any di/dt

Decoupling Capacitance

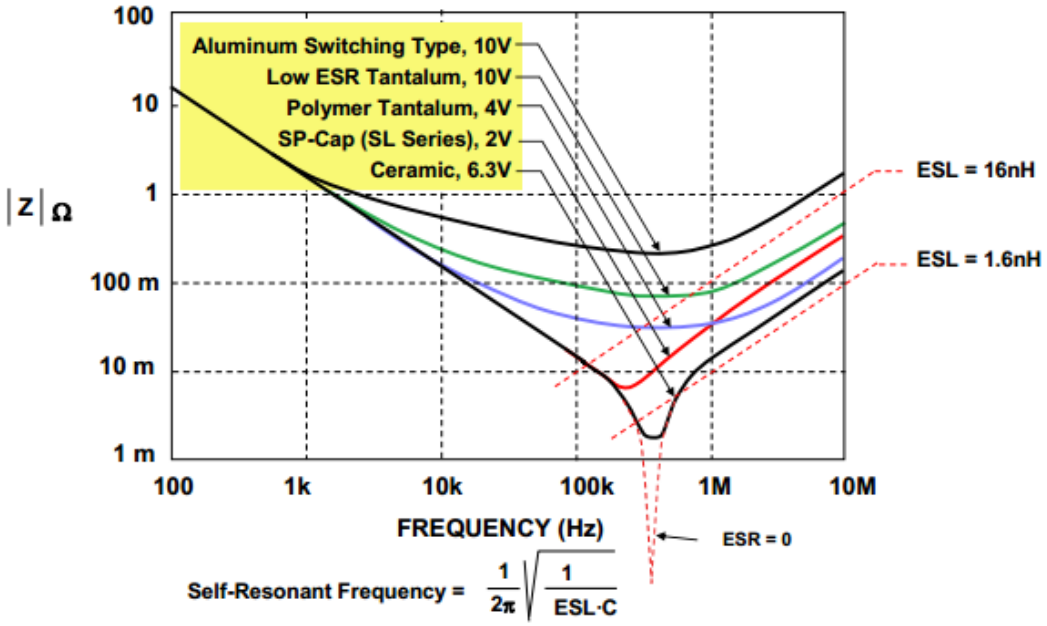
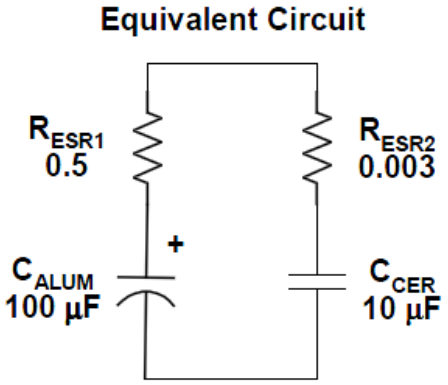


Figure 4: Impedance of Various 100µF Capacitors



High Impedance Nodes and Capacitive Coupling

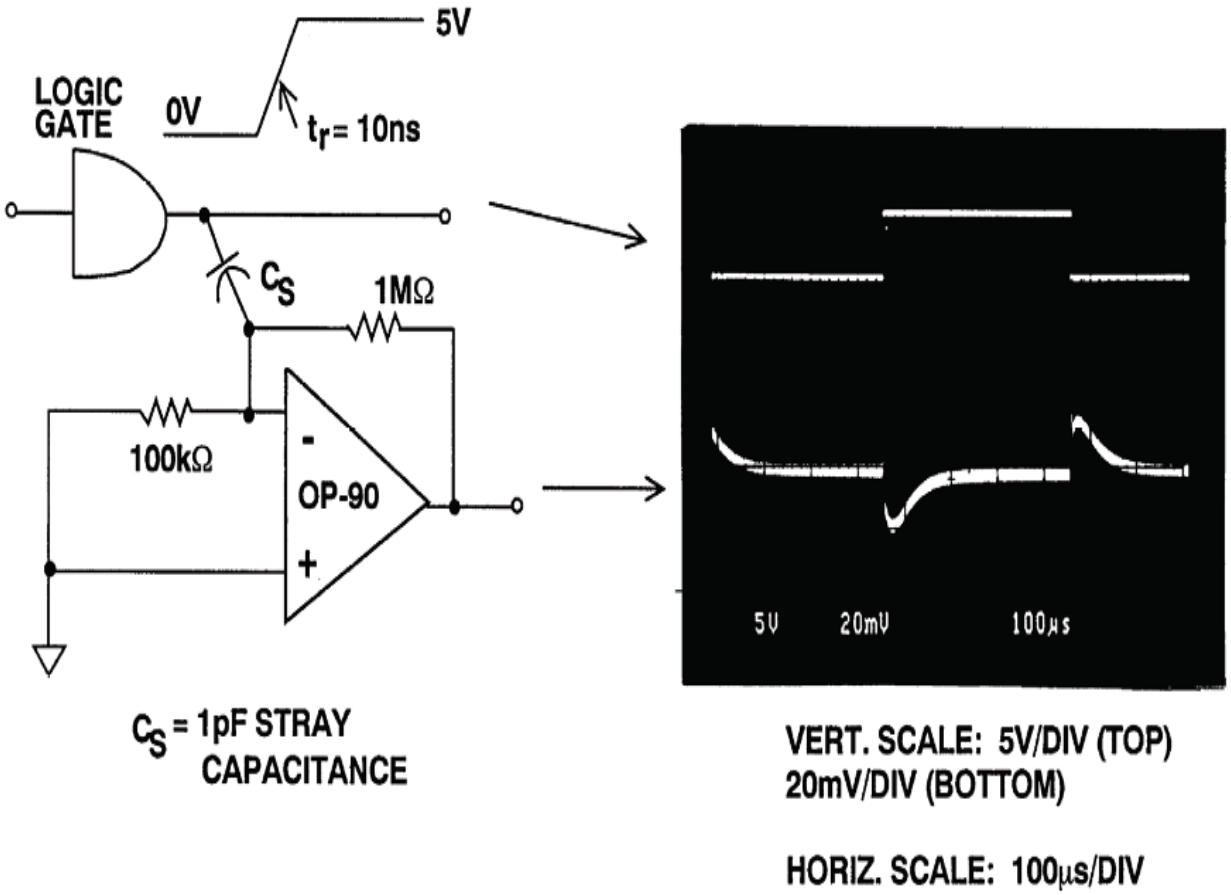


Figure 12.29 *High Circuit Impedances Increase Susceptibility to Noise Pickup*

Capacitive Shielding

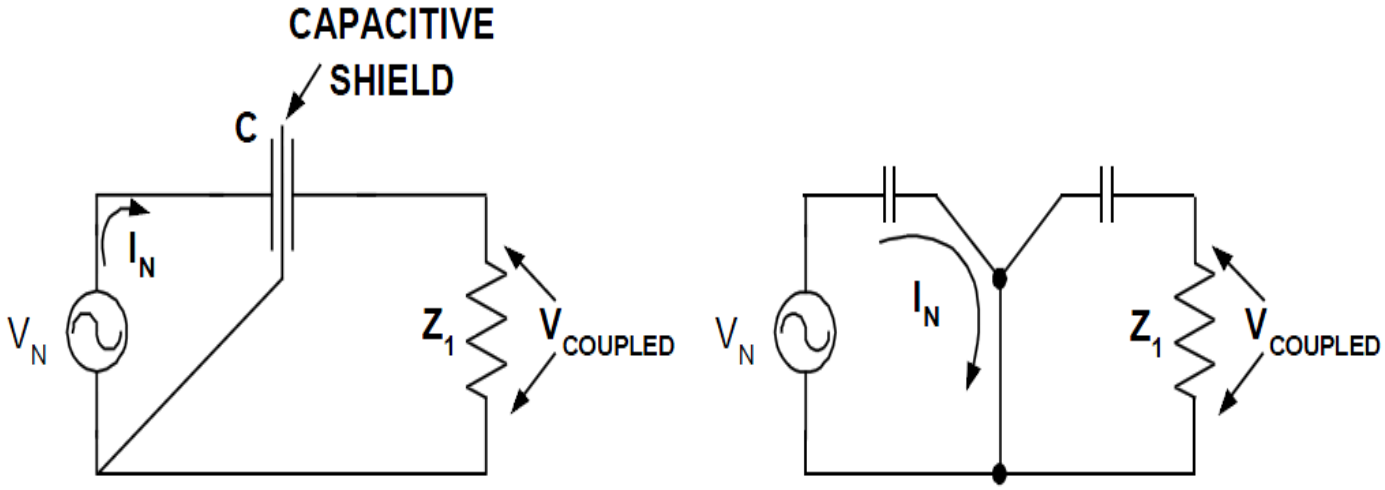
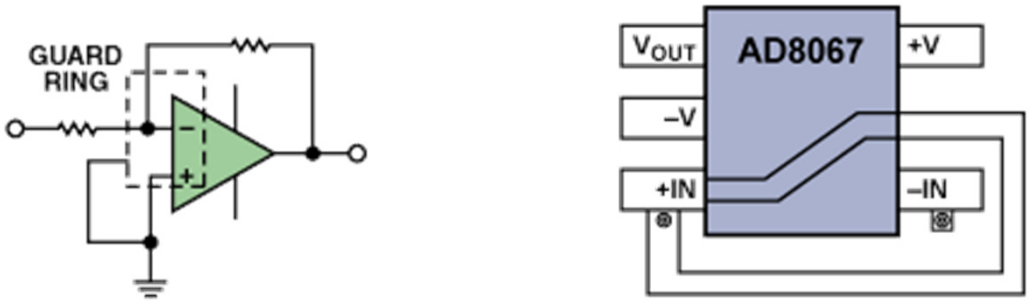
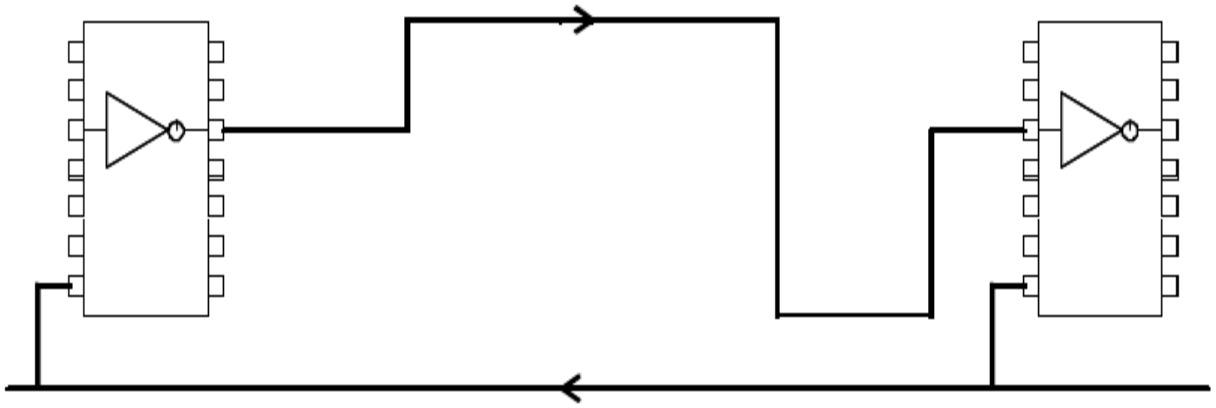


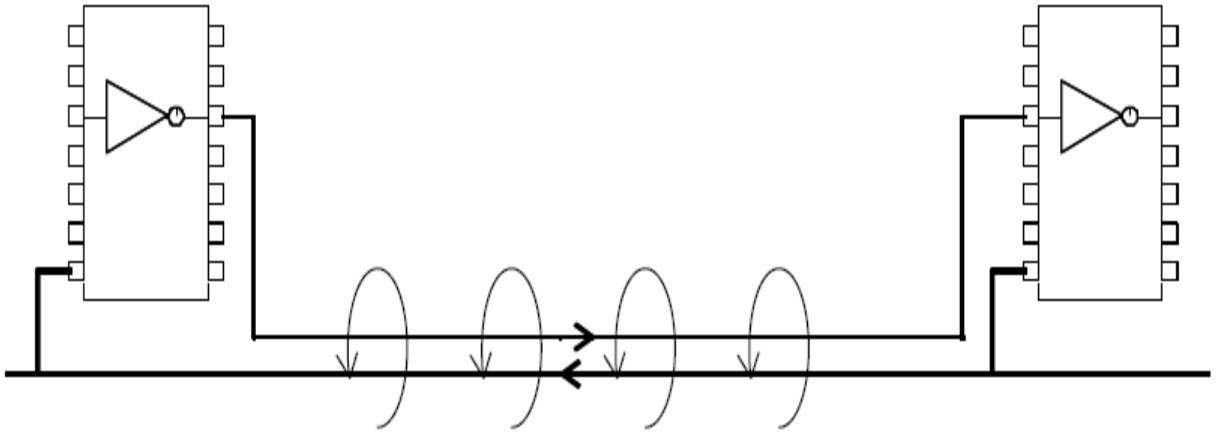
Figure 12.26: *An Operational Model of a Faraday Shield*



Loop Inductances



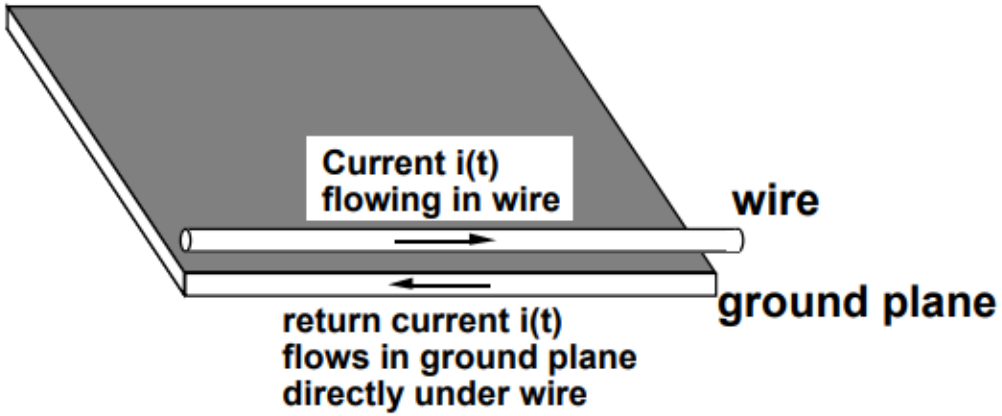
Bad practice: wide separation of signal and return



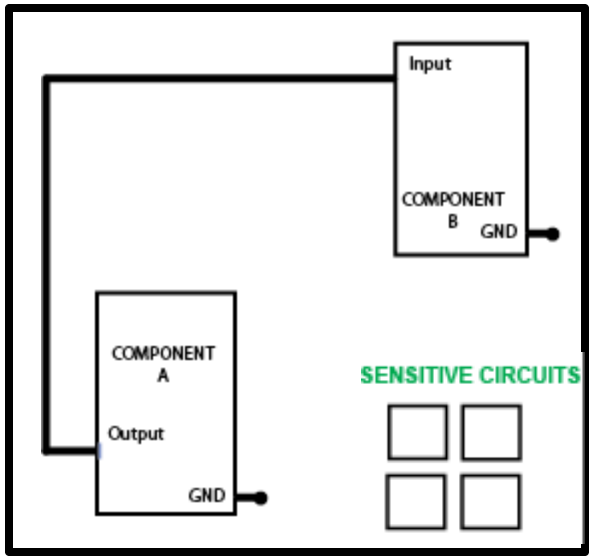
Good practice: close coupling of signal and return

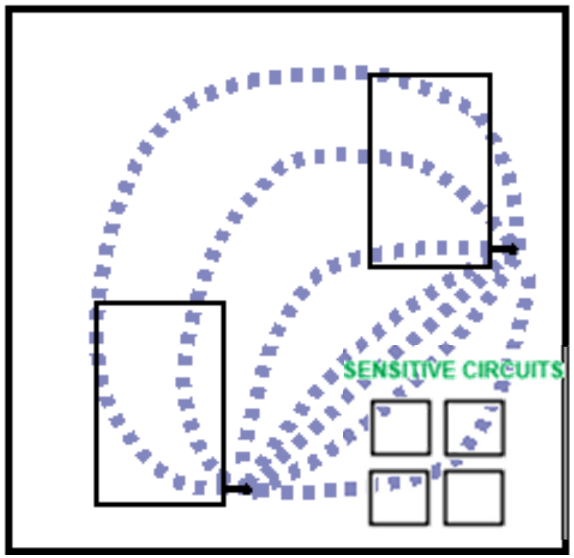
Ground Plane

- Benefits:
  - Common reference
  - Shielding
  - Heat dissipation
  - Reduced inductance (increased capacitance)
- Resist urge to cut ground plane as much as possible; consider paths of return currents when cuts are unavoidable



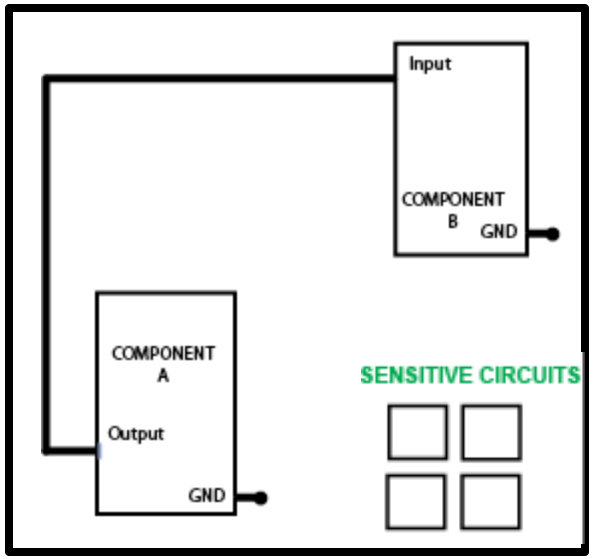
Ground Plane Cuts

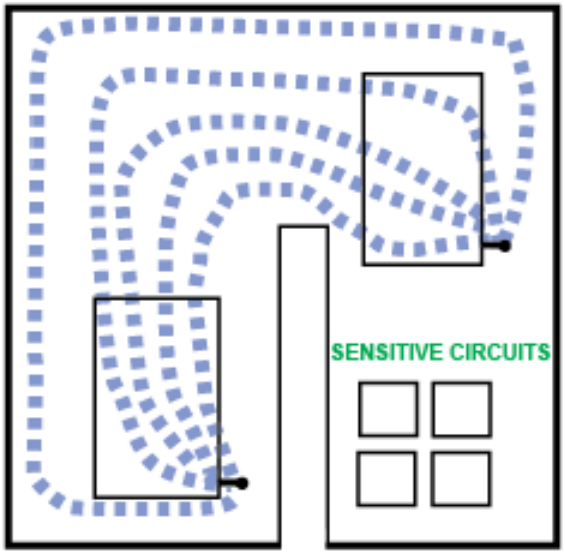




Ground return current path

Ground Plane Cuts





Ground return current path

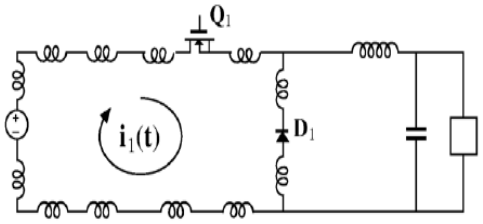
Cuts in Ground Plane

- Goals:
  - minimize inductance/loops
  - Minimize ground interference
- Routing cuts should be kept short and out of the path of any significant (high frequency) return paths
- Cuts can be used effectively for ground isolation, and to reduce noise coupled between digital/analog/power circuitry
- Reducing parasitic capacitance in sensitive signal locations (i.e. op-amp circuitry)

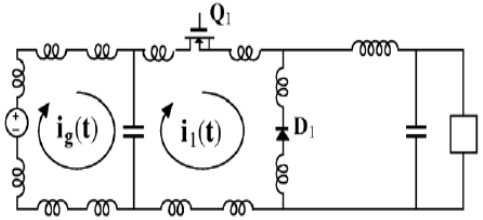
Ground Plane Example

Half Bridge Loop Inductance

Parasitic inductances of input loop explicitly shown:

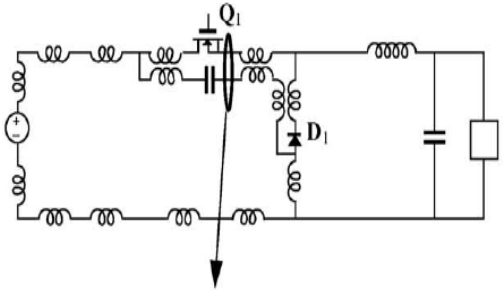


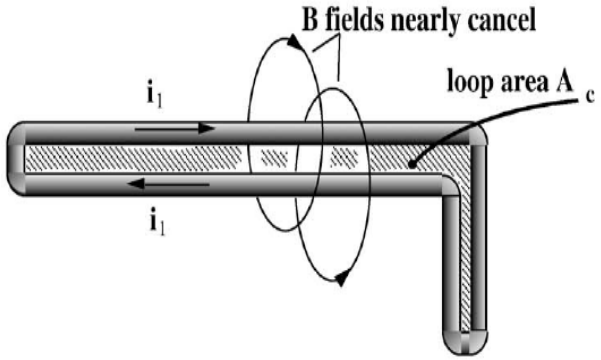
Addition of bypass capacitor confines the pulsating current to a smaller loop:



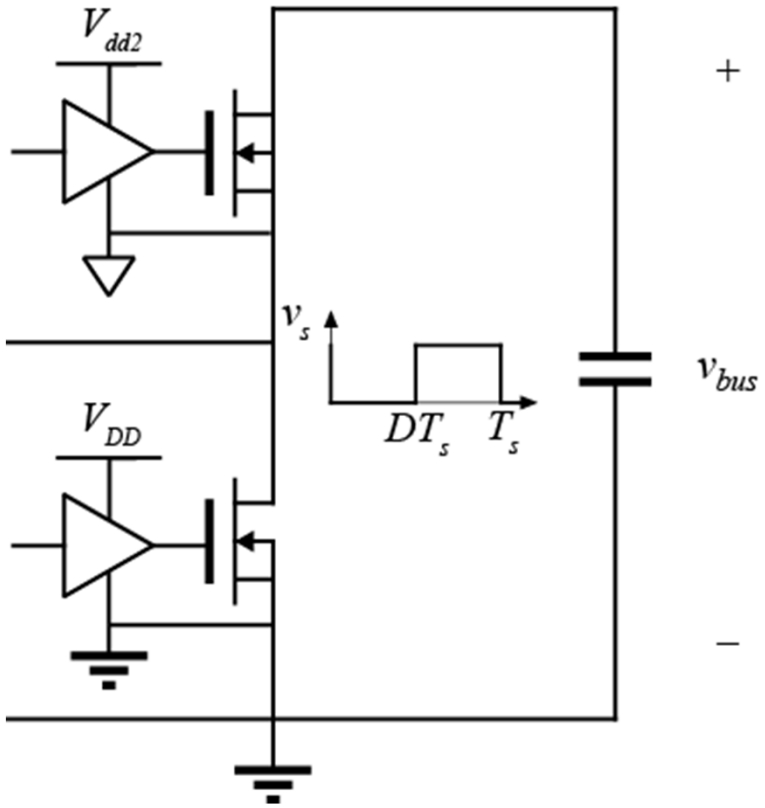
high frequency currents are shunted through capacitor instead of input source

Even better: minimize area of the high frequency loop, thereby minimizing its inductance

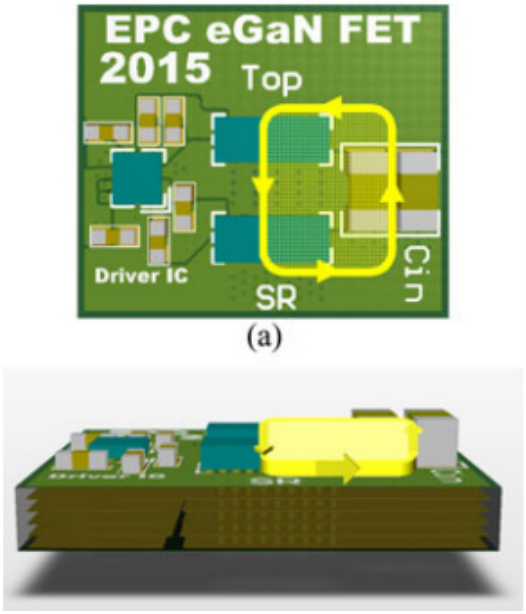


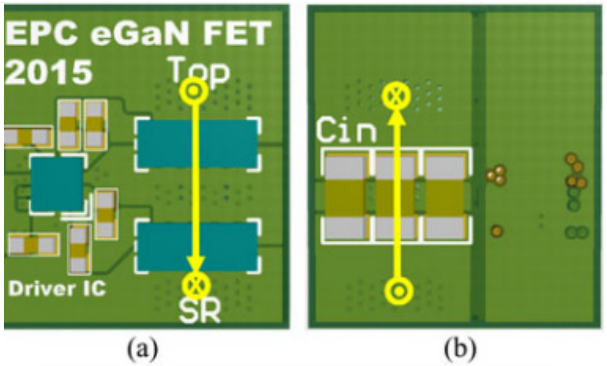


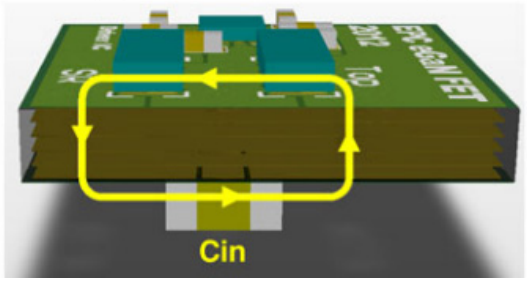
Bridge Layout

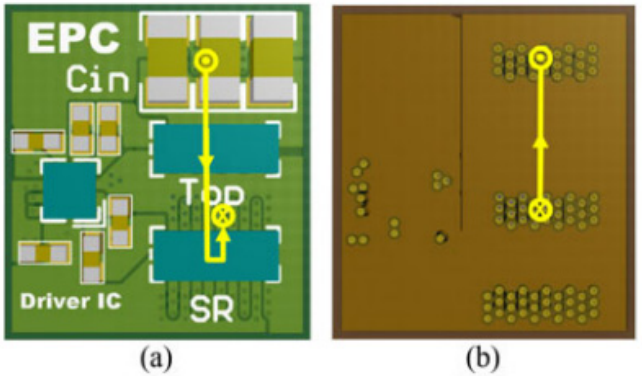


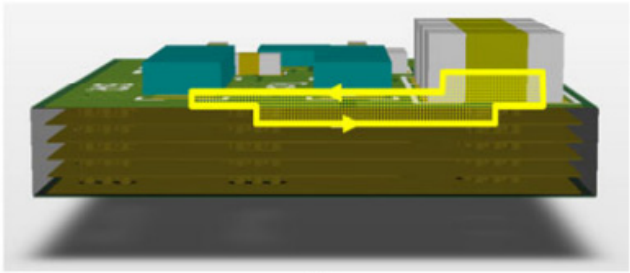
Half Bridge Layout: Another Example









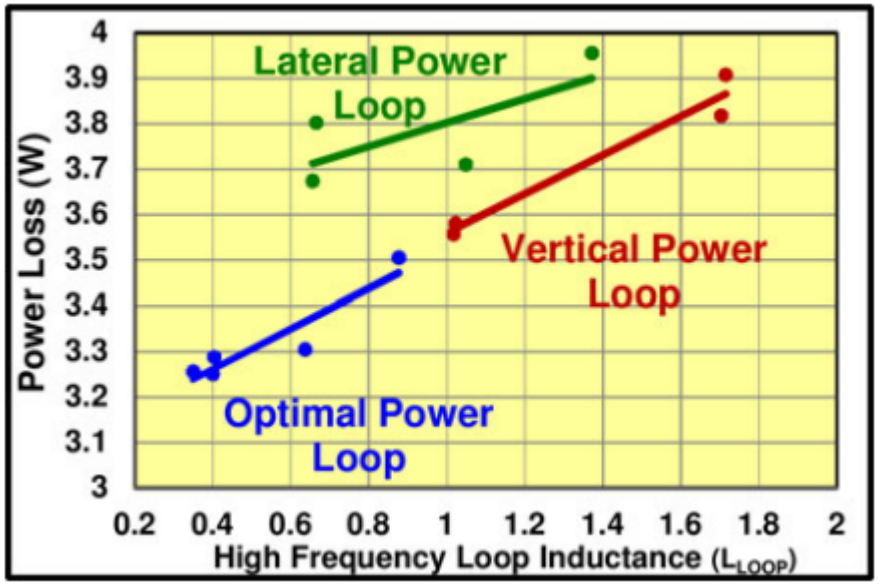


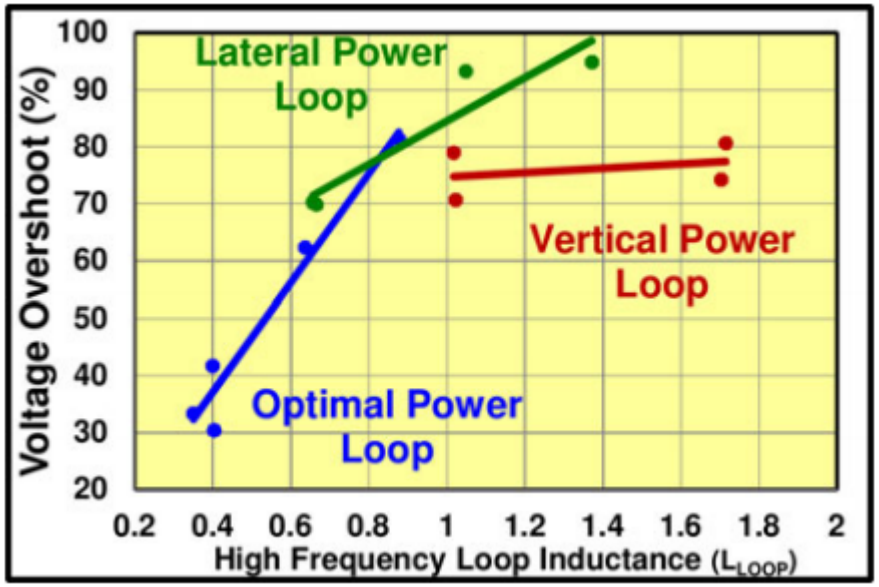
Lateral

Vertical

“Optimal”

Layout Impact Measurements





- Smallest Loop Area results in
  - Smaller overvoltage
  - Lower switching loss