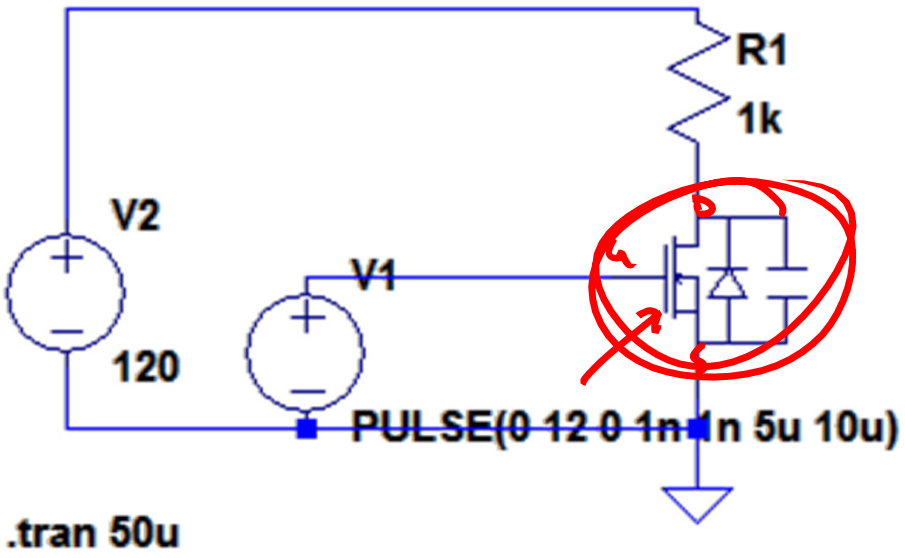
Simulation Modeling

Circuit Simulation

- LTSpice
  - Other tools accepted, but not supported
- Choose model type (switching, averaged, dynamic)
- Supplement analytical work rather than repeating it
- Show results which clearly demonstrate what matches and what does not with respect to experiments (i.e. ringing, slopes, etc.)

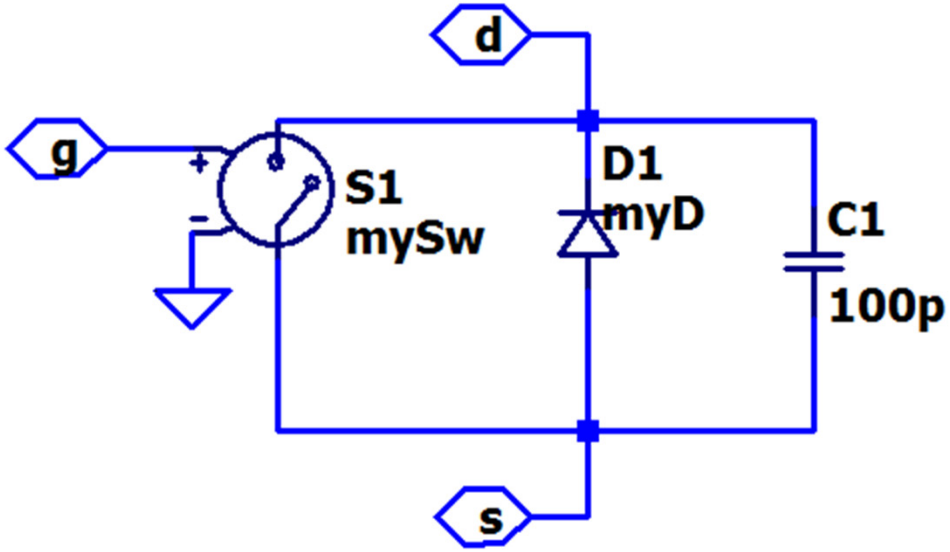
LTSpice Modeling Examples



- Example files added to course materials page
  - Custom model
  - VDMOS model
  - Manufacturer Model

Custom Transistor Model

```
.model myD D(n=.001)
.model mySw SW(Ron=10m Roff=1G Von=1 Voff = .5 )
```

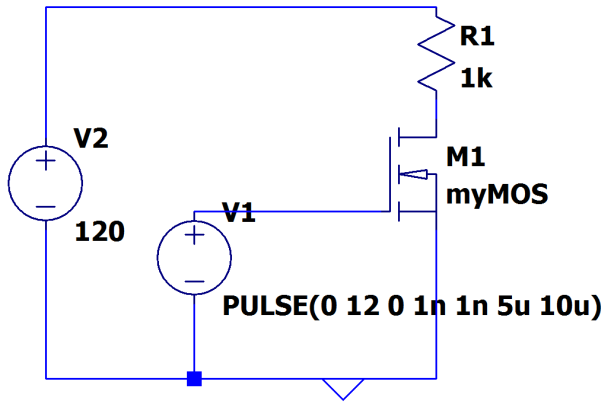


VDMOS Model

Name	Description	Units	Default	Example
Vto	Threshold voltage	V	0	1.0
Kp	Transconductance parameter	A/V^2	1.	.5
Phi	Surface inversion potential	V	0.6	0.65
Lambda	Channel-length modulation	1/V	0.	0.02
mtriode	Conductance multiplier in triode region(allows independent fit of triode and saturation regions	-	1.	2.
subthres	Current(per volt Vds) to switch from square law to exponential subthreshold conduction	A/V	0.	1n
BV	Vds breakdown voltage	V	Infin.	40
IBV	Current at Vds=BV	A	100pA	1u
NBV	Vds breakdown emission coefficient	-	1.	10
Rd	Drain ohmic resistance	Ω	0.	1.
Rs	Source ohmic resistance	Ω	0.	1.
Rg	Gate ohmic resistance	Ω	0.	2.
Rds	Drain-source shunt resistance	Ω	Infin.	10Meg
Rb	Body diode ohmic resistance	Ω	0.	.5
Cio	Zero-bias body diode	F	0.	1n

.model myMOS VDMOS(nchan Rg=3 Rd=14m Rs=10m Vto=-.8 Kp=32
+ Cgdmax=.5n Cgdmin=.07n Cgs=.9n Cjo=.26n Is=26p Rb=17m)

.tran 50u



- Note: any other parameters **ignored**
  - E.g. ron = 3m Qg = 1n mfg = Infineon

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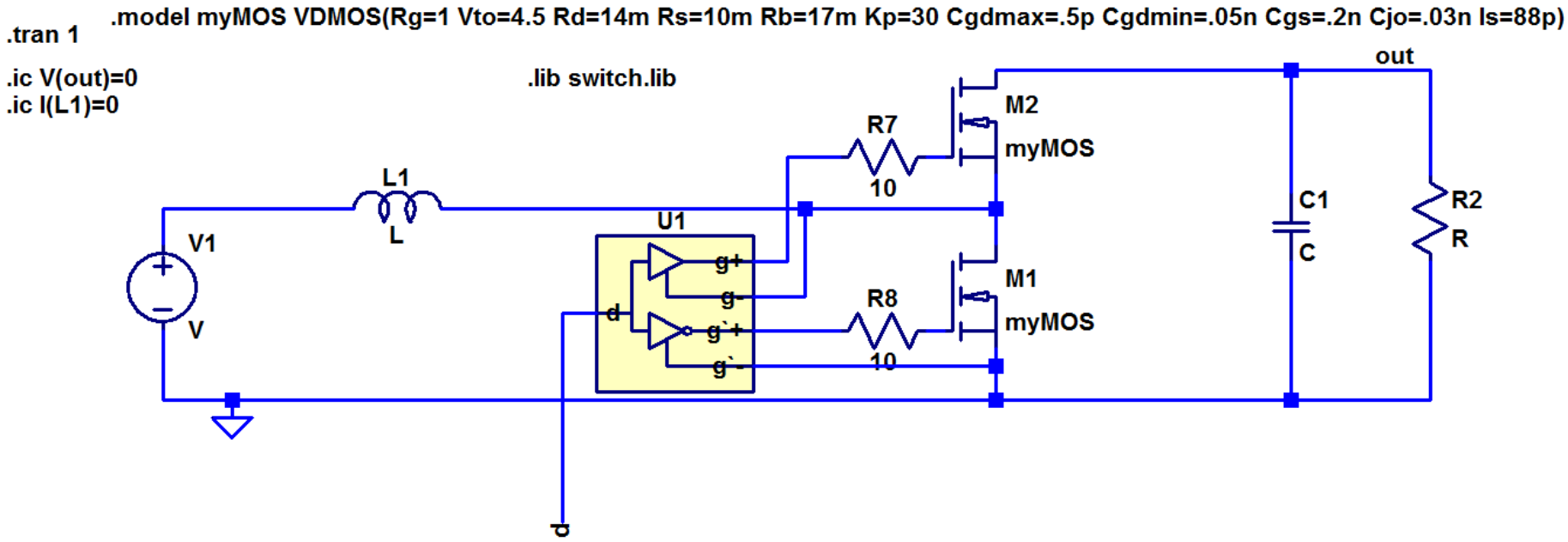
Manufacturer Device Model

- Text-only netlist model of device including additional parasitics and temperature effects
- May slow or stop simulation if timestep and accuracy are not adjusted appropriately

Full Switching Simulation



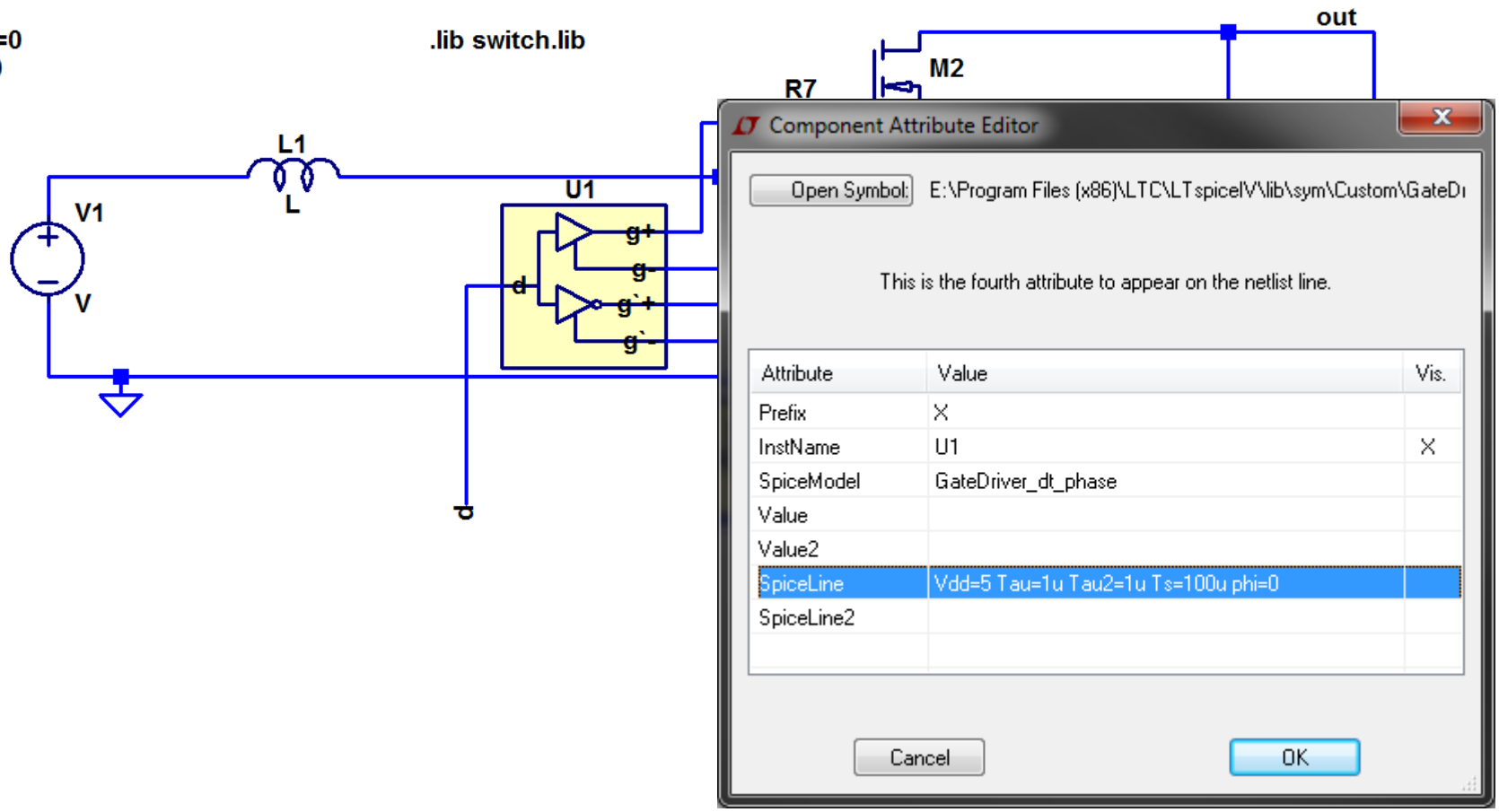
Full Switching Simulation

.model myMOS VDMOS(Rg=1 Vto=4.5 Rd=14m Rs=10m Rb=17m Kp=30 Cgdmax=.5p Cgdmin=.05n Cgs=.2n Cjo=.03n Is=88p)

.tran 1

.ic V(out)=0
.ic I(L1)=0

.lib switch.lib



Experiment 2

Experiment 3

Experiment Procedure
- Prelab Assignment
- Experiment 3 Procedure

Experiment 3 Components
- Contents of the Experiment 3 Parts Kit
- Contents of the Magnetics Library
- Breakout Board Schematics and Layout (pdf)
- Breakout Board Schematics and PCB Layout (Altium)

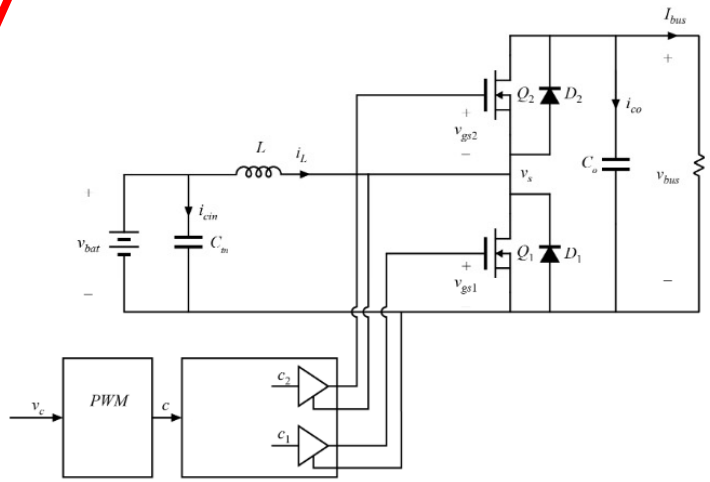
Reference Materials
- Designing Bootstrap Networks
- Power Converter Layout
- Reduction of Ringing in Power Converters (TI App. Note)
- RMS Values of Commonly Observed Waveforms

LTSpice Example Files
- **Examples of power semiconductor modeling using custom or manufacturer models**
- **Example Switching and Averaged Boost LTSpice Models**

Magnetics Design
- Filter Inductor Design Notes
- Kg Method Step-by-Step
- Kgfe Method Step-by-Step
- Overview of Empirical Core Loss Calculation Techniques
- Overview of Empirical State of Core Loss Prediction
- Magnetics Design Tables
- AWG Chart

Experiment 4

Available on Exp 3 Webpage



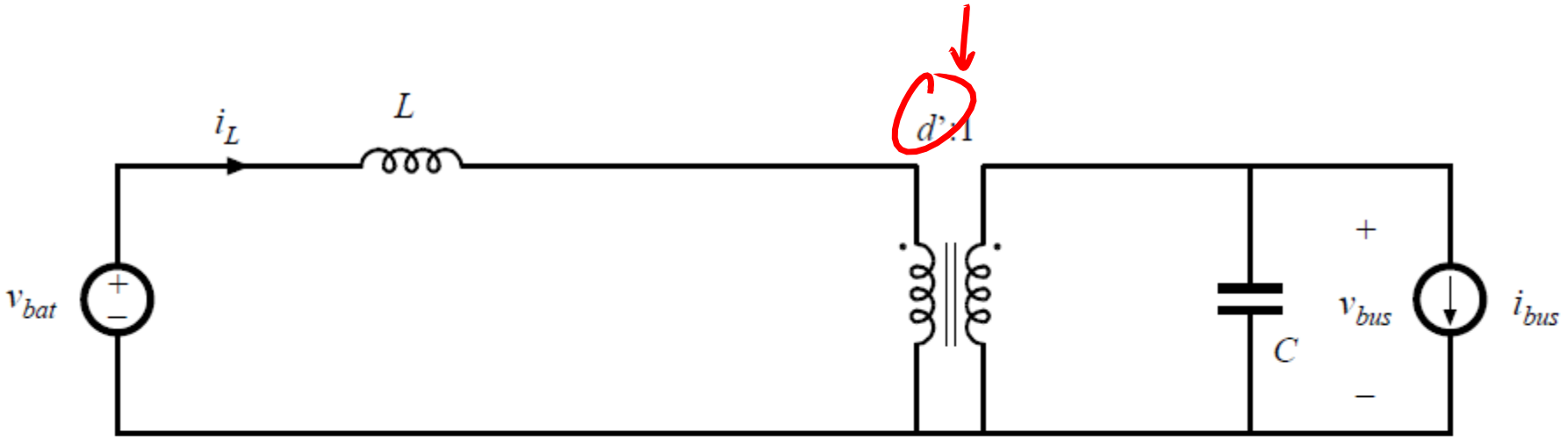
Full Switching Model

- Gives valuable insight into circuit operation
  - Understand expected waveforms
  - Identify discrepancies between predicted and experimental operation
- Slow to simulate; significant high frequency content
- Cannot perform AC analysis

Averaged Switch Modeling: Motivation

- A *large-signal, nonlinear* model of converter is difficult for hand analysis, but well suited to simulation across a wide range of operating points
- Want an *averaged* model to speed up simulation speed
- Also allows linearization (AC analysis) for control design

Nonlinear, Averaged Circuit



$d(t) \cdot v_{bus}(t)$

$$L\frac{d\langle i_L\rangle}{dt} = \langle v_{bat}\rangle - (1-d)\langle v_{bus}\rangle$$

$$C\frac{d\langle v_{bus}\rangle}{dt} = (1-d)\langle i_L\rangle - \langle i_{bus}\rangle$$

DC analysis

$\frac{dx}{dt} = 0$

↓

DC steady-state averaged behavior

AC analysis

small-signal analysis

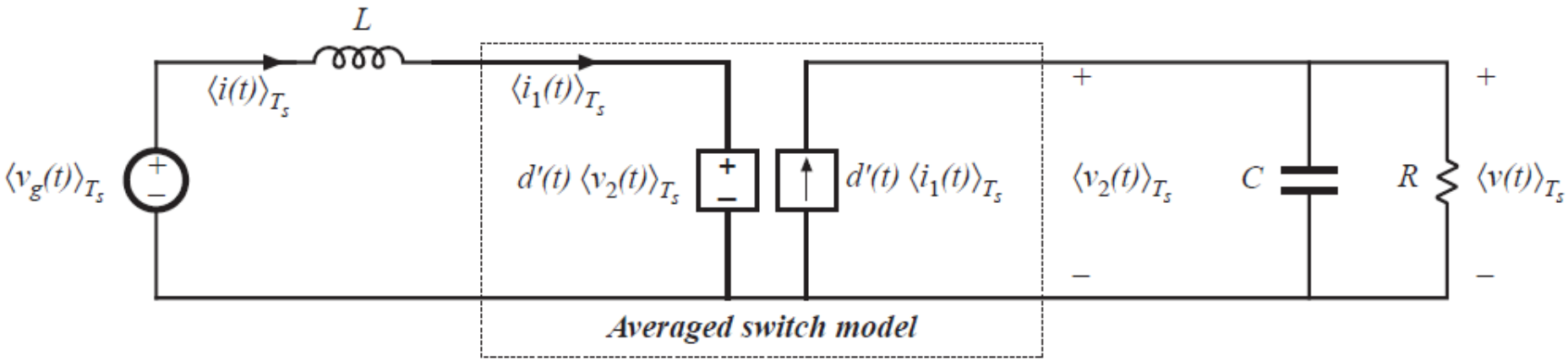
$x(t) = X + \hat{x}$

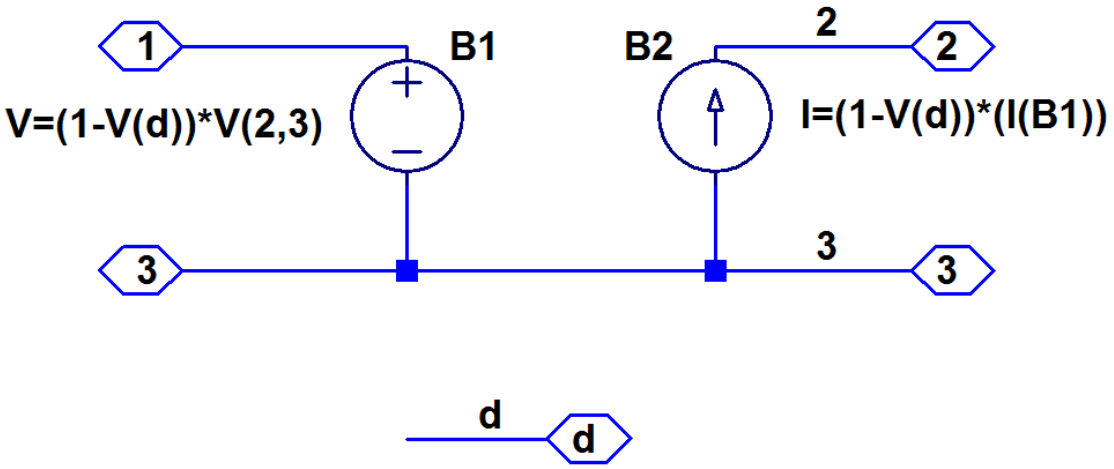
↓

Averaged, linear small-signal equations

for simulating: no need to linearize.

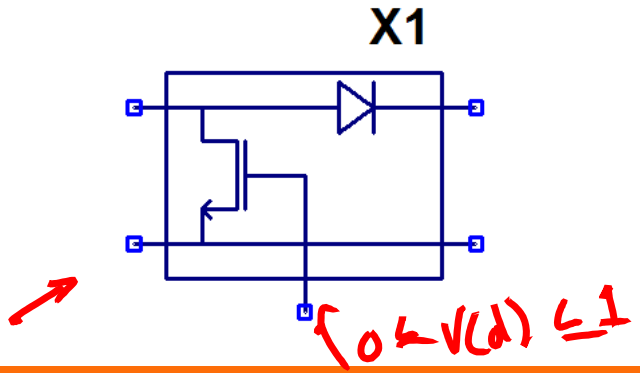
Implementation in LTSpice



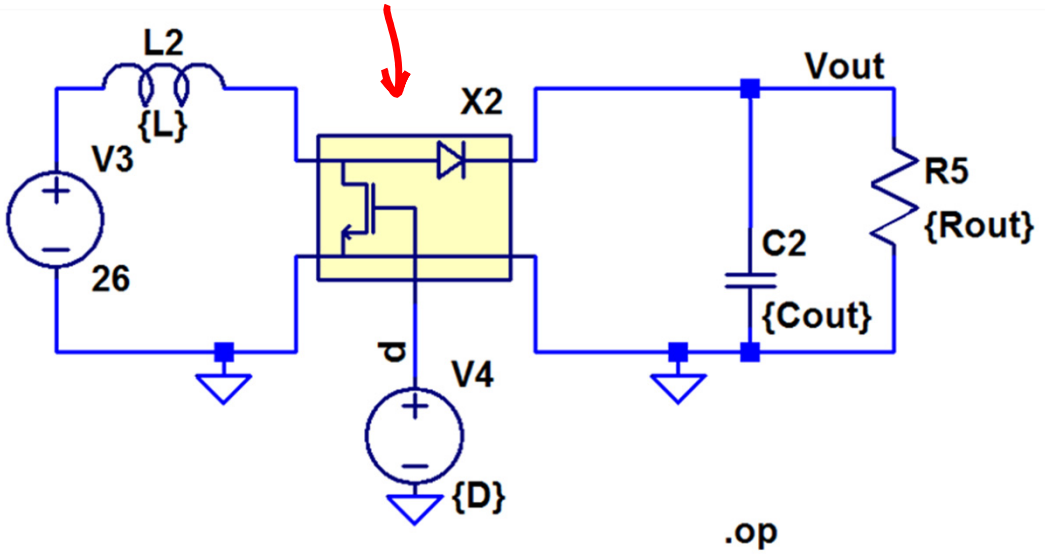


$$\left\langle v_1(t)\right\rangle_{T_s} = d'(t)\left\langle v_2(t)\right\rangle_{T_s}$$

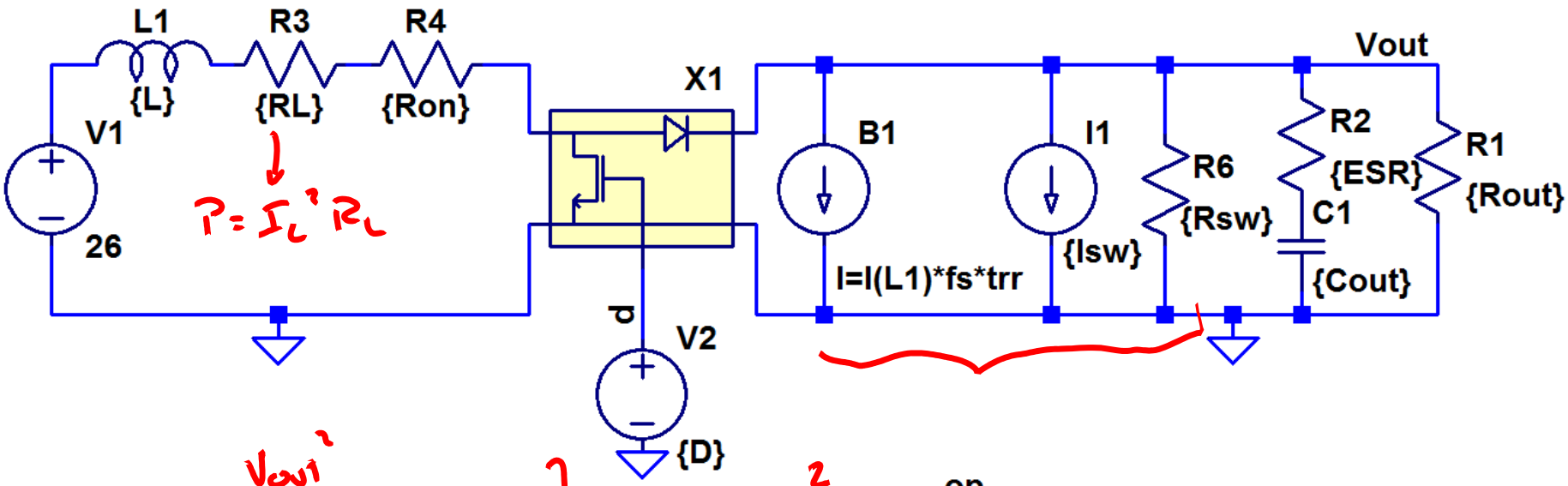
$$\left\langle i_2(t)\right\rangle_{T_s} = d'(t)\left\langle i_1(t)\right\rangle_{T_s}$$



Averaged Switch Model



Averaged Model With Losses



$P = I_L^2 R_L$

$P_{R_{sw}} = \frac{V_{out}^2}{R_{sw}}$

$P_{Coss} = \frac{1}{2} C_{oss} V_{out}^2 f_s$

$R_{sw} = \frac{2}{C_{oss} f_s}$

```
.op
.param Rout = 10
.step param Rout 10 100 10
```

What known error(s) will be present in loss predictions with this model?