Chapter 9

Controller Design

9.1. Introduction

In all switching converters, the output voltage $v(t)$ is a function of the input line voltage $v_g(t)$, the duty cycle $d(t)$, and the load current $i_{load}(t)$, as well as the converter circuit element values. In a dc-dc converter application, it is desired to obtain a constant output voltage $v(t) = V$, in spite of disturbances in $v_g(t)$ and $i_{load}(t)$, and in spite of variations in the converter circuit element values. The sources of these disturbances and variations are many, and a typical situation is illustrated in Fig. 9.1. The input voltage $v_g(t)$ of an off-line power supply may typically contain periodic variations at the second harmonic of the ac power system frequency (100Hz or 120Hz), produced by a rectifier circuit. The magnitude of $v_g(t)$ may also vary when neighboring power system loads are switched on or off. The load current $i_{load}(t)$ may contain variations of significant amplitude, and a typical power supply specification is that the output voltage must remain within a specified range (for example, 5V ±0.1V) when the load current takes a step change from, for example, full rated load current to 50% of the rated current, and vice-versa. The values of the circuit elements are

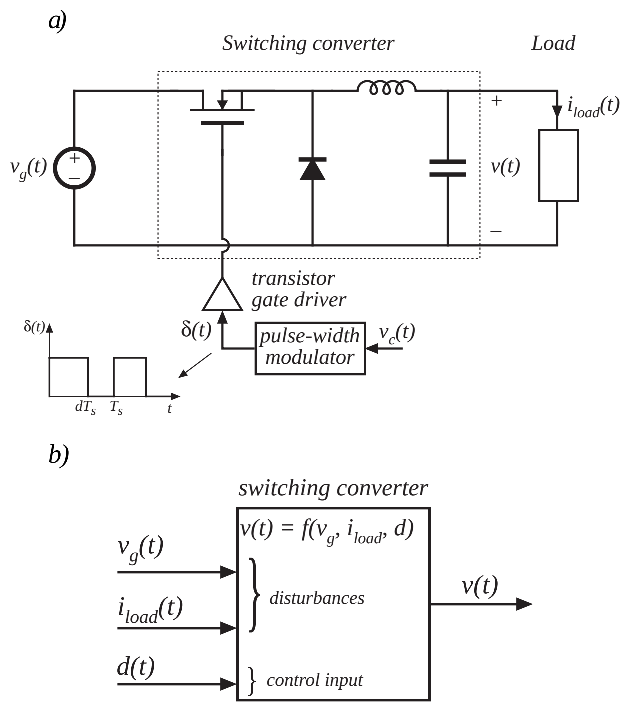

Fig. 9.1. The output voltage of a typical switching converter is a function of the line input voltage v_g, the duty cycle d, and the load current i_{load}: (a) open-loop buck converter, (b) functional diagram illustrating dependence of v on the independent quantities v_g, d, and i_{load}.

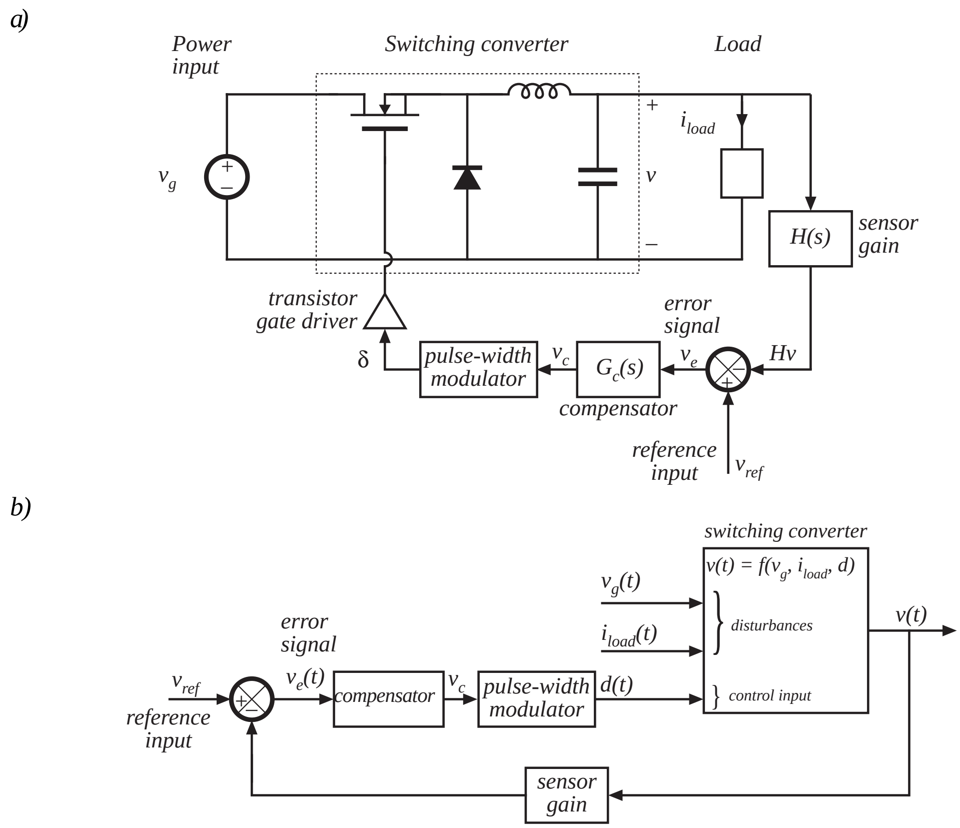

Fig. 9.2. Feedback loop for regulation of the output voltage: (a) buck converter, with feedback loop block diagram; (b) functional block diagram of the feedback system.

constructed to a certain tolerance, and so in high-volume manufacturing of a converter, converters are constructed whose output voltages lie in some distribution. It is desired that essentially all of this distribution fall within the specified range; however, this is not practical to achieve without the use of negative feedback. Similar considerations apply to inverter applications, except that the output voltage is ac.

So we cannot expect to simply set the dc-dc converter duty cycle to a single value, and obtain a given constant output voltage under all conditions. The idea behind the use of negative feedback is to build a circuit that automatically adjusts the duty cycle as necessary, to obtain the desired output voltage with high accuracy, regardless of disturbances in $v_g(t)$ or $i_{load}(t)$ or variations in component values. This is a useful thing to do whenever there are variations and unknowns that otherwise prevent the system from attaining the desired performance.

A block diagram of a feedback system is shown in Fig. 9.2. The output voltage $v(t)$ is measured, using a “sensor” with gain $H(s)$. In a dc voltage regulator or dc-ac inverter, the sensor circuit is usually a voltage divider, comprised of precision resistors. The sensor output signal $H(s)v(s)$ is compared with a reference input voltage $v_{ref}(s)$. The objective is to make $H(s)v(s)$ equal to $v_{ref}(s)$, so that $v(s)$ accurately follows $v_{ref}(s)$ regardless of disturbances or component variations in the compensator, pulse-width modulator, gate driver, or converter power stage.

The difference between the reference input $v_{ref}(s)$ and the sensor output $H(s)v(s)$ is called the error signal $v_e(s)$. If the feedback system works perfectly, then $v_{ref}(s) = H(s)v(s)$, and hence the error signal is zero. In practice, the error signal is usually nonzero but nonetheless small. Obtaining a small error is one of the objectives in adding a compensator network $G_c(s)$ as shown in Fig. 9.2. Note that the output voltage $v(s)$ is equal to the error signal $v_e(s)$, multiplied by the gains of the compensator, pulse-width modulator, and converter power stage. If the compensator gain $G_c(s)$ is large enough in magnitude, then a small error signal can produce the required output voltage $v(t) = V$ for a dc regulator (Q: how should H and v_{ref} then be chosen?). So a large compensator gain leads to a small error, and therefore the output follows the reference input with good accuracy. This is the key idea behind feedback systems.

The averaged small-signal converter models derived in chapter 7 are used in the following sections to find the effects of feedback on the small-signal transfer functions of the regulator. The loop gain $T(s)$ is defined as the product of the small-signal gains in the forward and feedback paths of the feedback loop. It is found that the transfer function from a disturbance to the output is multiplied by the factor $1/(1+T(s))$. Hence, when the loop gain T is large in magnitude, then the influence of disturbances on the output voltage is small. A large loop gain also causes the output voltage $v(s)$ to be nearly equal to $v_{ref}(s) / H(s)$, with very little dependence on the gains in the forward path of the feedback loop. So the loop gain magnitude $\| T \|$ is a measure of how well the feedback system works. All of these gains can be easily constructed using the algebra-on-the-graph method; this allows easy evaluation of important closed-loop performance measures, such as the output voltage ripple resulting from 120Hz rectification ripple in $v_g(t)$ or the closed-loop output impedance.

Stability is another important issue in feedback systems. Adding a feedback loop can cause an otherwise well-behaved circuit to exhibit oscillations, ringing and overshoot, and other undesirable behavior. An in-depth treatment of stability is beyond the scope of this book; however, the simple phase margin criterion for assessing stability is used here. When the phase margin of the loop gain T is positive, then the feedback system is stable. Moreover, increasing the phase margin causes the system transient response to be better-behaved, with less overshoot and ringing. The relation between phase margin and closed-loop response is quantified in section 9.4.

An example is given in section 9.5, in which a compensator network is designed for a dc regulator system. The compensator network is designed to attain adequate phase margin and good rejection of expected disturbances. Lead compensators and P-D controllers are used to improve the phase margin and extend the bandwidth of the feedback loop. This leads to better rejection of high-frequency disturbances. Lag compensators and P-I controllers are used to increase the low-frequency loop gain. This leads to better rejection of low-frequency disturbances and very small steady-state error. More complicated compensators can achieve the advantages of both approaches.

Injection methods for experimental measurement of loop gain are introduced in section 9.6. The use of voltage or current injection solves the problem of establishing the correct quiescent operating point in high-gain systems. Conditions for obtaining an accurate measurement are exposed. The injection method also allows measurement of the loop gains of unstable systems.

9.2. Effect of negative feedback on the network transfer functions

We have seen how to derive the small-signal ac transfer functions of a switching converter. For example, the equivalent circuit model of the buck converter can be written as in Fig. 9.3. This equivalent circuit contains three independent inputs: the control input variations $\hat{d}$, the power input voltage variations $\hat{v}_g$, and the load current variations $\hat{i}_{load}$. The output voltage variation $\hat{v}$ can therefore be expressed as a linear combination of the three independent inputs, as follows:

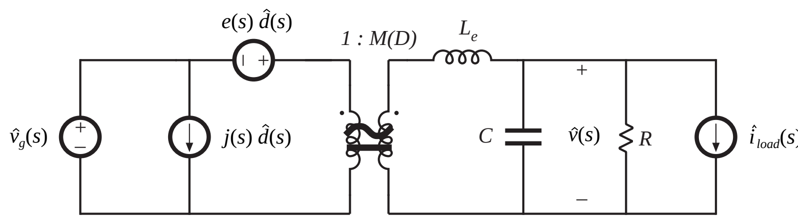

Fig. 9.3. Small-signal converter model, which represents variations in v_a, d, and i_{load}.

$$\hat{v}(s) = G_{vd}(s)\,\hat{d}(s) + G_{vg}(s)\,\hat{v}_g(s) - Z_{out}(s)\,\hat{i}_{load}(s) \tag{9-1}$$

where

$$G_{vd}(s) = \left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\substack{\hat{v}_g = 0 \\ \hat{i}_{load} = 0}}$$ converter control-to-output transfer function

$$G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\substack{\hat{d} = 0 \\ \hat{i}_{load} = 0}}$$ converter line-to-output transfer function

$$Z_{out}(s) = -\left.\frac{\hat{v}(s)}{\hat{i}_{load}(s)}\right|_{\substack{\hat{d}=0\\ \hat{v}_g=0}} \qquad \text{converter output impedance}$$

The Bode diagrams of these quantities are constructed in chapter 8. Equation (9-1) describes how disturbances $\hat{v}_g$ and $\hat{i}_{load}$ propagate to the output $\hat{v}$, through the transfer function $G_{vg}(s)$ and the output impedance $Z_{out}(s)$. If the disturbances $\hat{v}_g$ and $\hat{i}_{load}$ are known to have some maximum worst-case amplitude, then Eq. (9-1) can be used to compute the resulting worst-case open-loop variation in $\hat{v}$.

As described previously, the feedback loop of Fig. 9.2 can be used to reduce the influences of $\hat{v}_g$ and $\hat{i}_{load}$ on the output $\hat{v}$. To analyze this system, let us perturb and linearize its averaged signals about their quiescent operating points. Both the power stage and the control block diagram are perturbed and linearized:

$$v_{ref}(t) = V_{ref} + \hat{v}_{ref}(t) \tag{9-2}$$

$$v_e(t) = V_e + \hat{v}_e(t)$$

etc.

In a dc regulator system, the reference input is constant, so $\hat{v}_{ref}(t) = 0$. In a switching amplifier or dc-ac inverter, the reference input may contain an ac variation. In Fig. 9.4(a), the converter model of Fig. 9.3 is combined with the perturbed and linearized control circuit block diagram. This is equivalent to the reduced block diagram of Fig. 9.4(b), in which the converter model has been replaced by blocks representing Eq. (9-1).

Solution of Fig. 9.4(b) for the output voltage variation $\hat{v}$ yields

$$\hat{v} = \hat{v}_{ref}\frac{G_cG_{vd}/V_M}{1 + HG_cG_{vd}/V_M} + \hat{v}_g\frac{G_{vg}}{1 + HG_cG_{vd}/V_M} - \hat{i}_{load}\frac{Z_{out}}{1 + HG_cG_{vd}/V_M} \tag{9-3}$$

which can be written in the form

$$\hat{v} = \hat{v}_{ref}\frac{1}{H}\frac{T}{1+T} + \hat{v}_g\frac{G_{vg}}{1+T} - \hat{i}_{load}\frac{Z_{out}}{1+T} \tag{9-4}$$

with $T(s) = H(s)G_c(s)G_{vd}(s) / V_M$ = "loop gain"

Equation (9-4) is a general result. The loop gain $T(s)$ is defined in general as the product of the gains around the forward and feedback paths of the loop. This equation shows how the addition of a feedback loop modifies the transfer functions and performance of the system, as described in detail below.

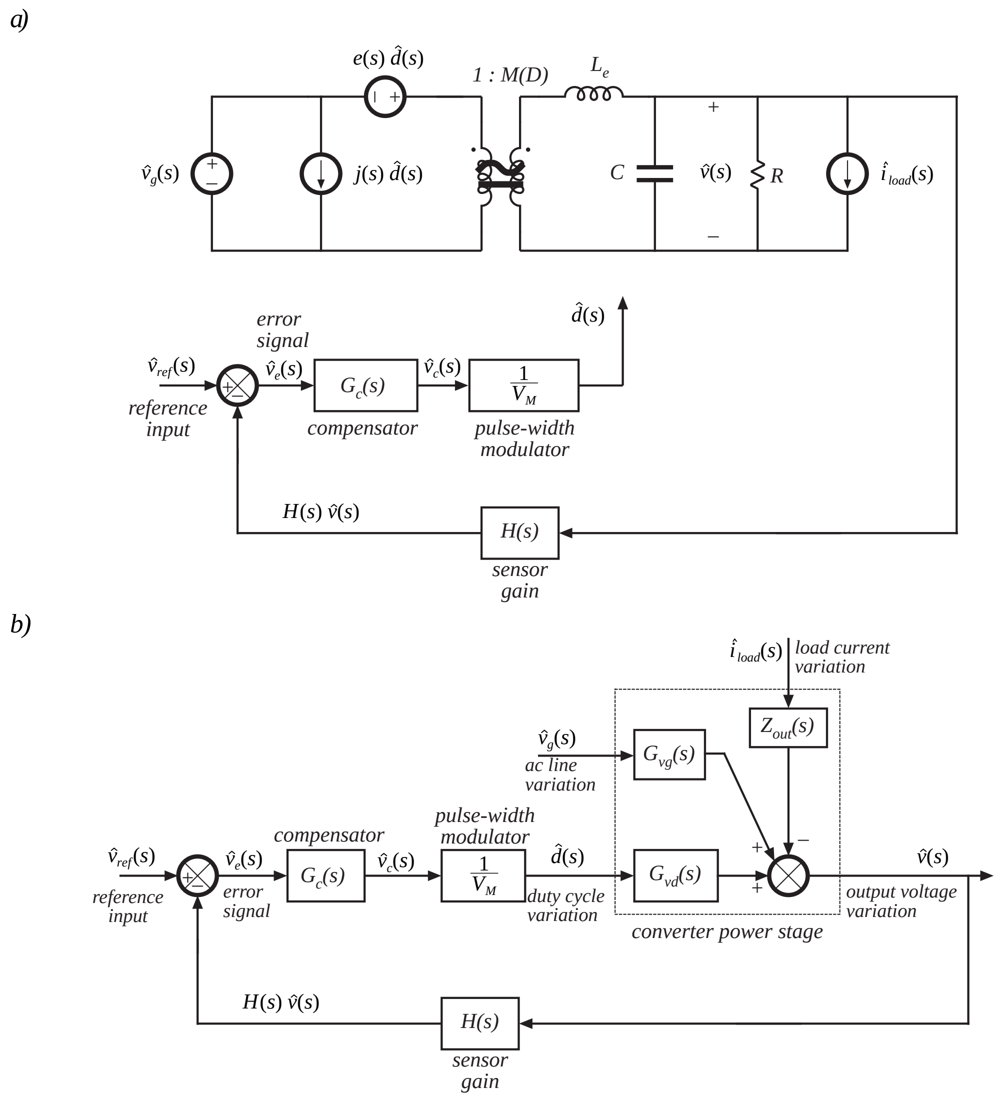

Fig. 9.4. Voltage regulator system small-signal model: (a) with converter equivalent circuit; (b) complete block diagram.

9.2.1. *Feedback reduces the transfer functions from disturbances to the output*

The transfer function from $\hat{v}_g$ to $\hat{v}$ in the open-loop buck converter of Fig. 9.3 is $G_{vg}(s)$, as given in Eq. (9-1). When feedback is added, this transfer function becomes

$$\left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\substack{\hat{v}_{ref}=0 \\ \hat{i}_{load}=0}} = \frac{G_{vg}(s)}{1+T(s)} \tag{9-5}$$

from Eq. (9-4). So this transfer function is reduced via feedback by the factor $1/(1+T(s))$. If the loop gain $T(s)$ is large in magnitude, then the reduction can be substantial. Hence, the output voltage variation $\hat{v}$ resulting from a given $\hat{v}_g$ variation is attenuated by the feedback loop.

Equation (9-4) also predicts that the converter output impedance is reduced, from $Z_{out}(s)$ to

$$\left.\frac{\hat{v}(s)}{-\hat{i}_{load}(s)}\right|_{\substack{\hat{v}_{ref}=0\\ \hat{v}_g=0}} = \frac{Z_{out}(s)}{1+T(s)} \tag{9-6}$$

So the feedback loop also reduces the converter output impedance by a factor of $1/(1+T(s))$, and the influence of load current variations on the output voltage is reduced.

9.2.2. Feedback causes the transfer function from the reference input to the output to be insensitive to variations in the gains in the forward path of the loop

According to Eq. (9-4), the closed-loop transfer function from $\hat{v}_{ref}(t)$ to $\hat{v}$ is

$$\left.\frac{\hat{v}(s)}{\hat{v}_{ref}(s)}\right|_{\substack{\hat{v}_g=0\\ \hat{i}_{load}=0}} = \frac{1}{H(s)}\,\frac{T(s)}{1+T(s)} \tag{9-7}$$

If the loop gain is large in magnitude, i.e., $\| T \| >> 1$, then $(1+T) \approx T$ and $T/(1+T) \approx T/T = 1$. The transfer function then becomes

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} \approx \frac{1}{H(s)} \tag{9-8}$$

which is independent of $G_c(s)$, V_M, and $G_{vd}(s)$. So provided that the loop gain is large in magnitude, then variations in $G_c(s)$, V_M, and $G_{vd}(s)$ have negligible effect on the output voltage. Of course, in the dc regulator application, v_{ref} is constant and $\hat{v}_{ref}(t) = 0$. But Eq. (9-8) applies equally well to the dc values. For example, if the system is linear, then we can write

$$\frac{V}{V_{ref}} = \frac{1}{H(0)}\,\frac{T(0)}{1+T(0)} \approx \frac{1}{H(0)} \tag{9-9}$$

So to make the dc output voltage V accurately follow the dc reference V_{ref}, we need only ensure that the dc sensor gain $H(0)$ and dc reference V_{ref} are well-known and accurate, and that $T(0)$ is large. Precision resistors are normally used to realize H, but components with tightly-controlled values need not be used in G_c, the pulse-width modulator, or the power stage. The sensitivity of the output voltage to the gains in the forward path is reduced, while the sensitivity of v to the feedback gain H and the reference input v_{ref} is increased.

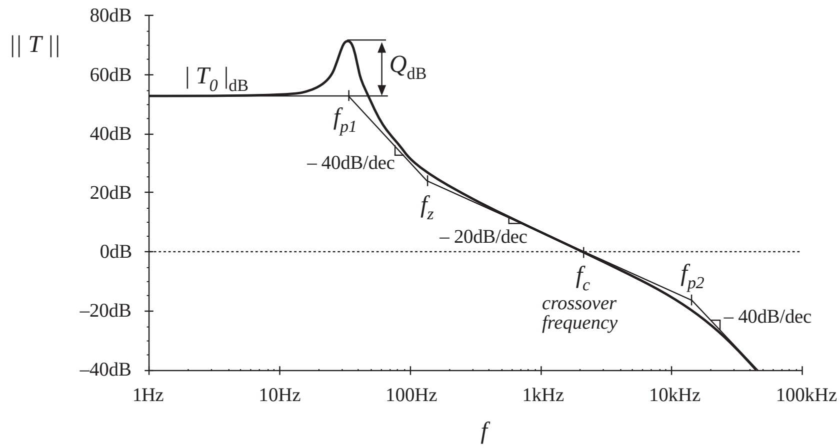

Fig. 9.5. Magnitude of the loop gain example, Eq. (9-10).

9.3. Construction of the important quantities *1/(1+T)* and *T/(1+T)* and the closed-loop transfer functions

The transfer functions in Eqs. (9-4) – (9-9) can be easily constructed using the algebra-on-the-graph method [4]. Let us assume that we have analyzed the blocks in our feedback system, and have plotted the Bode diagram of $\| T(s) \|$. To use a concrete example, suppose that the result is given in Fig. 9.5, for which $T(s)$ is

$$T(s) = T_0 \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{Q\omega_{p1}} + \left(\frac{s}{\omega_{p1}}\right)^2\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \tag{9-10}$$

This example appears somewhat complicated. But the loop gains of practical voltage regulators are often even more complex, and may contain four, five, or more poles. Evaluation of Eqs. (9-5) - (9-7), to determine the closed-loop transfer functions, requires quite a bit of work. The loop gain T must be added to 1, and the resulting numerator and denominator must be re-factored. Using this approach, it is difficult to obtain physical insight into the relationship between the closed-loop transfer functions and the loop gain. In consequence, design of the feedback loop to meet specifications is difficult.

Using the algebra-on-the-graph method, the closed-loop transfer functions can be constructed by inspection, and hence the relation between these transfer functions and the loop gain becomes obvious. Let us first investigate how to plot $\| T/(1+T) \|$. It can be seen from Fig. 9.5 that there is a frequency f_c, called the “crossover frequency”, where $\| T \| = 1$. At frequencies less than f_c, $\| T \| > 1$; indeed, $\| T \| >> 1$ for $f << f_c$. Hence, at low frequency, $(1+T) \approx T$, and $T/(1+T) \approx T/T = 1$. At frequencies greater than f_c, $\| T \| < 1$, and $\| T \| << 1$ for $f >> f_c$. So at high frequency, $(1+T) \approx 1$ and $T/(1+T) \approx T/1 = T$. So we have

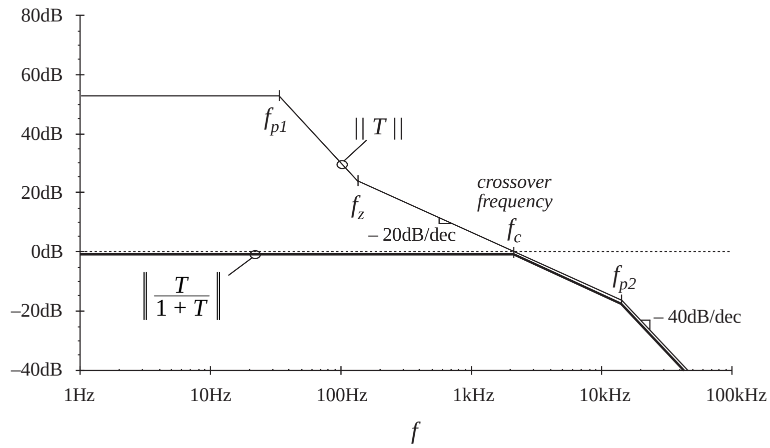

Fig. 9.6. Graphical construction of the asymptotes of $\| T / (1 + T) \|$. Exact curves are omitted.

$$\frac{T}{1+T} \approx \begin{cases} 1 & for \; \| T \| >> 1 \\ T & for \; \| T \| << 1 \end{cases} \tag{9-11}$$

The asymptotes corresponding to Eq. (9-11) are relatively easy to construct. The low-frequency asymptote, for $f < f_c$, is 1 or 0dB. The high-frequency asymptotes, for $f > f_c$, follow T. The result is shown in Fig. 9.6.

So at low frequency, where $\| T \|$ is large, the reference-to-output transfer function is

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} = \frac{1}{H(s)} \frac{T(s)}{1+T(s)} \approx \frac{1}{H(s)} \tag{9-12}$$

This is the desired behavior, and the feedback loop works well at frequencies where $\| T \|$ is large. At high frequency ($f >> f_c$) where $\| T \|$ is small, the reference-to-output transfer function is

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} = \frac{1}{H(s)} \frac{T(s)}{1+T(s)} \approx \frac{T(s)}{H(s)} = \frac{G_c(s)G_{vd}(s)}{V_M} \tag{9-13}$$

This is not the desired behavior; in fact, this is the gain with the feedback connection removed ($H \to 0$). At high frequencies, the feedback loop is unable to reject the disturbance because the bandwidth of T is limited. The reference-to-output transfer function can be constructed on the graph by multiplying the $T/(1+T)$ asymptotes of Fig. 9.6 by $1/H$.

We can plot the asymptotes of $\| 1/(1+T) \|$ using similar arguments. At low frequencies where $\| T \| >> 1$, then $(1+T) \approx T$, and hence $1/(1+T) \approx 1/T$. At high frequencies where $\| T \| << 1$, then $(1+T) \approx 1$ and $1/(1+T) \approx 1$. So we have

$$\frac{1}{1+T(s)} \approx \begin{cases} \dfrac{1}{T(s)} & for \; \| T \| >> 1 \\ 1 & for \; \| T \| << 1 \end{cases} \tag{9-14}$$

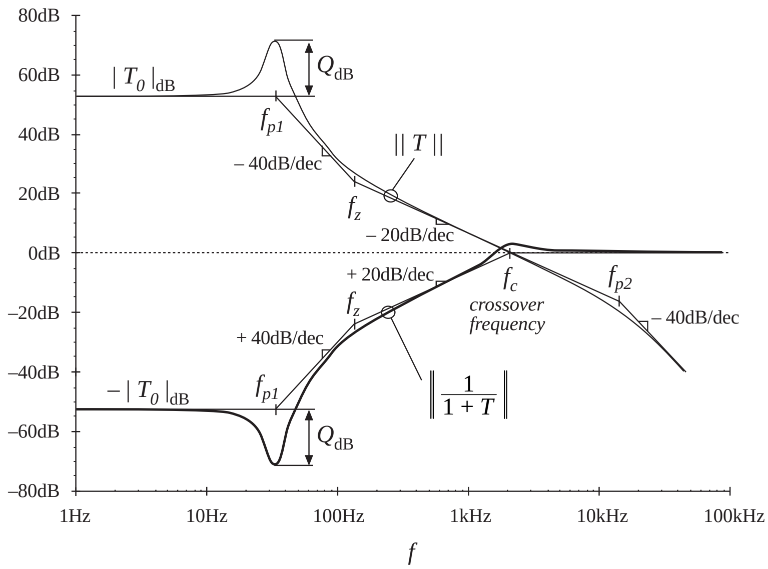

Fig. 9.7. Graphical construction of $\| 1 / (1 + T) \|$.

The asymptotes for the *T(s)* example of Fig. 9.5 are plotted in Fig. 9.7.

At low frequencies where $\| T \|$ is large, the disturbance transfer function from $\hat{v}_g$ to $\hat{v}$ is

$$\frac{\hat{v}(s)}{\hat{v}_g(s)} = \frac{G_{vg}(s)}{1 + T(s)} \approx \frac{G_{vg}(s)}{T(s)} \tag{9-15}$$

Again, $G_{vg}(s)$ is the original transfer function, with no feedback. The closed-loop transfer function has magnitude reduced by the factor $1/\| T \|$. So if, for example, we want to reduce this transfer function by a factor of 20 at 120Hz, then we need a loop gain $\| T \|$ of at least $20 \Rightarrow 26$dB at 120Hz. The disturbance transfer function from $\hat{v}_g$ to $\hat{v}$ can be constructed on the graph, by multiplying the asymptotes of Fig. 9.7 by the asymptotes for $G_{vg}(s)$.

Similar arguments apply to the output impedance. The closed-loop output impedance at low frequencies is

$$\frac{\hat{v}(s)}{-\hat{i}_{load}(s)} = \frac{Z_{out}(s)}{1 + T(s)} \approx \frac{Z_{out}(s)}{T(s)} \tag{9-16}$$

The output impedance is also reduced in magnitude by a factor of $1/\| T \|$ at frequencies below the crossover frequency.

At high frequencies ($f > f_c$) where $\| T \|$ is small, then $1/(1+T) \approx 1$, and

$$\frac{\hat{v}(s)}{\hat{v}_g(s)} = \frac{G_{vg}(s)}{1 + T(s)} \approx G_{vg}(s)$$

$$\frac{\hat{v}(s)}{-\hat{i}_{load}(s)} = \frac{Z_{out}(s)}{1 + T(s)} \approx Z_{out}(s) \tag{9-17}$$

This is the same as the original disturbance transfer function and output impedance. So the feedback loop has essentially no effect on the disturbance transfer functions at frequencies above the crossover frequency.

9.4. Stability

It is well known that adding a feedback loop can cause an otherwise stable system to become unstable. Even though the transfer functions of the original converter, Eq. (9-1), as well as of the loop gain $T(s)$, contain no right half-plane poles, it is possible for the closed-loop transfer functions of Eq. (9-4) to contain right half-plane poles. The feedback loop then fails to regulate the system at the desired quiescent operating point, and oscillations are usually observed. It is important to avoid this situation. And even when the feedback system is stable, it is possible for the transient response to exhibit undesirable ringing and overshoot. The stability problem is discussed in this section, and a method for ensuring that the feedback system is stable and well-behaved is explained.

When feedback destabilizes the system, the denominator $(1+T(s))$ terms in Eq. (9-4) contain roots in the right half-plane (i.e., with positive real parts). If $T(s)$ is a rational fraction, i.e., the ratio $N(s)/D(s)$ of two polynomial functions $N(s)$ and $D(s)$, then we can write

$$\frac{T(s)}{1+T(s)} = \frac{\frac{N(s)}{D(s)}}{1+\frac{N(s)}{D(s)}} = \frac{N(s)}{N(s)+D(s)}$$
$$\frac{1}{1+T(s)} = \frac{1}{1+\frac{N(s)}{D(s)}} = \frac{D(s)}{N(s)+D(s)} \qquad (9\text{-}18)$$

So $T(s)/(1+T(s))$ and $1/(1+T(s))$ contain the same poles, given by the roots of the polynomial $(N(s) + D(s))$. A brute-force test for stability is to evaluate $(N(s) + D(s))$, and factor the result to see whether any of the roots have positive real parts. However, for all but very simple loop gains, this involves a great deal of work. A simpler method is given by the Nyquist stability theorem, in which the number of right half-plane roots of $(N(s) + D(s))$ can be determined by testing $T(s)$ [1,2]. This theorem is not discussed here. However, a special case of the theorem known as the phase margin test is sufficient for designing most voltage regulators, and is discussed in this section.

9.4.1. The phase margin test

The crossover frequency f_c is defined as the frequency where the magnitude of the loop gain is unity:

$$\| T(j2\pi f_c) \| = 1 \Rightarrow 0\text{dB} \qquad (9\text{-}19)$$

To compute the phase margin φ_m, the phase of the loop gain T is evaluated at the crossover frequency, and 180˚ is added. Hence,

$$\varphi_m = 180^\circ + \angle T(j2\pi f_c) \qquad (9\text{-}20)$$

If there is exactly one crossover frequency, and if the loop gain $T(s)$ contains no right half-plane poles, then the quantities $1/(1+T)$ and $T/(1+T)$ contain no right half-plane poles when the phase margin defined in Eq. (9-20) is positive. Thus, using a simple test on $T(s)$, we can determine the stability of $T/(1+T)$ and $1/(1+T)$. This is an easy-to-use design tool —we simple ensure that the phase of T is greater than –180˚ at the crossover frequency.

When there are multiple crossover frequencies, the phase margin test may be ambiguous. Also, when T contains right half-plane poles (i.e., the original open-loop system is unstable), then the phase margin test cannot be used. In either case, the more general Nyquist stability theorem must be employed.

The loop gain of a typical stable system is shown in Fig. 9.8. It can be seen that $\angle T(j2\pi f_c) = -112^\circ$. Hence, $\varphi_m = 180^\circ - 112^\circ = +68^\circ$. Since the phase margin is positive, $T/(1+T)$ and $1/(1+T)$ contain no right half-plane poles, and the feedback system is stable.

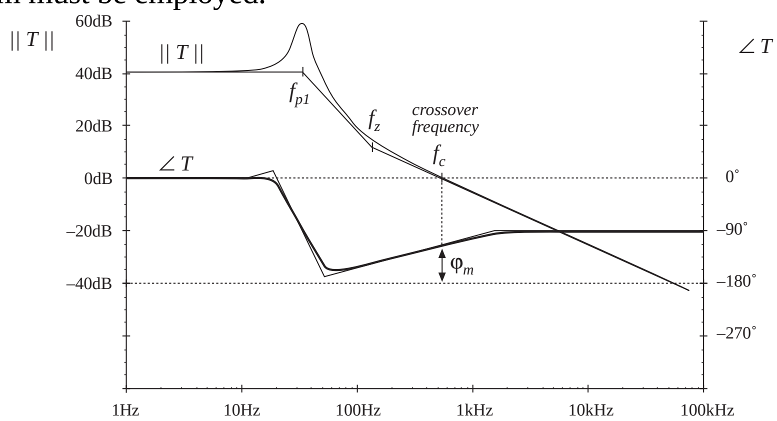

Fig. 9.8. Magnitude and phase of the loop gain of a stable system. The phase margin φ_m is positive.

The loop gain of an unstable system is sketched in Fig. 9.9. For this example, $\angle T(j2\pi f_c) = -230^\circ$. The phase margin is $\varphi_m = 180^\circ - 230^\circ = -50^\circ$. The negative phase margin implies that $T/(1+T)$ and $1/(1+T)$ each contain at least one right half-plane pole.

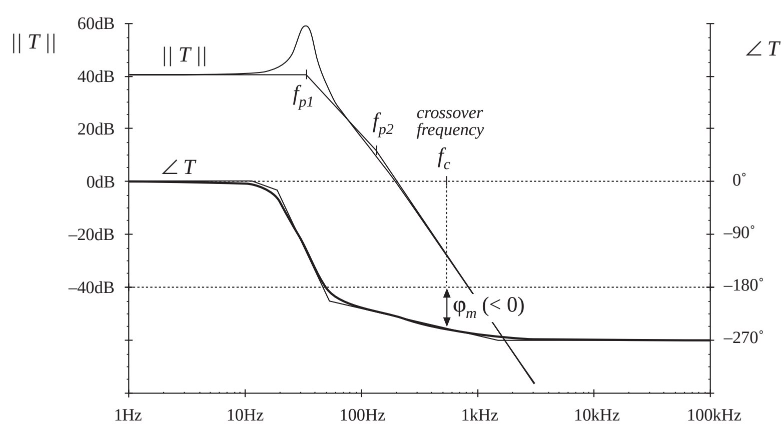

Fig. 9.9. Magnitude and phase of the loop gain of an unstable system. The phase margin φ_m is negative.

9.4.2. *The relation between phase margin and closed-loop damping factor*

How much phase margin is necessary? Is a worst-case phase margin of 1˚ satisfactory? Of course, good designs should have adequate design margins, but there is another important reason why additional phase margin is needed. A small phase margin (in T) causes the closed-loop transfer functions $T/(1+T)$ and $1/(1+T)$ to exhibit resonant poles with high Q in the vicinity of the crossover frequency. The system transient response exhibits overshoot and ringing. As the phase margin is reduced these characteristics become worse (higher Q, longer ringing) until, for $\varphi_m \le 0˚$, the system becomes unstable.

Let us consider a loop gain $T(s)$ which is well-approximated, in the vicinity of the crossover frequency, by the following function:

$$T(s) = \frac{1}{\left(\frac{s}{\omega_0}\right)\left(1+\frac{s}{\omega_2}\right)} \tag{9-21}$$

Magnitude and phase asymptotes are plotted in Fig. 9.10. This function is a good approximation near the crossover frequency for many common loop gains, in which $\| T \|$ approaches unity gain with a –20dB/decade slope, with an additional pole at frequency $f_2 = \omega_2/2\pi$. Any additional poles and zeroes are assumed to be sufficiently far above or below the crossover frequency, such that they have negligible effect on the system transfer functions near the crossover frequency.

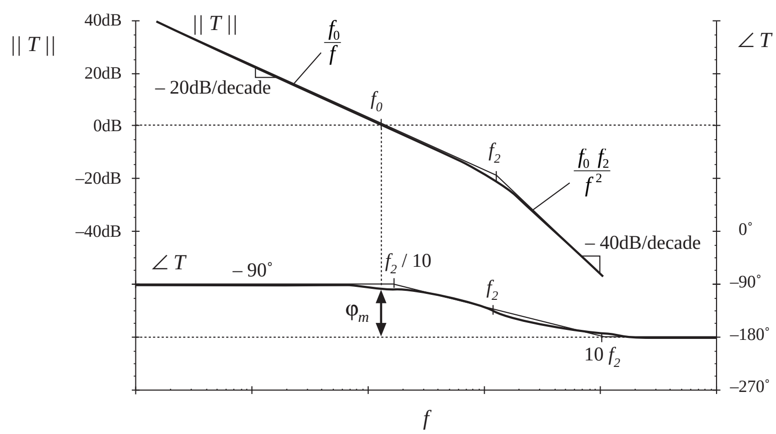

Fig. 9.10. Magnitude and phase asymptotes for the loop gain T of Eq. (9-21).

Note that, as $f_2 \to \infty$, the phase margin φ_m approaches 90˚. As $f_2 \to 0$, $\varphi_m \to 0˚$. So as f_2 is reduced, the phase margin is also reduced. Let's investigate how this affects the closed-loop response via $T/(1+T)$. We can write

$$\frac{T(s)}{1+T(s)} = \frac{1}{1+\frac{1}{T(s)}} = \frac{1}{1+\frac{s}{\omega_0}+\frac{s^2}{\omega_0\omega_2}} \tag{9-22}$$

using Eq. (9-21). By putting this into standard quadratic form, one obtains

$$\frac{T(s)}{1+T(s)} = \frac{1}{1+\frac{s}{Q\omega_c}+\left(\frac{s}{\omega_c}\right)^2} \tag{9-23}$$

where $$\omega_c = \sqrt{\omega_0 \omega_2} = 2\pi f_c$$
$$Q = \frac{\omega_0}{\omega_c} = \sqrt{\frac{\omega_0}{\omega_2}}$$

So the closed-loop response contains quadratic poles at f_c, the geometric mean of f_0 and f_2. These poles have a low Q-factor when $f_0 << f_2$. In this case, we can use the low-Q approximation to estimate their frequencies:

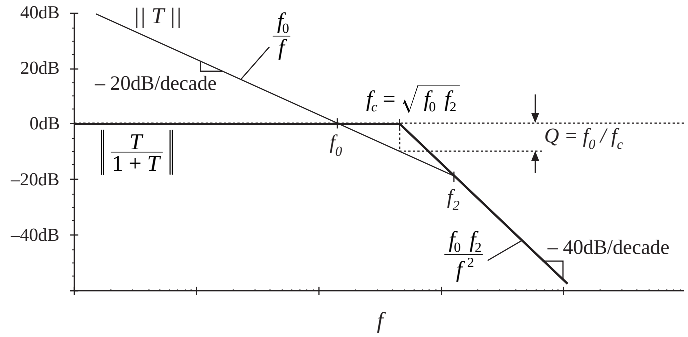

Fig. 9.11. Construction of magnitude asymptotes of the closed-loop transfer function $T / (1 + T)$, for the low-Q case.

$$Q\,\omega_c = \omega_0$$
$$\frac{\omega_c}{Q} = \omega_2 \qquad (9\text{-}24)$$

Magnitude asymptotes are plotted in Fig. 9.11 for this case. It can be seen that these asymptotes conform to the rules of section 9.3 for constructing $T/(1+T)$ by the algebra-on-the-graph method.

Next consider the high-Q case. When the pole frequency f_2 is reduced, reducing the phase margin, then the Q-factor given by Eq. (9-23) is increased. For $Q > 0.5$, resonant poles occur at frequency f_c. The magnitude Bode plot for the case $f_2 < f_0$ is given in Fig. 9.12. The frequency f_c continues to be the geometric mean of f_2 and f_0, and f_c now coincides with the crossover (unity-gain) frequency of the $\| T \|$ asymptotes. The exact value of the closed-loop gain $T/(1+T)$ at frequency f_c is equal to $Q = f_0/f_c$. As shown in Fig. 9.12, this is identical to the value of the low-frequency –20dB/decade asymptote (f_0/f), evaluated at frequency f_c. It can be seen that the Q-factor becomes very large as the pole frequency f_2 is reduced.

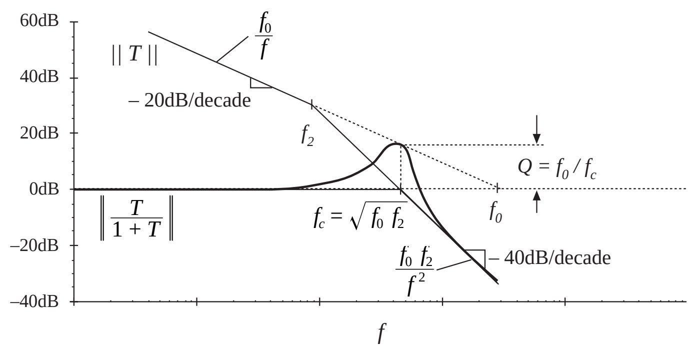

Fig. 9.12. Construction of magnitude asymptotes of the closed-loop transfer function $T / (1 + T)$, for the high-Q case.

The asymptotes of Fig. 9.12 also follow the algebra-on-the-graph rules of section 9.3, but the deviation of the exact curve from the asymptotes is not predicted by the algebra-on-the-graph method. These two poles with Q-factor appear in both $T/(1+T)$ and $1/(1+T)$. We need an easy way to predict the Q-factor. We can obtain such a relation by finding the frequency at which the magnitude of T is exactly equal to unity. We then

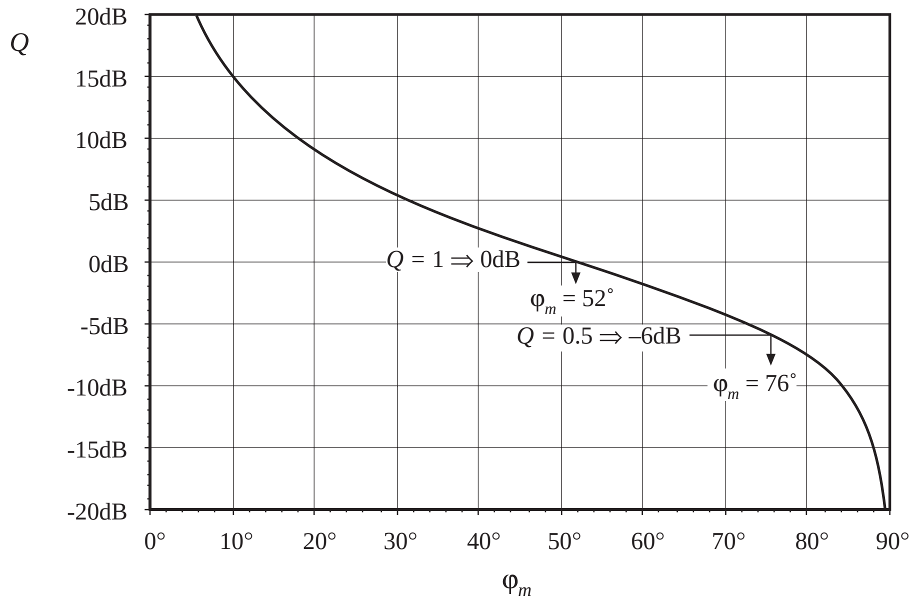

Fig. 9.13. Relation between loop gain phase margin φ_m and closed-loop peaking factor Q.

evaluate the exact phase of T at this frequency, and compute the phase margin. This phase margin is a function of the ratio f_0/f_2, or Q^2. We can then solve to find Q as a function of the phase margin. The result is

$$Q = \frac{\sqrt{\cos \varphi_m}}{\sin \varphi_m}$$

$$\varphi_m = \tan^{-1}\sqrt{\frac{1+\sqrt{1+4Q^4}}{2Q^4}} \tag{9-25}$$

This function is plotted in Fig. 9.13, with Q expressed in dB. It can be seen that obtaining real poles (Q < 0.5) requires a phase margin of at least 76˚. To obtain Q = 1, a phase margin of 52˚ is needed. The system with a phase margin of 1˚ exhibits a closed-loop response with very high Q! With a small phase margin, $T(j\omega)$ is very nearly equal to –1 in the vicinity of the crossover frequency. The denominator (1+T) then becomes very small, causing the closed-loop transfer functions to exhibit a peaked response at frequencies near the crossover frequency f_c.

Figure 9.13 is the result for the simple loop gain defined by Eq. (9-21). However, this loop gain is a good approximation for many other loop gains that are encountered in practice, in which $\| T \|$ approaches unity gain with a –20dB/decade slope, with an additional pole at frequency f_2. If all other poles and zeroes of $T(s)$ are sufficiently far above or below the crossover frequency, then they have negligible effect on the system transfer functions near the crossover frequency, and Fig. 9.13 gives a good approximation for the relation between φ_m and Q.

Another common case is the one in which ‖ T ‖ approaches unity gain with a –40dB/decade slope, with an additional zero at frequency f_2. As f_2 is increased, the phase margin is decreased and Q is increased. It can be shown that the relation between φ_m and Q is exactly the same, Eq. (9-25).

A case where Fig. 9.13 fails is when the loop gain $T(s)$ three or more poles at or near the crossover frequency. The closed-loop response then also contains three or more poles near the crossover frequency, and these poles cannot be completely characterized by a single Q-factor. Additional work is required to find the behavior of the exact $T/(1+T)$ and $1/(1+T)$ near the crossover frequency, but nonetheless it can be said that a small phase margin leads to a peaked closed-loop response.

9.4.3. *Transient response vs. damping factor*

One can solve for the unit-step response of the $T/(1+T)$ transfer function, by multiplying Eq. (9-23) by $1/s$ and then taking the inverse Laplace transform. The result for $Q > 0.5$ is

$$\hat{v}(t) = 1 + \frac{2Q\, e^{-\omega_c t/2Q}}{\sqrt{4Q^2-1}} \sin\left[\frac{\sqrt{4Q^2-1}}{2Q}\,\omega_c\, t + \tan^{-1}\left(\sqrt{4Q^2-1}\right)\right] \qquad (9\text{-}26)$$

For $Q < 0.5$, the result is

$$\hat{v}(t) = 1 - \frac{\omega_2}{\omega_2-\omega_1}\, e^{-\omega_1 t} - \frac{\omega_1}{\omega_1-\omega_2}\, e^{-\omega_2 t} \qquad (9\text{-}27)$$

with $$\omega_1,\, \omega_2 = \frac{\omega_c}{2Q}\left(1 \pm \sqrt{1-4Q^2}\right)$$

These equations are plotted in Fig. 9.14 for various values of Q.

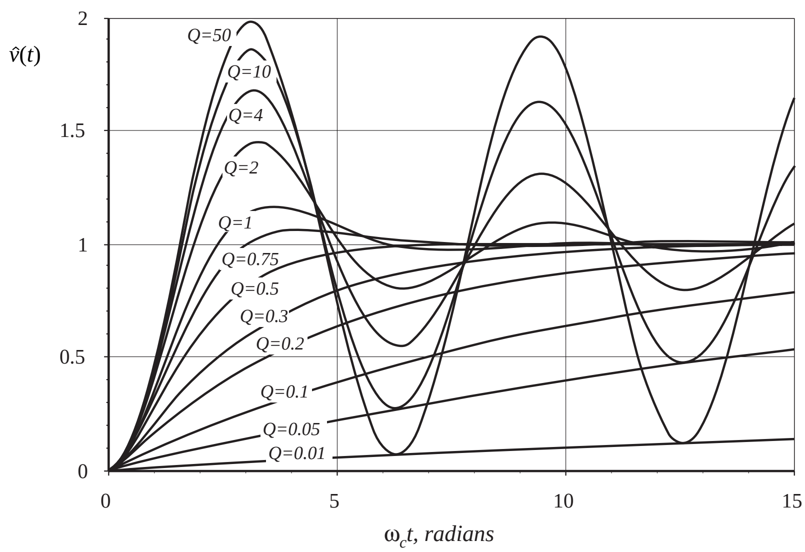

Fig. 9.14. Unit-step response of the second-order system, Eqs. (9-26) and (9-27), for various values of Q.

According to Eq. (9-23), when $f_2 > 4f_0$, the Q-factor is less than 0.5, and the closed-loop response contains a low-frequency and a high-frequency real pole. The transient response in this case, Eq. (9-27), contains decaying-exponential functions of time, of the form

$$Ae^{(pole)\,t} \tag{9-28}$$

This is called the "overdamped" case. With very low Q, the low-frequency pole leads to a slow step response.

For $f_2 = 4f_0$, the Q-factor is equal to 0.5. The closed-loop response contains two real poles at frequency $2f_0$. This is called the "critically damped" case. The transient response is faster than in the overdamped case, because the lowest-frequency pole is at a higher frequency. This is the fastest response that does not exhibit overshoot. At $\omega_c t = \pi$ radians ($t = 1/2f_c$), the voltage has reached 82% of its final value. At $\omega_c t = 2\pi$ radians ($t = 1/f_c$), the voltage has reached 98.6% of its final value.

For $f_2 < 4f_0$, the Q-factor is greater than 0.5. The closed-loop response contains complex poles, and the transient response exhibits sinusoidal-type waveforms with decaying amplitude, Eq. (9-26). The rise time of the step response is faster than in the critically-damped case, but the waveforms exhibit overshoot. The peak value of $\hat{v}(t)$ is

$$peak\ \hat{v}(t) = 1 + e^{-\pi/\sqrt{4Q^2-1}} \tag{9-29}$$

This is called the "underdamped" case. A Q-factor of 1 leads to an overshoot of 16.3%, while a Q-factor of 2 leads to a 44.4% overshoot. Large Q-factors lead to overshoots approaching 100%.

The exact transient response of the feedback loop may differ from the plots of Fig. 9.14, because of additional poles and zeroes in T, and because of differences in initial conditions. Nonetheless, Fig. 9.14 illustrates how high-Q poles lead to overshoot and ringing. In most power applications, overshoot is unacceptable. For example, in a 5V computer power supply, the voltage must not be allowed to overshoot to 7 or 10 volts when the supply is turned on —this would destroy all of the TTL integrated circuits in the computer! So the Q-factor must be sufficiently low, often 0.5 or less, corresponding to a phase margin of at least 76˚.

9.5. Regulator design

Let's now consider how to design a regulator system, to meet specifications or design goals regarding rejection of disturbances, transient response, and stability. Typical dc regulator designs are defined using specifications such as the following:

(1) Effect of load current variations on the output voltage regulation. The output voltage must remain within a specified range when the load current varies in a prescribed way. This amounts to a limit on the maximum magnitude of the closed-loop output impedance of Eq. (9-6), repeated below

$$\left.\frac{\hat{v}(s)}{-\hat{i}_{load}(s)}\right|_{\substack{\hat{v}_{ref}=0 \\ \hat{v}_g=0}} = \frac{Z_{out}(s)}{1+T(s)} \qquad \text{(9-30)}$$

If, over some frequency range, the open-loop output impedance Z_{out} has magnitude which exceeds the limit, then the loop gain T must be sufficiently large in magnitude over the same frequency range, such that the magnitude of the closed-loop output impedance given in Eq. (9-30) is less than the given limit.

(2) Effect of input voltage variations (for example, at the second harmonic of the ac line frequency) on the output voltage regulation. Specific maximum limits are usually placed on the amplitude of variations in the output voltage at the second harmonic of the ac line frequency (120Hz or 100Hz). If we know the magnitude of the rectification voltage ripple which appears at the converter input (as $\hat{v}_g$), then we can calculate the resulting output voltage ripple (in $\hat{v}$) using the closed loop line-to-output transfer function of Eq. (9-5), repeated below

$$\left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\substack{\hat{v}_{ref}=0 \\ \hat{i}_{load}=0}} = \frac{G_{vg}(s)}{1+T(s)} \qquad \text{(9-31)}$$

The output voltage ripple can be reduced by increasing the magnitude of the loop gain at the ripple frequency. In a typical good design, $\| T \|$ is 20dB or more at 120Hz, so that the transfer function of Eq. (9-31) is at least an order of magnitude smaller than the open-loop line-to-output transfer function $\| G_{vg} \|$.

(3) Transient response time. When a specified large disturbance occurs, such as a large step change in load current or input voltage, the output voltage may undergo a transient. During this transient, the output voltage typically deviates from its specified allowable range. Eventually, the feedback loop operates to return the output voltage within tolerance. The time required to do so is the transient response time; typically, the response time can be shortened by increasing the feedback loop crossover frequency.

(4) Overshoot and ringing. As discussed in section 9.4.3, the amount of overshoot and ringing allowed in the transient response may be limited. Such a specification implies that the phase margin must be sufficiently large.

Each of these requirements imposes constraints on the loop gain $T(s)$. Therefore, the design of the control system involves modifying the loop gain. As illustrated in Fig.

9.2, a compensator network is added for this purpose. Several well-known strategies for design of the compensator transfer function $G_c(s)$ are discussed below.

9.5.1. Lead (PD) compensator

This type of compensator transfer function is used to improve the phase margin. A zero is added to the loop gain, at a frequency f_z sufficiently far below the crossover frequency f_c, such that the phase margin of $T(s)$ is increased by the desired amount. The lead compensator is also called a proportional-plus-derivative, or PD, controller —at high frequencies, the zero causes the compensator to differentiate the error signal. It often finds application in systems originally containing a two-pole response. By use of this type of compensator, the bandwidth of the feedback loop (i.e., the crossover frequency f_c) can be extended while maintaining an acceptable phase margin.

A side effect of the zero is that it causes the compensator gain to increase with frequency, with a +20dB/decade slope. So steps must be taken to ensure that $\| T \|$ remains equal to unity at the desired crossover frequency. Also, since the gain of any practical amplifier must tend to zero at high frequency, the compensator transfer function $G_c(s)$ must contain high frequency poles. These poles also have the beneficial effect of attenuating high frequency noise. Of particular concern are the switching frequency harmonics present in the output voltage and feedback signals. If the compensator gain at the switching frequency is too great, then these switching harmonics are amplified by the compensator, and can disrupt the operation of the pulse-width modulator (see section 7.7). So the compensator network should contain poles at a frequency less than the switching frequency. These considerations typically restrict the crossover frequency f_c to be less than approximately 10% of the converter switching frequency f_s. In addition, the circuit designer must take care not to exceed the gain-bandwidth limits of available operational amplifiers.

The transfer function of the lead compensator therefore contains a low-frequency zero and several high-frequency poles. A simplified example containing a single high-frequency pole is given in Eq. (9-32) and illustrated in Fig. 9.15.

$$G_c(s) = G_{c0} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \qquad (9\text{-}32)$$

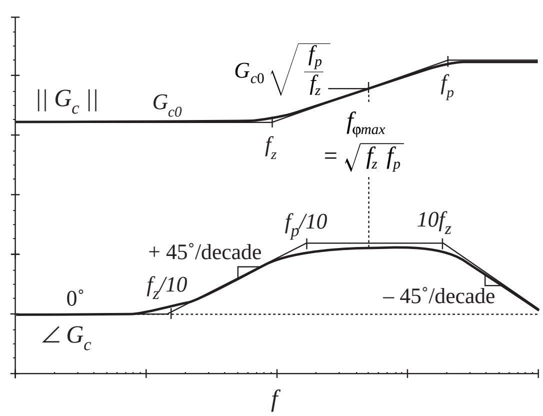

Fig. 9.15. Magnitude and phase asymptotes of the PD compensator transfer function G_c of Eq. (9-32).

The maximum phase occurs at a frequency $f_{\varphi max}$ given by the geometrical mean of the pole and zero frequencies:

$$f_{\varphi \max} = \sqrt{f_z f_p} \tag{9-33}$$

To obtain the maximum improvement in phase margin, we should design our compensator so that the frequency $f_{\varphi max}$ coincides with the loop gain crossover frequency f_c. The value of the phase at this frequency can be shown to be

$$\angle G_c(f_{\varphi \max}) = \tan^{-1}\left(\frac{\sqrt{\frac{f_p}{f_z}} - \sqrt{\frac{f_z}{f_p}}}{2}\right) \tag{9-34}$$

This equation is plotted in Fig. 9.16. Equation (9-34) can be inverted to obtain

$$\frac{f_p}{f_z} = \frac{1 + \sin\left(\theta\right)}{1 - \sin\left(\theta\right)} \tag{9-35}$$

where $\theta = \angle G_c(f_{\varphi max})$. Equations (9-34) and (9-32) imply that, to optimally obtain a compensator phase lead of θ at frequency f_c, the pole and zero frequencies should be chosen as follows:

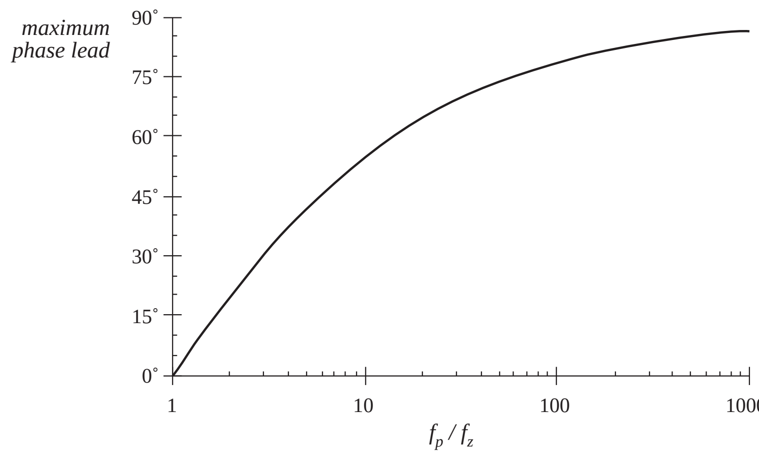

Fig. 9.16. Maximum phase lead θ vs. frequency ratio f_p / f_z for the lead compensator.

$$f_z = f_c \sqrt{\frac{1 - \sin\left(\theta\right)}{1 + \sin\left(\theta\right)}}$$
$$f_p = f_c \sqrt{\frac{1 + \sin\left(\theta\right)}{1 - \sin\left(\theta\right)}} \tag{9-36}$$

When it is desired to avoid changing the crossover frequency, the magnitude of the compensator gain is chosen to be unity at the loop gain crossover frequency f_c. This requires that G_{c0} be chosen according to the following formula:

$$G_{c0} = \sqrt{\frac{f_z}{f_p}} \tag{9-37}$$

It can be seen that G_{c0} is less than unity, and therefore the lead compensator reduces the dc gain of the feedback loop. Other choices of G_{c0} can be selected when it is desired to shift the crossover frequency f_c; for example, increasing the value of G_{c0} causes the crossover frequency to increase. If the frequencies f_p and f_z are chosen as in Eq. (9-36), then $f_{\varphi max}$ of Eq. (9-32) will coincide with the new crossover frequency f_c.

The Bode diagram of a typical loop gain $T(s)$ containing two poles is illustrated in Fig. 9.17. The phase margin of the original $T(s)$ is small, since the crossover frequency f_c is substantially greater than the pole frequency f_0. The result of adding a lead compensator is also illustrated. The lead compensator of this example is designed to maintain the same crossover frequency but improve the phase margin.

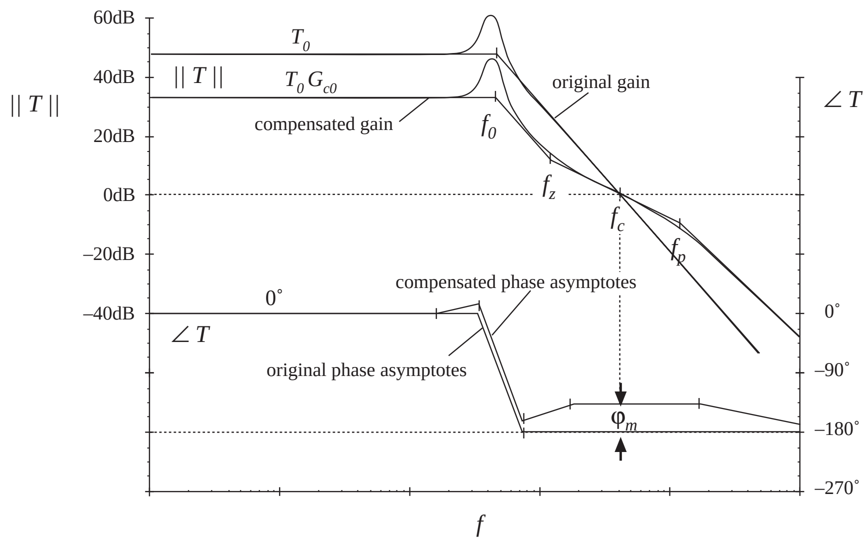

Fig. 9.17. Compensation of a loop gain containing two poles, using a lead (PD) compensator. The phase margin φ_m is improved.

9.5.2. Lag (PI) compensator

This type of compensator is used to increase the low-frequency loop gain, such that the output is better regulated at dc and at frequencies well below the loop crossover frequency. As given in Eq. (9-38) and illustrated in Fig. 9.18, an inverted zero is added to the loop gain, at frequency f_L.

$$G_c(s) = G_{c\infty}\left(1 + \frac{\omega_L}{s}\right) \tag{9-38}$$

If f_L is sufficiently lower than the loop crossover frequency f_c, then the phase margin is unchanged. This type of compensator is also called a proportional-plus-integral, or PI, controller —at low frequencies, the inverted zero causes the compensator to integrate the error signal.

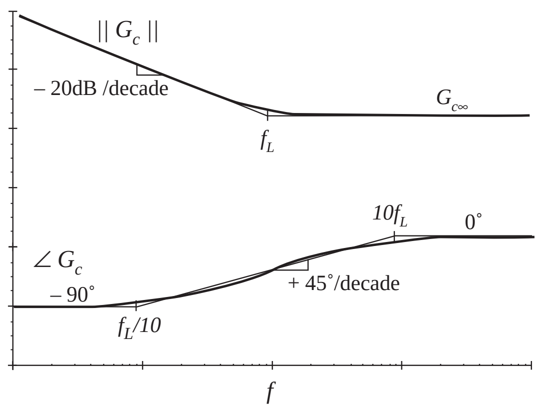

Fig. 9.18. Magnitude and phase asymptotes of the PI compensator transfer function G_c of Eq. (9-38).

To the extent that the compensator gain can be made arbitrarily large at dc, the dc loop gain $T(0)$ becomes arbitrarily large. This causes the dc component of the error signal to approach zero. In consequence, the steady-state output voltage is perfectly regulated, and the disturbance-to-output transfer functions approach zero at dc. Such behavior is easily obtained in practice, with the compensator of Eq. (9-38) realized using a conventional operational amplifier.

Although the PI compensator is useful in nearly all types of feedback systems, it is an especially simple and effective approach for systems originally containing a single pole. For the example of Fig. 9.19, the original uncompensated loop gain is of the form

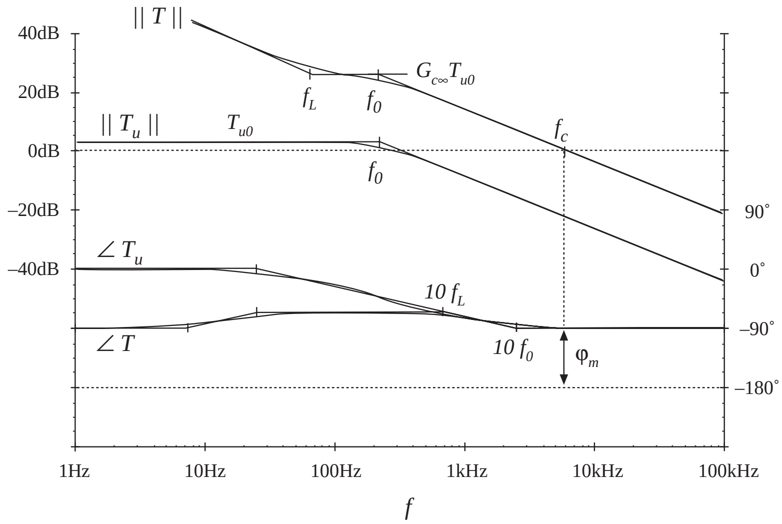

Fig. 9.19. Compensation of a loop gain containing a single pole, using a lag (PI) compensator. The loop gain magnitude is increased.

$$T_u(s) = \frac{T_{u0}}{\left(1 + \frac{s}{\omega_0}\right)} \tag{9-39}$$

The compensator transfer function of Eq. (9-38) is used, so that the compensated loop gain is $T(s) = T_u(s)\ G_c(s)$. Magnitude and phase asymptotes of $T(s)$ are also illustrated in Fig. 9.19. The compensator high-frequency gain $G_{c\infty}$ is chosen to obtain the desired crossover frequency f_c. If we approximate the compensated loop gain by its high-frequency asymptote, then at high frequencies we can write

$$\| T \| \approx \frac{T_{u0}G_{c\infty}}{\left(\frac{f}{f_0}\right)} \tag{9-40}$$

At the crossover frequency $f = f_c$, the loop gain has unity magnitude. Equation (9-40) predicts that the crossover frequency is

$$f_c \approx T_{u0}G_{c\infty}f_0 \tag{9-41}$$

Hence, to obtain a desired crossover frequency f_c, we should choose the compensator gain $G_{c\infty}$ as follows:

$$G_{c\infty} = \frac{f_c}{T_{u0}\ f_0} \tag{9-42}$$

The corner frequency f_L is then chosen to be sufficiently less than f_c, such that an adequate phase margin is maintained.

Magnitude asymptotes of the quantity 1 / (1 + $T(s)$) are constructed in Fig. 9.20. At frequencies less than f_L, the PI compensator improves the rejection of disturbances. At dc, where the magnitude of G_c approaches infinity, the magnitude of $1 / (1 + T)$ tends to zero. Hence, the closed-loop disturbance-to-output transfer functions, such as Eqs. (9-30) and (9-31), tend to zero at dc.

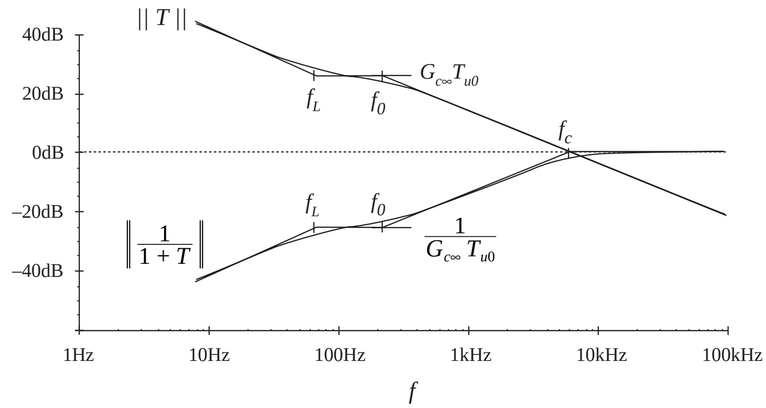

Fig. 9.20. Construction of $\| 1 / (1 + T) \|$ for the PI-compensated example of Fig. 9.19.

9.5.3. Combined (PID) compensator

The advantages of the lead and lag compensators can be combined, to obtain both wide bandwidth and zero steady-state error. At low frequencies, the compensator integrates the error signal, leading to large low-frequency loop gain and accurate regulation of the low-frequency components of the output voltage. At high frequency (in the vicinity of the crossover frequency), the compensator introduces phase lead into the loop gain, improving the phase margin. Such a compensator is sometimes called a PID controller.

A typical Bode diagram of a practical version of this compensator is illustrated in Fig. 9.21. The compensator has transfer function

$$G_c(s) = G_{cm} \frac{\left(1 + \frac{\omega_L}{s}\right)\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \qquad (9\text{-}43)$$

The inverted zero at frequency f_L functions in the same manner as the PI compensator. The zero at frequency f_z adds phase lead in the vicinity of the crossover frequency, as in the PD compensator. The high-frequency poles at frequencies f_{p1} and f_{p2} must be present in practical compensators, to cause the gain to roll

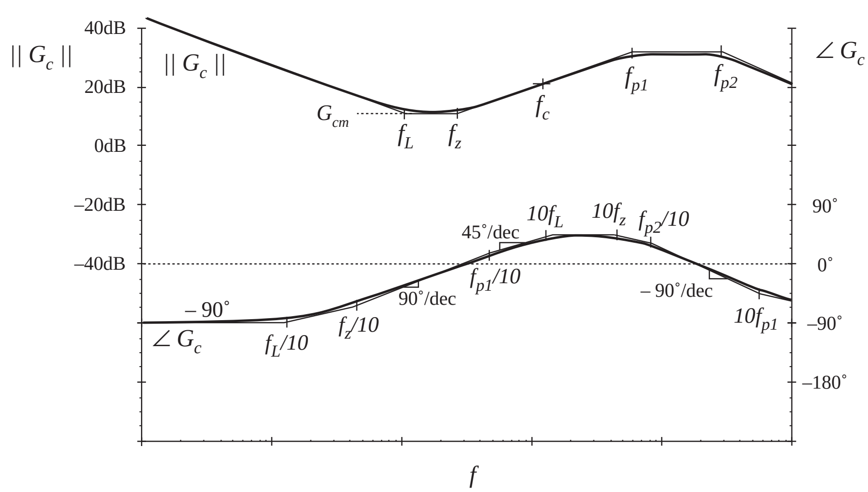

Fig. 9.21. Magnitude and phase asymptotes of the combined (PID) compensator transfer function G_c of Eq. (9-43).

off at high frequencies and to prevent the switching ripple from disrupting the operation of the pulse-width modulator. The loop gain crossover frequency f_c is chosen to be greater than f_L and f_z, but less than f_{p1} and f_{p2}.

9.5.4. Design example

To illustrate the design of PI and PD compensators, let us consider the design of a combined PID compensator for the dc-dc buck converter system of Fig. 9.22. The input voltage $v_g(t)$ for this system has nominal value 28V. It is desired to supply a regulated 15V to a 5A load. The load is modeled here with a 3Ω resistor. An accurate 5V reference is available.

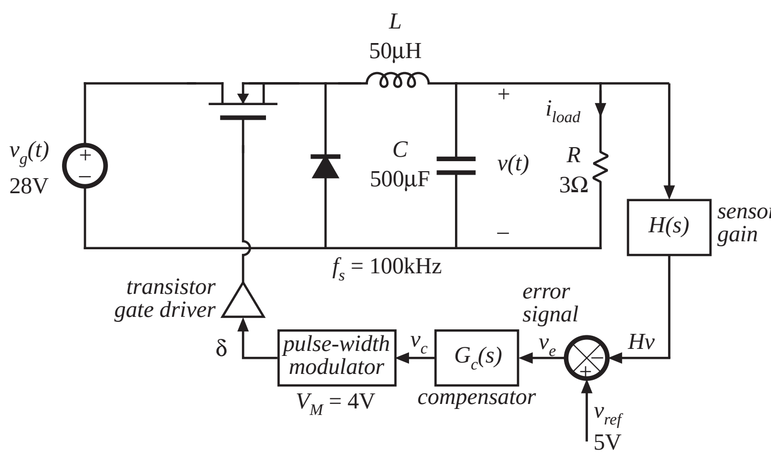

Fig. 9.22. Design example.

The first step is to select the feedback gain *H(s)*. The gain *H* is chosen such that the regulator produces a regulated 15V dc output. Let us assume that we will succeed in designing a good feedback system, which causes the output voltage to accurately follow the reference voltage. This is accomplished via a large loop gain *T*, which leads to a small error voltage: $v_e \approx 0$. Hence, $Hv \approx v_{ref}$. So we should choose

$$H = \frac{V_{ref}}{V} = \frac{5}{15} = \frac{1}{3} \tag{9-44}$$

The quiescent duty cycle is given by the steady-state solution of the converter:

$$D = \frac{V}{V_g} = \frac{15}{28} = 0.536 \tag{9-45}$$

The quiescent value of the control voltage, V_c, must satisfy Eq. (7-135). Hence,

$$V_c = DV_M = 2.14 \text{ V} \tag{9-46}$$

Thus, the quiescent conditions of the system are known. It remains to design the compensator gain $G_c(s)$.

A small-signal ac model of the regulator system is illustrated in Fig. 9.23. The buck converter ac model is represented in canonical form. Disturbances in the input voltage and in the load current are modeled. For generality, reference voltage variations $\hat{v}_{ref}$ are included in the diagram; in a dc voltage regulator, these variations are normally zero.

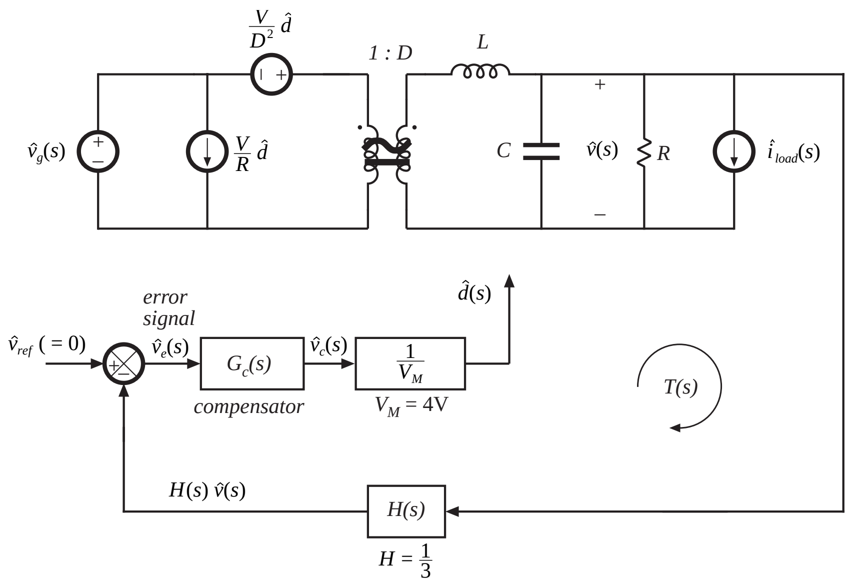

Fig. 9.23. System small-signal ac model, design example.

The open-loop converter transfer functions are discussed in the previous chapters. The open-loop control-to-output transfer function is

$$G_{vd}(s) = \frac{V}{D} \frac{1}{1 + s\frac{L}{R} + s^2 LC} \tag{9-47}$$

The open-loop control-to-output transfer function contains two poles, and can be written in the following normalized form:

$$G_{vd}(s) = G_{d0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{9-48}$$

By equating like coefficients in Eqs. (9-47) and (9-48), one finds that the dc gain, corner frequency, and Q-factor are given by

$$\begin{aligned} G_{d0} &= \frac{V}{D} = 28\text{V} \\ f_0 &= \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}} = 1\text{kHz} \\ Q_0 &= R\sqrt{\frac{C}{L}} = 9.5 \Rightarrow 19.5\text{dB} \end{aligned} \tag{9-49}$$

In practice, parasitic loss elements, such as the capacitor equivalent series resistance (esr), would cause a lower Q-factor to be observed. Figure 9.24 contains a Bode diagram of $G_{vd}(s)$.

The open-loop line-to-output transfer function is

$$G_{vg}(s) = D \frac{1}{1 + s\frac{L}{R} + s^2 LC} \tag{9-50}$$

This transfer function contains the same poles as in $G_{vd}(s)$, and can be written in the normalized form

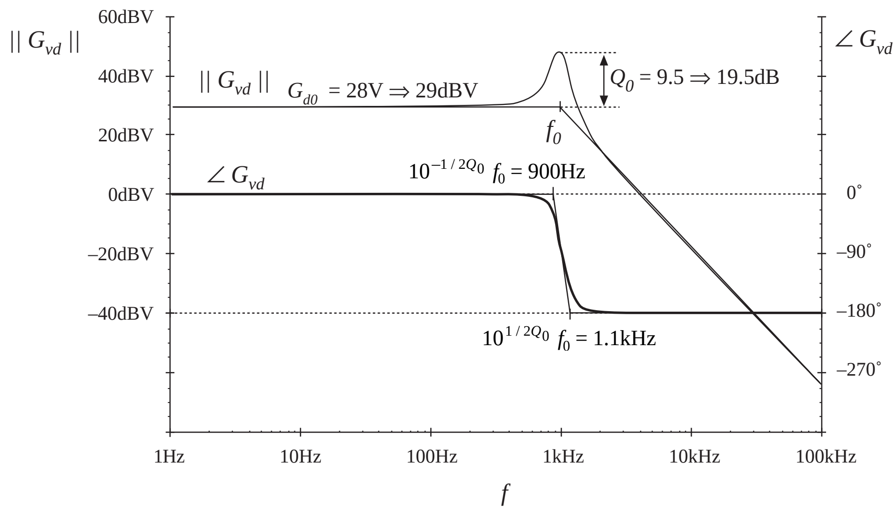

Fig. 9.24. Converter small-signal control-to-output transfer function G_{vd}, design example.

$$G_{vg}(s) = G_{g0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{9-51}$$

with $G_{g0} = D$. The open-loop output impedance of the buck converter is

$$Z_{out}(s) = R \parallel \frac{1}{sC} \parallel sL = \frac{sL}{1 + s\frac{L}{R} + s^2 LC} \tag{9-52}$$

Use of these equations to represent the converter in block-diagram form leads to the complete system block diagram of Fig. 9.25. The loop gain of the system is

$$T(s) = G_c(s) \left(\frac{1}{V_M}\right) G_{vd}(s)\, H(s) \tag{9-53}$$

Substitution of Eq. (9-48) into (9-53) leads to

$$T(s) = \frac{G_c(s)\, H(s)}{V_M} \frac{V}{D} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{9-54}$$

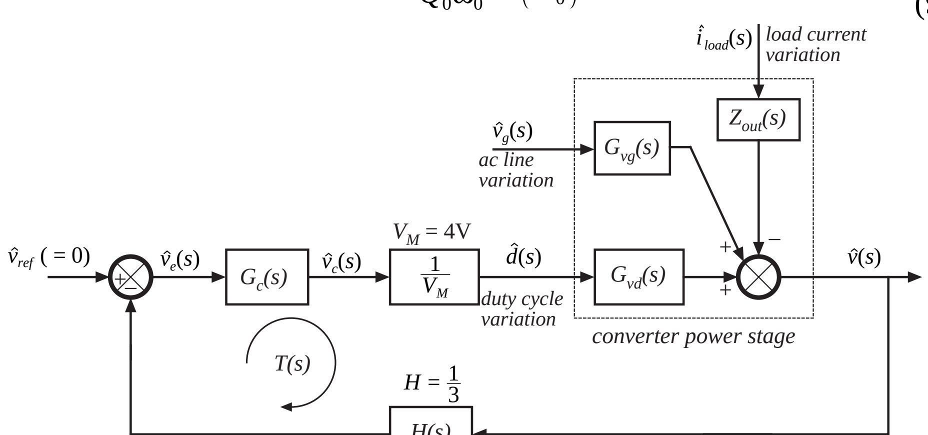

Fig. 9.25. System block diagram, design example.

The closed-loop disturbance-to-output transfer functions are given by Eqs. (9-5) and (9-6).

The uncompensated loop gain $T_u(s)$, with unity compensator gain, is sketched in Fig. 9.26. With $G_c(s) = 1$, Eq. (9-54) can be written

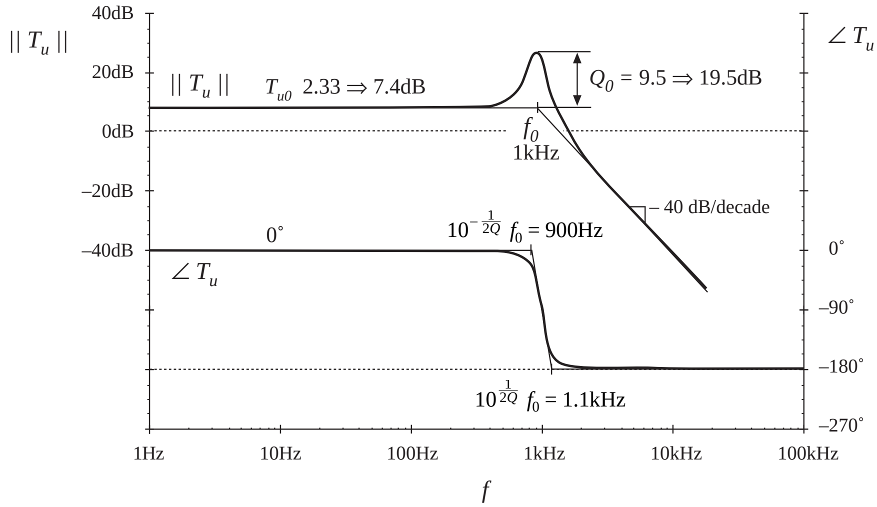

Fig. 9.26. Uncompensated loop gain T_u, design example.

$$T_u(s) = T_{u0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0} \right)^2} \tag{9-55}$$

where the dc gain is

$$T_{u0} = \frac{H\ V}{D\ V_M} = 2.33 \Rightarrow 7.4\text{dB} \tag{9-56}$$

The uncompensated loop gain has a crossover frequency of approximately 1.8kHz, with a phase margin of less than five degrees.

Let us design a compensator, to attain a crossover frequency of f_c = 5kHz, or one twentieth of the switching frequency. From Fig. 9.26, the uncompensated loop gain has a magnitude at 5kHz of approximately $T_{u0}\ (f_0\ /\ f_c)^2 = 0.093 \Rightarrow -20.6$dB. So to obtain unity loop gain at 5kHz, our compensator should have a 5kHz gain of +20.6dB. In addition, the compensator should improve the phase margin, since the phase of the uncompensated loop gain is nearly –180˚ at 5kHz. So a lead (PD) compensator is needed. Let us (somewhat arbitrarily) choose to design for a phase margin of 52˚. According to Fig. 9.13, this choice leads to closed-loop poles having a Q-factor of 1. The unit step response, Fig. 9.14, then exhibits a peak overshoot of 16%. Evaluation of Eq. (9-36), with f_c = 5kHz and θ = 52˚, leads to the following compensator pole and zero frequencies:

$$f_z = (5\text{kHz}) \sqrt{\frac{1 - \sin(52°)}{1 + \sin(52°)}} = 1.7\text{kHz}$$
$$f_p = (5\text{kHz}) \sqrt{\frac{1 + \sin(52°)}{1 - \sin(52°)}} = 14.5\text{kHz} \tag{9-57}$$

To obtain a compensator gain of 20.6dB ⇒ 10.7 at 5kHz, the low-frequency compensator gain must be

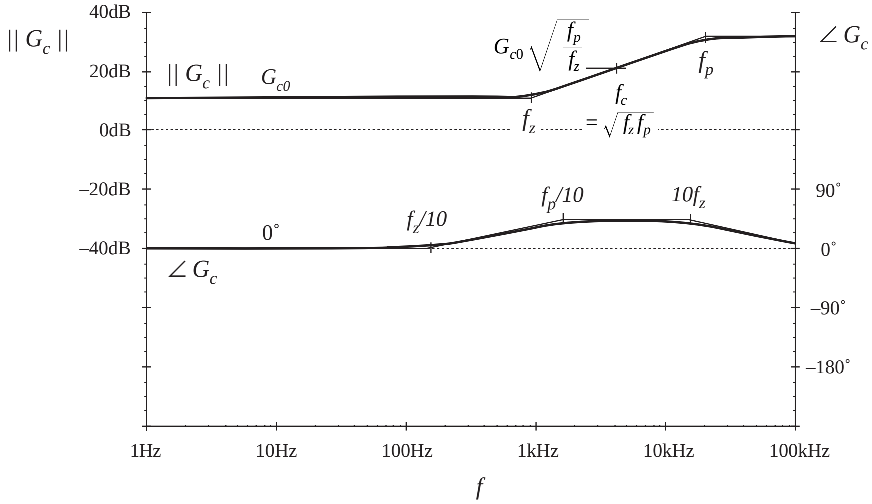

Fig. 9.27. PD compensator transfer function G_c, design example.

$$G_{c0} = \left(\frac{f_c}{f_0}\right)^2 \frac{1}{T_{u0}} \sqrt{\frac{f_z}{f_p}} = 3.7 \Rightarrow 11.3\text{dB} \tag{9-58}$$

A Bode diagram of the PD compensator magnitude and phase is sketched in Fig. 9.27.

With this PD controller, the loop gain becomes

$$T(s) = T_{u0}\, G_{c0} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)\left(1 + \frac{s}{Q_0\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \tag{9-59}$$

The compensated loop gain is sketched in Fig. 9.28. It can be seen that the phase of $T(s)$ is approximately equal to 52˚ over the frequency range of 1.4kHz to 17kHz. Hence variations in component values, which cause the crossover frequency to deviate somewhat from 5kHz, should have little impact on the phase margin. In addition, it can be seen from Fig. 9.28 that the loop gain has a dc magnitude of $T_{u0}G_{c0} \Rightarrow$ 18.7dB.

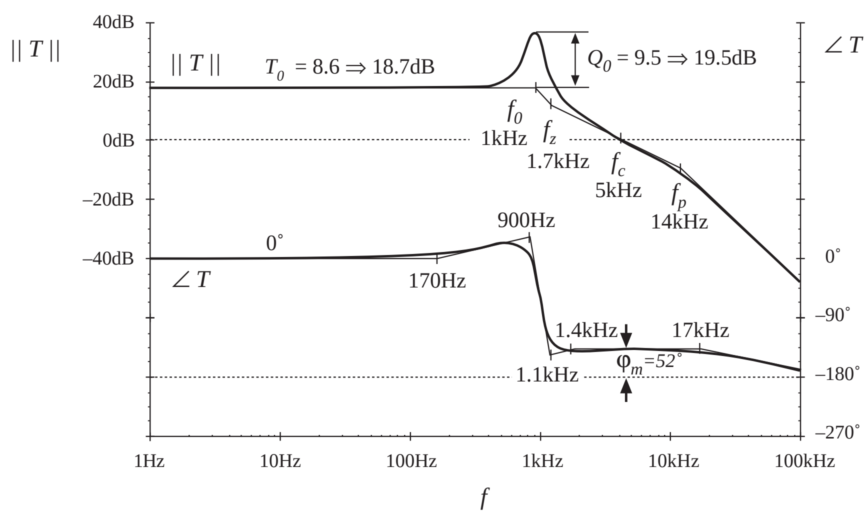

Fig. 9.28. The compensated loop gain of Eq. (9-59).

Asymptotes of the quantity 1 / (1 + T) are constructed in Fig. 9.29. This quantity has a dc asymptote of –18.7dB. Therefore, at frequencies less than 1kHz, the feedback loop attenuates output voltage disturbances by 18.7dB. For example, suppose that the input voltage $v_g(t)$ contains a 100Hz variation of amplitude 1V. With no feedback loop, this disturbance would propagate to the output according to the open-loop transfer function $G_{vg}(s)$, given in Eq. (9-51). At 100Hz, this transfer function has a gain essentially equal to the dc asymptote D = 0.536. Therefore, with no feedback loop, a 100Hz variation of amplitude 0.536V would be observed at the output. In the presence of feedback, the closed-loop line-to-output transfer function of Eq. (9-5) is obtained; for our example, this attenuates the 100Hz variation by an additional factor of 18.7dB ⇒ 8.6. The 100Hz output voltage variation now has magnitude 0.536 / 8.6 = 0.062V.

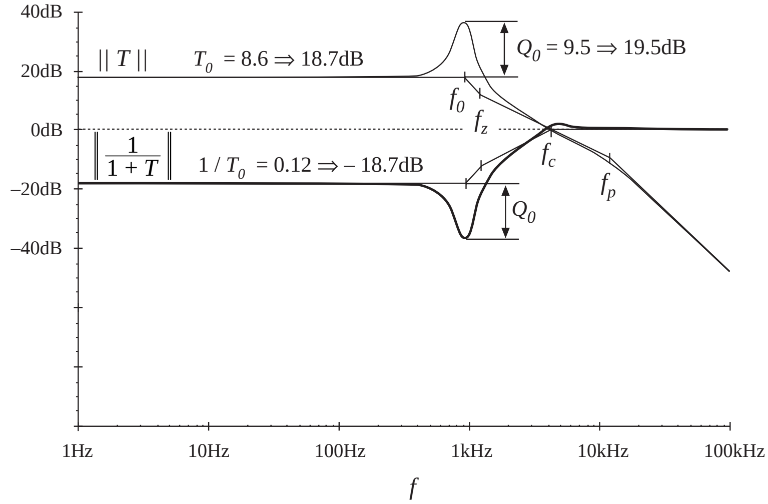

Fig. 9.29. Construction of || 1 / (1 + T) || for the PD-compensated design example of Fig. 9.28.

The low-frequency regulation can be further improved by addition of an inverted zero, as discussed in section 9.5.2. A PID controller, as in section 9.5.3, is then obtained. The compensator transfer function becomes

$$G_c(s) = G_{cm} \frac{\left(1 + \frac{s}{\omega_z}\right)\left(1 + \frac{\omega_L}{s}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \tag{9-60}$$

The pole and zero frequencies f_z and f_p are unchanged, and are given by Eq. (9-57). The midband gain G_{cm} is chosen to be the same as the previous G_{c0}, Eq. (9-58). Hence, for frequencies greater than f_L, the magnitude of the loop gain is unchanged by the inverted zero. The loop continues to exhibit a crossover frequency of 5kHz.

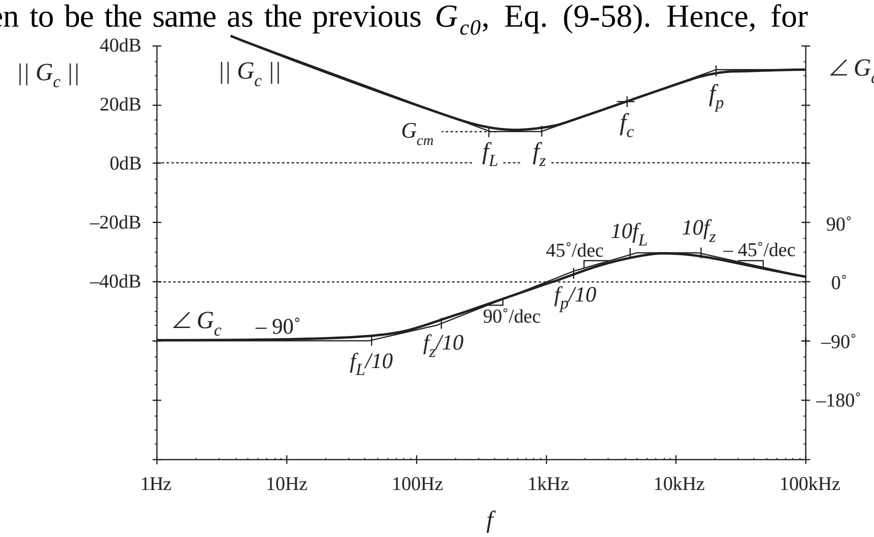

Fig. 9.30. PID compensator transfer function, Eq. (9-60).

So that the inverted zero does not significantly degrade the phase margin, let us (somewhat arbitrarily) choose f_L to be one-tenth of the crossover frequency, or 500Hz. The inverted zero will then increase the loop gain at frequencies below 500Hz, improving the low-frequency regulation of the output voltage. The loop gain of Fig. 9.31 is obtained. The magnitude of the quantity 1 / (1 + T) is also constructed. It can be seen that the inverted zero at 500Hz causes the magnitude of 1 / (1 + T) at 100Hz to be reduced by a factor of approximately (100Hz) / (500Hz) = 1/5. The total attenuation of 1 / (1 + T) at 100Hz is -32.7dB. A 1V, 100Hz variation in $v_g(t)$ would now induce a 12mV variation in $v(t)$. Further improvements could be obtained by increasing f_L; however, this would require redesign of the PD portion of the compensator to maintain an adequate phase margin.

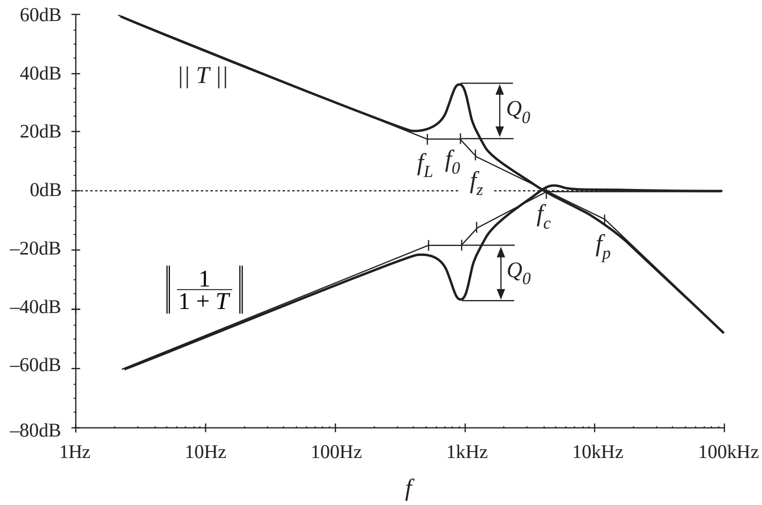

Fig. 9.31. Construction of || T || and || 1 / (1 + T) || with the PID-compensator of Fig. 9.30.

The line-to-output transfer function is constructed in Fig. 9.32. Both the open-loop transfer function $G_{vg}(s)$, Eq. (9-51), and the closed-loop transfer function $G_{vg}(s)$ / (1 + $T(s)$), are constructed using the algebra-on-the-graph method. The two transfer functions coincide at frequencies greater than the crossover frequency. At frequencies less than the crossover frequency f_c, the closed-loop transfer function is reduced by a factor of $T(s)$. It can be seen that the poles of $G_{vg}(s)$ are cancelled by zeroes of 1 / (1 + T). Hence the closed-loop line-to-output transfer function is approximately

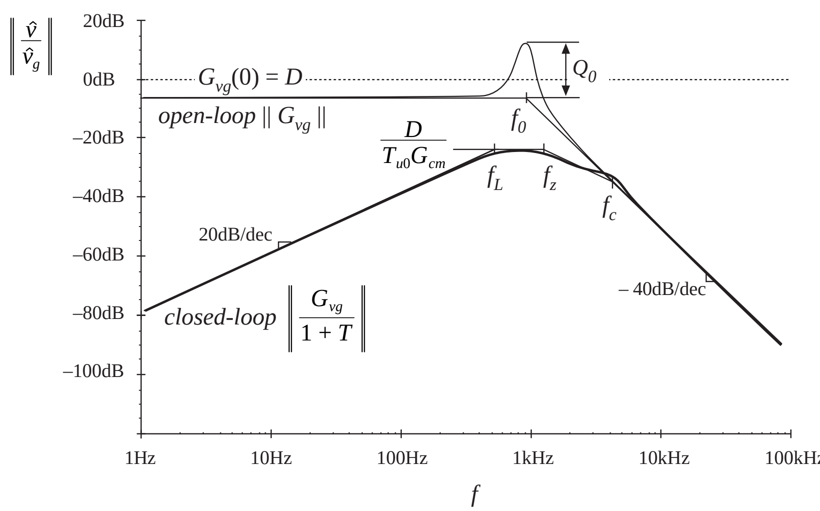

Fig. 9.32. Comparison of open-loop line-to-output transfer function G_{vg} and closed-loop line-to-output transfer function of Eq. (9-61).

$$\frac{G_{vg}(s)}{\left(1+T(s)\right)} \approx \frac{D}{T_{u0}\,G_{cm}} \frac{1}{\left(1+\frac{\omega_L}{s}\right)\left(1+\frac{s}{\omega_z}\right)\left(1+\frac{s}{\omega_c}\right)} \qquad (9\text{-}61)$$

So the algebra-on-the-graph method allows simple approximate disturbance-to-output closed-loop transfer functions to be written. Armed with such an analytical expression, the system designer can easily compute the output disturbances, and can gain the insight required to modify the element values such that system specifications are met.

9.6. Measurement of loop gains

It is good engineering practice to measure the loop gains of prototype feedback systems. The objective of such an exercise is to verify that the system has been correctly modeled. If so, then provided that a good controller design has been implemented, then the system behavior will meet expectations regarding transient overshoot (and phase margin), rejection of disturbances, dc output voltage regulation, etc. Unfortunately, there are reasons why practical system prototypes are likely to differ from theoretical models. Phenomena may occur which were not accounted for in the original model, and which significantly influence the system behavior. Noise and EMI can be present, which cause the system transfer functions to deviate in unexpected ways.

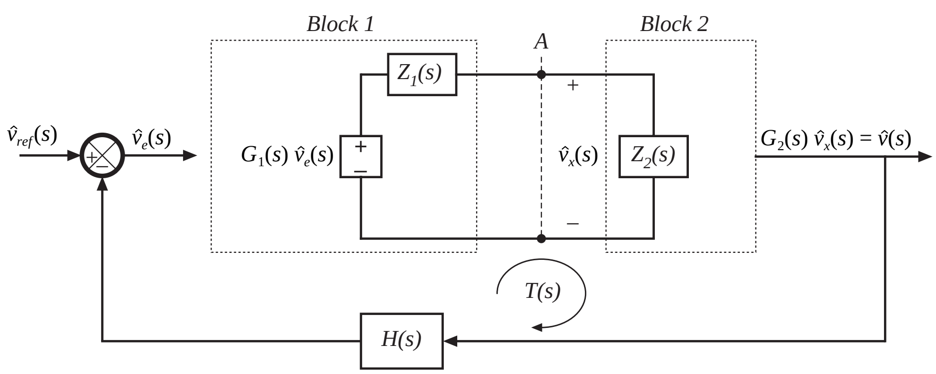

Fig. 9.33. It is desired to determine the loop gain *T(s)* experimentally, by making measurements at point *A*.

So let us consider the measurement of the loop gain *T(s)* of the feedback system of Fig. 9.33. We will make measurements at some point *A*, where two blocks of the network are connected electrically. In Fig. 9.33, the output port of block *1* is represented by a Thevenin-equivalent network, composed of the dependent voltage source $G_1 v_e$ and output impedance Z_1. Block *1* is loaded by the input impedance Z_2 of block *2*. The remainder of the feedback system is represented by a block diagram as shown. The loop gain of the system is

$$T(s) = G_1(s)\left(\frac{Z_2(s)}{Z_1(s)+Z_2(s)}\right) G_2(s)\, H(s) \tag{9-62}$$

Measurement of this loop gain presents several challenges not present in other frequency response measurements.

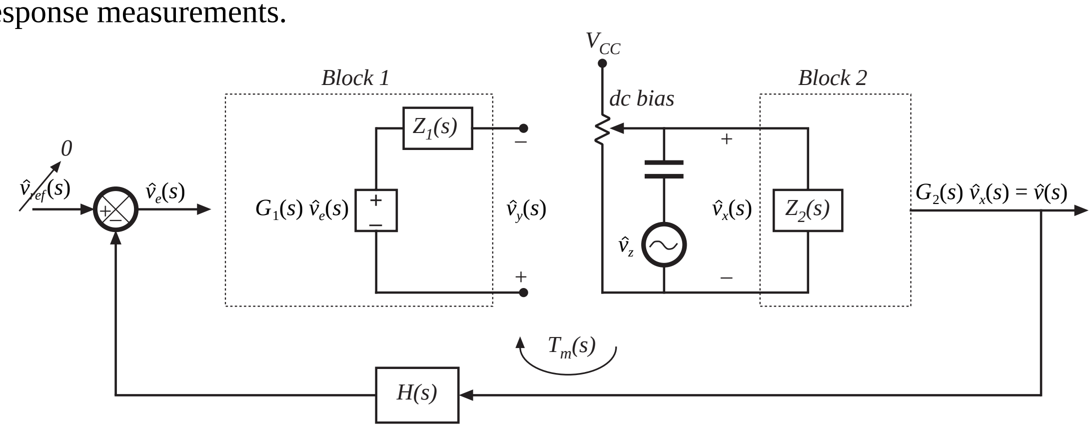

Fig. 9.34. Measurement of loop gain by breaking the loop.

In principle, one could break the loop at point *A*, and attempt to measure *T(s)* using the transfer function measurement method of the previous chapter. As illustrated in Fig. 9.34, a dc supply voltage V_{CC} and potentiometer would be used, to establish a dc bias in the voltage v_x, such that all of the elements of the network operate at the correct quiescent point. Ac voltage variations in $v_z(t)$ are coupled into the injection point via a dc blocking capacitor. Any other independent ac inputs to the system are disabled. A network analyzer is used to measure the relative magnitudes and phases of the ac components of the voltages $v_y(t)$ and $v_x(t)$:

$$T_m(s) = \left.\frac{\hat{v}_y(s)}{\hat{v}_x(s)}\right|_{\substack{\hat{v}_{ref}=0\\ \hat{v}_g=0}} \tag{9-63}$$

The measured gain $T_m(s)$ differs from the actual gain *T(s)* because, by breaking the connection between blocks *1* and *2* at the measurement point, we have removed the loading of block *2* on block *1*. Solution of Fig. 9.34 for the measured gain $T_m(s)$ leads to

$$T_m(s) = G_1(s)\, G_2(s)\, H(s) \tag{9-64}$$

Equations (9-62) and (9-64) can be combined to express $T_m(s)$ in terms of *T(s)*:

$$T_m(s) = T(s)\left(1 + \frac{Z_1(s)}{Z_2(s)}\right) \tag{9-65}$$

Hence,

$$T_m(s) \approx T(s) \quad \text{provided that} \quad \|Z_2\| >> \|Z_1\| \tag{9-66}$$

So to obtain an accurate measurement, we need to find an injection point where loading is negligible over the range of frequencies to be measured.

Other difficulties are encountered when using the method of Fig. 9.34. The most serious problem is adjustment of the dc bias using a potentiometer. The dc loop gain is typically very large, especially when a PI controller is used. A small change in the dc component of $v_x(t)$ can therefore lead to very large changes in the dc biases of some elements in the system. So it is difficult to establish the correct dc conditions in the circuit. The dc gains may drift during the experiment, making the problem even worse, and saturation of the error amplifier is a common complaint. Also, we have seen that the gains of the converter can be a function of the quiescent operating point; significant deviation from the correct operating point can cause the measured gain to differ from the loop gain of actual operating conditions.

9.6.1. Voltage injection

An approach which avoids the dc biasing problem [3] is illustrated in Fig. 9.35. The voltage source $v_z(t)$ is injected between blocks *1* and *2*, without breaking the feedback loop. Ac variations in $v_z(t)$ again excite variations in the feedback system, but dc bias conditions are determined by the circuit. Indeed, if $v_z(t)$ contains no dc component, then the biasing circuits of the system itself establish the quiescent operating point. Hence, the loop gain measurement is made at the actual system operating point.

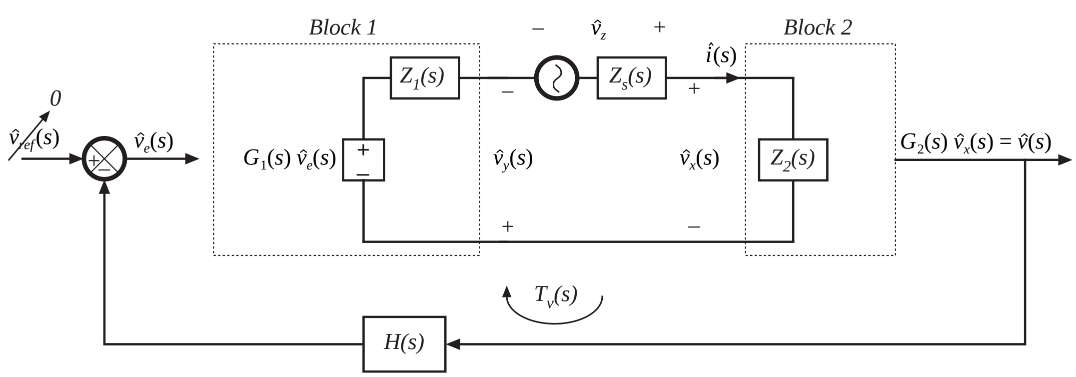

Fig. 9.35. Measurement of loop gain by voltage injection.

The injection source is modeled in Fig. 9.35 by a Thevenin equivalent network, containing an independent voltage source with source impedance $Z_s(s)$. The magnitudes of v_z and Z_s are irrelevant in the determination of the loop gain. However, the injection of v_z does disrupt the loading of block *2* on block *1*. Hence, a suitable injection point must be found, where the loading effect is negligible.

To measure the loop gain by voltage injection, we connect a network analyzer to measure the transfer function from v_x to v_y. The system independent ac inputs are set to zero, and the network analyzer sweeps the injection voltage $v_z(t)$ over the intended frequency range. The measured gain is

$$T_v(s) = \left.\frac{\hat{v}_y(s)}{\hat{v}_x(s)}\right|_{\substack{\hat{v}_{ref}=0\\ \hat{v}_g=0}} \tag{9-67}$$

Let us solve Fig. 9.35, to compare the measured gain $T_v(s)$ with the actual loop gain $T(s)$ given by Eq. (9-62). The error signal is

$$\hat{v}_e(s) = -H(s)\, G_2(s)\, \hat{v}_x(s) \tag{9-68}$$

The voltage $\hat{v}_y(s)$ can be written

$$-\hat{v}_y(s) = G_1(s)\, \hat{v}_e(s) - \hat{i}(s)\, Z_1(s) \tag{9-69}$$

where $\hat{\imath}(s)\, Z_1(s)$ is the voltage drop across the source impedance Z_1. Substitution of Eq. (9-68) into (9-69) leads to

$$-\hat{v}_y(s) = -\hat{v}_x(s)\, G_2(s)\, H(s)\, G_1(s) - \hat{i}(s)\, Z_1(s) \tag{9-70}$$

But $\hat{\imath}(s)$ is

$$\hat{i}(s) = \frac{\hat{v}_x(s)}{Z_2(s)} \tag{9-71}$$

Therefore, Eq. (9-70) becomes

$$\hat{v}_y(s) = \hat{v}_x(s)\left(G_1(s)\, G_2(s)\, H(s) + \frac{Z_1(s)}{Z_2(s)}\right) \tag{9-72}$$

Substitution of Eq. (9-72) into (9-67) leads to the following expression for the measured gain $T_v(s)$:

$$T_v(s) = G_1(s)\, G_2(s)\, H(s) + \frac{Z_1(s)}{Z_2(s)} \tag{9-73}$$

Equations (9-62) and (9-73) can be combined to determine the measured gain $T_v(s)$ in terms of the actual loop gain $T(s)$:

$$T_v(s) = T(s)\left(1 + \frac{Z_1(s)}{Z_2(s)}\right) + \frac{Z_1(s)}{Z_2(s)} \tag{9-74}$$

Thus, $T_v(s)$ can be expressed as the sum of two terms. The first term is proportional to the actual loop gain $T(s)$, and is approximately equal to $T(s)$ whenever $\| Z_1 \| << \| Z_2 \|$. The second term is not proportional to $T(s)$, and limits the minimum $T(s)$ that can be measured with the voltage injection technique. If Z_1 / Z_2 is much smaller in magnitude than $T(s)$, then the second term can be ignored, and $T_v(s) \approx T(s)$. At frequencies where $T(s)$ is smaller in magnitude than Z_1 / Z_2, the measured data must be discarded. Thus,

$$T_v(s) \approx T(s) \quad \text{provided} \quad (i) \ \left\| Z_1(s) \right\| << \left\| Z_2(s) \right\|, \ \text{and}$$
$$(ii) \ \left\| T(s) \right\| >> \left\| \frac{Z_1(s)}{Z_2(s)} \right\| \tag{9-75}$$

Again, note that the value of the injection source impedance Z_s is irrelevant.

As an example, consider voltage injection at the output of an operational amplifier, having a 50Ω output impedance, which drives a 500Ω effective load. The system in the vicinity of the injection point is illustrated in Fig. 9.36. So $Z_1(s)$ = 50Ω and $Z_2(s)$ = 500Ω. The ratio Z_1 / Z_2 is 0.1, or –20dB. Let us further suppose that the actual loop gain $T(s)$ contains poles at 10Hz and 100kHz, with a dc gain of 80dB. The actual loop gain magnitude is illustrated in Fig. 9.37.

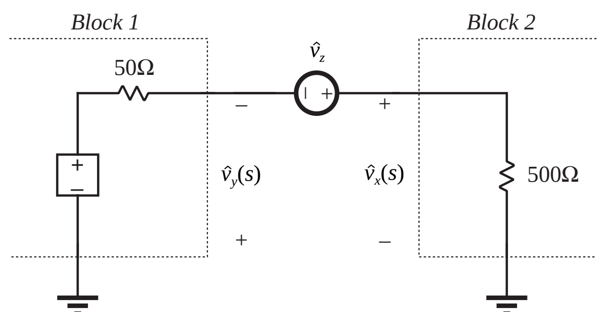

Fig. 9.36. Voltage injection example.

Voltage injection would result in measurement of $T_v(s)$ given in Eq. (9-74). Note that

$$\left(1 + \frac{Z_1(s)}{Z_2(s)}\right) = 1.1 \Rightarrow 0.83\text{dB} \tag{9-76}$$

Hence, for large $\| T \|$, the measured $\| T_v \|$ deviates from the actual loop gain by less than 1dB. However, at high frequency where $\| T \|$ is less than –20dB, the measured gain differs significantly. Apparently, $T_v(s)$ contains two high-frequency zeroes that are not present in $T(s)$. Depending on the Q-factor of these zeroes, the phase of T_v at the crossover frequency could be influenced. To ensure that the phase

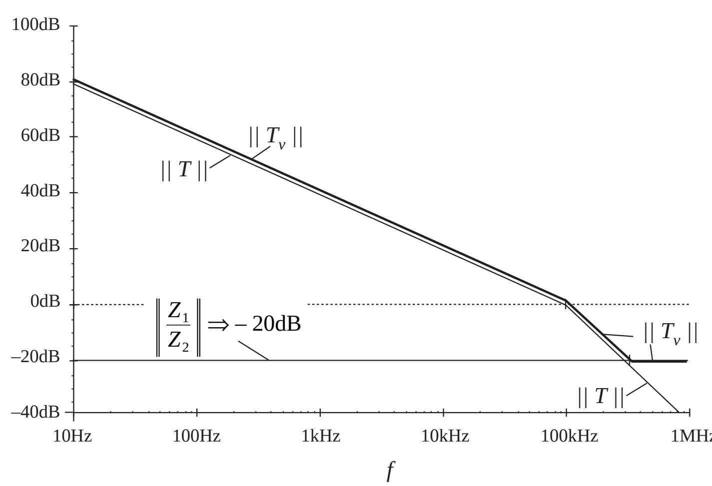

Fig. 9.37. Comparison of measured loop gain T_v and actual loop gain T, voltage injection example. The measured gain deviates at high frequency.

margin is correctly measured, it is important that Z_1 / Z_2 be sufficiently small in magnitude.

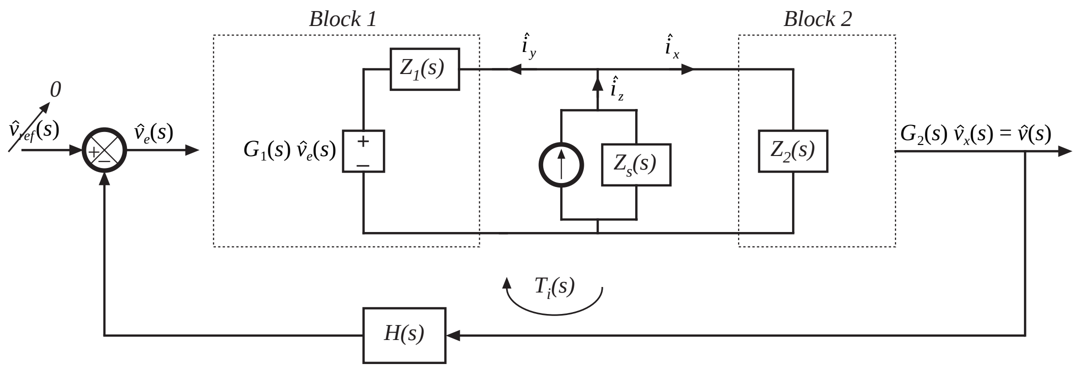

Fig. 9.38. Measurement of loop gain by current injection.

9.6.2. Current injection

The results of the preceding paragraphs can also be obtained in dual form, where the loop gain is measured by current injection [3]. As illustrated in Fig. 9.38, we can model block *1* and the analyzer injection source by their Norton equivalents, and use current probes to measure $\hat{i}_x$ and $\hat{i}_y$. The gain measured by current injection is

$$T_i(s) = \left.\frac{\hat{i}_y(s)}{\hat{i}_x(s)}\right|_{\substack{\hat{v}_{ref}=0\\ \hat{v}_g=0}} \tag{9-77}$$

It can be shown that

$$T_i(s) = T(s)\left(1 + \frac{Z_2(s)}{Z_1(s)}\right) + \frac{Z_2(s)}{Z_1(s)} \tag{9-78}$$

Hence,

$$T_i(s) \approx T(s) \text{ provided } \quad (i) \quad \left\| Z_2(s) \right\| << \left\| Z_1(s) \right\|, \quad \text{and}$$

$$(ii) \quad \left\| T(s) \right\| >> \left\| \frac{Z_2(s)}{Z_1(s)} \right\| \tag{9-79}$$

So to obtain an accurate measurement of the loop gain by current injection, we must find a point in the network where block *2* has sufficiently small input impedance. Again, note that the injection source impedance Z_s does not affect the measurement. In fact, we can realize $\hat{i}_z$ by use of a Thevenin-equivalent source, as illustrated in Fig. 9.39. The network analyzer injection source is represented

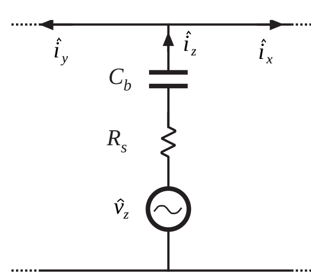

Fig. 9.39. Current injection using Thevenin-equivalent source.

by voltage source $\hat{v}_z$ and output resistance R_s. A series capacitor, C_b, is inserted to avoid disrupting the dc bias at the injection point.

9.6.3. Measurement of unstable systems

When the prototype feedback system is unstable, we are even more eager to measure the loop gain —to find out what went wrong. But measurements cannot be made while the system oscillates. We need to stabilize the system, yet measure the original unstable loop gain. It is possible to do this by recognizing that the injection source impedance Z_s does not influence the measured loop gain [3]. As illustrated in Fig. 9.40, we can even add additional resistance R_{ext}, effectively increasing the source impedance Z_s. The measured loop gain $T_v(s)$ is unaffected.

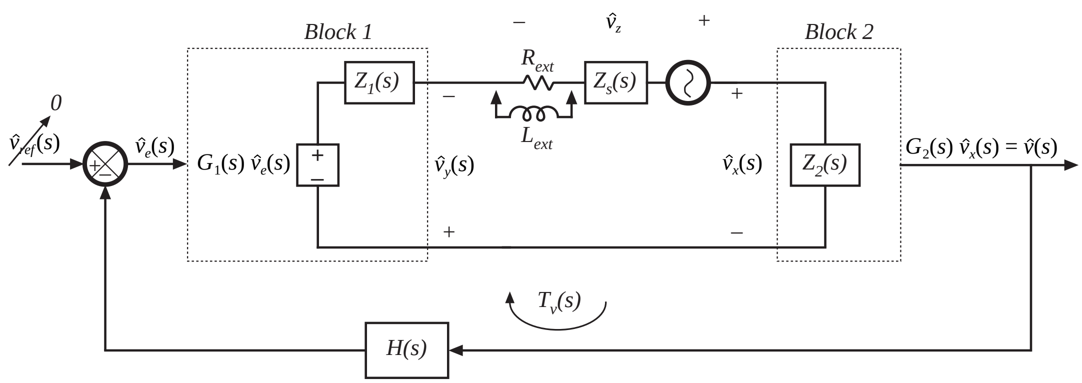

Fig. 9.40. Measurement of an unstable loop gain by voltage injection.

Adding series impedance generally lowers the loop gain of a system, leading to a lower crossover frequency and a more positive phase margin. Hence, it is usually possible to add a resistor R_{ext} that is sufficiently large to stabilize the system. The gain $T_v(s)$, Eq. (9-67), continues to be approximately equal to the original unstable loop gain, according to Eq. (9-75). To avoid disturbing the dc bias conditions, it may be necessary to bypass R_{ext} with inductor L_{ext}. If the inductance value is sufficiently large, then it will not influence the stability of the modified system.

9.7. Summary of key points

1. Negative feedback causes the system output to closely follow the reference input, according to the gain 1 / $H(s)$. The influence on the output of disturbances and variation of gains in the forward path is reduced.
2. The loop gain $T(s)$ is equal to the products of the gains in the forward and feedback paths. The loop gain is a measure of how well the feedback system works: a large loop gain leads to better regulation of the output. The crossover frequency f_c is the

frequency at which the loop gain T has unity magnitude, and is a measure of the bandwidth of the control system.

3. The introduction of feedback causes the transfer functions from disturbances to the output to be multiplied by the factor $1/(1+T(s))$. At frequencies where T is large in magnitude (i.e., below the crossover frequency), this factor is approximately equal to $1/T(s)$. Hence, the influence of low-frequency disturbances on the output is reduced by a factor of $1/T(s)$. At frequencies where T is small in magnitude (i.e., above the crossover frequency), the factor is approximately equal to 1. The feedback loop then has no effect. Closed-loop disturbance-to-output transfer functions, such as the line-to-output transfer function or the output impedance, can easily be constructed using the algebra-on-the-graph method.
4. Stability can be assessed using the phase margin test. The phase of T is evaluated at the crossover frequency, and the stability of the important closed-loop quantities $T/(1+T)$ and $1/(1+T)$ is then deduced. Inadequate phase margin leads to ringing and overshoot in the system transient response, and peaking in the closed-loop transfer functions.
5. Compensators are added in the forward paths of feedback loops to shape the loop gain, such that desired performance is obtained. Lead compensators, or PD controllers, are added to improve the phase margin and extend the control system bandwidth. PI controllers are used to increase the low-frequency loop gain, to improve the rejection of low-frequency disturbances and reduce the steady-state error.
6. Loop gains can be experimentally measured by use of voltage or current injection. This approach avoids the problem of establishing the correct quiescent operating conditions in the system, a common difficulty in systems having a large dc loop gain. An injection point must be found where interstage loading is not significant. Unstable loop gains can also be measured.

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PROBLEMS

9.1. Derive both forms of Eq. (9-25).

9.2. The flyback converter system of Fig. 9.41 contains a feedback loop for regulation of the main output voltage v_1. An auxiliary output produces voltage v_2. The dc input voltage v_g lies in the range 280V ≤ v_g ≤ 380V. The compensator network has transfer function

$$G_c(s) = G_{c\infty}\left(1 + \frac{\omega_1}{s}\right)$$

where $G_{c\infty} = 0.05$, and $f_1 = \omega_1/2\pi = 400$Hz.

(a) What is the steady-state value of the error voltage $v_e(t)$? Explain your reasoning.

(b) Determine the steady-state value of the main output voltage v_1.

(c) Estimate the steady-state value of the auxiliary output voltage v_2.

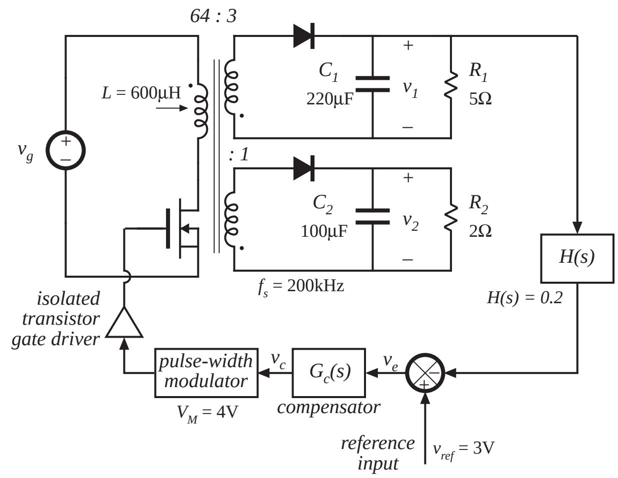

Fig. 9.41.

9.3. In the boost converter system of Fig. 9.42, all elements are ideal. The compensator has gain $G_c(s) = 1000/s$.

(a) Construct the Bode plot of the loop gain $T(s)$ magnitude and phase. Label values of all corner frequencies and Q-factors, as appropriate.

(b) Determine the crossover frequency and phase margin.

(c) Construct the Bode diagram of the magnitude of $1/(1+T)$, using the algebra-on-the-graph method. Label values of all corner frequencies and Q-factors, as appropriate.

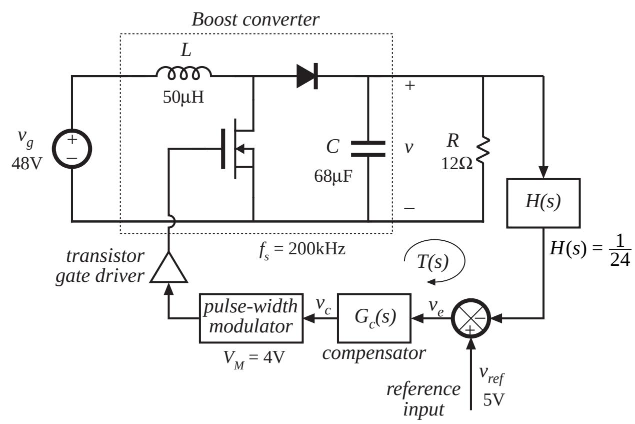

Fig. 9.42.

(d) Construct the Bode diagram of the magnitude of the closed-loop line-to-output transfer function. Label values of all corner frequencies and Q-factors, as appropriate.

9.4. A certain inverter system has the following loop gain

$$T(s) = T_0 \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)\left(1 + \frac{s}{\omega_3}\right)}$$

and the following open-loop line-to-output transfer function

$$G_{vg}(s) = G_{g0} \frac{1}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_3}\right)}$$

where

$T_0 = 100$ $\omega_1 = 500$ rad/s

$\omega_2 = 1000$ rad/s $\omega_3 = 24000$ rad/s

$\omega_z = 4000$ rad/s $G_{g0} = 0.5$

The gain of the feedback connection is $H(s) = 0.1$.

(a) Sketch the magnitude and phase asymptotes of the loop gain $T(s)$. Determine numerical values of the crossover frequency in Hz and phase margin in degrees.

(b) Construct the magnitude asymptotes of the closed-loop line-to-output transfer function. Label important features.

(c) Construct the magnitude asymptotes of the closed-loop transfer function from the reference voltage to the output voltage. Label important features.

9.5. The forward converter system of Fig. 9.43 is constructed with the element values shown. The quiescent value of the input voltage is V_g = 380V. The transformer has turns ratio $n_1 / n_3 = 4.5$. The duty cycle produced by the pulse-width modulator is restricted to the range $0 \le d(t) \le 0.5$. Within this range, $d(t)$ follows the control voltage $v_c(t)$ according to

$$d(t) = \frac{1}{2}\frac{v_c(t)}{V_M}$$

with V_M = 3 volts.

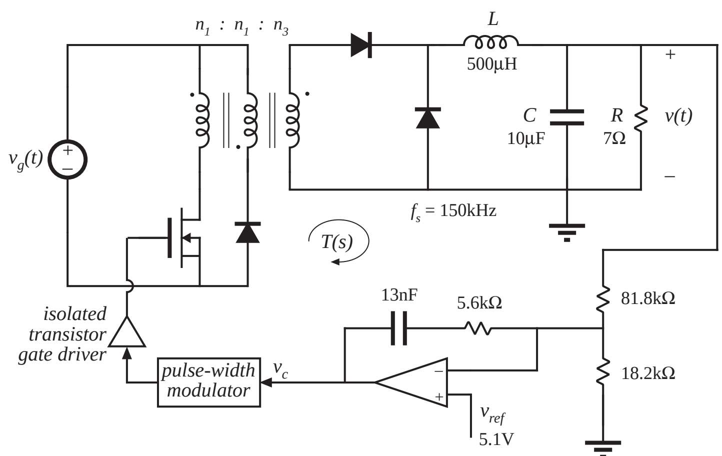

Fig. 9.43.

(a) Determine the quiescent values of: the duty cycle D, the output voltage V, and the control voltage V_c.

(b) Sketch a block diagram which models the small-signal ac variations in the system, and determine the transfer function of each block.

(c) Construct a Bode plot of the loop gain magnitude and phase. What is the crossover frequency? What is the phase margin?

(d) Construct the Bode plot of the closed-loop line-to-output transfer function magnitude

$$\left\| \frac{\hat{v}}{\hat{v}_g} \right\|$$

Label important features. What is the gain at 120Hz? At what frequency do disturbances in v_g have the greatest influence on the output voltage?

9.6. In the voltage regulator system of Fig. 9.43, described in problem 9.5, the input voltage $v_g(t)$ contains a 120Hz variation of peak amplitude 10V.

(a) What is the amplitude of the resulting 120Hz variation in $v(t)$?

(b) Modify the compensator network such that the 120Hz output voltage variation has peak amplitude less than 25mV. Your modification should leave the dc output voltage unchanged, and should result in a crossover frequency no greater than 10kHz.

9.7. Design of a boost converter with current feedback and a PI compensator. In some applications, it is desired to control the converter terminal current waveform. The boost converter system of Fig. 9.44 contains a feedback loop which causes the converter input current $i_g(t)$ to be proportional to a reference voltage $v_{ref}(t)$. The feedback connection is a current sense circuit having gain $H(s)$ = 0.2 volts per ampere. A conventional pulse width modulator circuit (Fig. 7.62) is employed, having a sawtooth waveform with peak-peak amplitude of V_M = 3 volts. The quiescent values of the inputs are: V_g = 120 volts, V_{ref} = 2 volts. All elements are ideal.

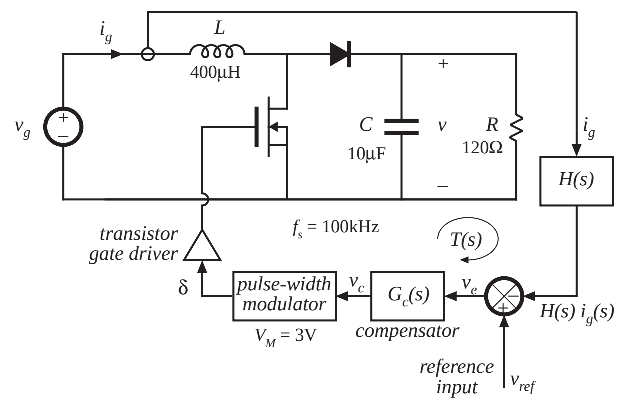

Fig. 9.44.

(a) Determine the quiescent values D, V, and I_g.

(b) Determine the small-signal transfer function

$$G_{id}(s) = \frac{\hat{i}_g(s)}{\hat{d}(s)}$$

(c) Sketch the magnitude and phase asymptotes of the uncompensated ($G_c(s)$ = 1) loop gain.

(d) It is desired to obtain a loop gain magnitude of at least 35dB at 120Hz, while maintaining a phase margin of at least 72˚. The crossover frequency should be no greater than f_s / 10 = 10kHz. Design a PI compensator which accomplishes this. Sketch the magnitude and phase asymptotes of the resulting loop gain, and label important features.

(e) For your design of part (d), sketch the magnitude of the closed-loop transfer function

$$\frac{\hat{i}_g(s)}{\hat{v}_{ref}(s)}$$

Label important features.

9.8. Design of a buck regulator to meet closed-loop output impedance specifications. The buck converter with control system illustrated in Fig. 9.45 is to be designed to meet the following specifications. The closed-loop output impedance should be less than 0.2Ω over the entire frequency range 0-20kHz. To ensure that the transient response is well-behaved, the poles of the closed-loop transfer functions, in the vicinity of the crossover frequency, should have Q-factors no greater than unity. The quiescent load current I_{LOAD} can vary from 5A to 50A, and the above specifications must be met for every value of I_{LOAD} in this range. For simplicity, you may assume that the

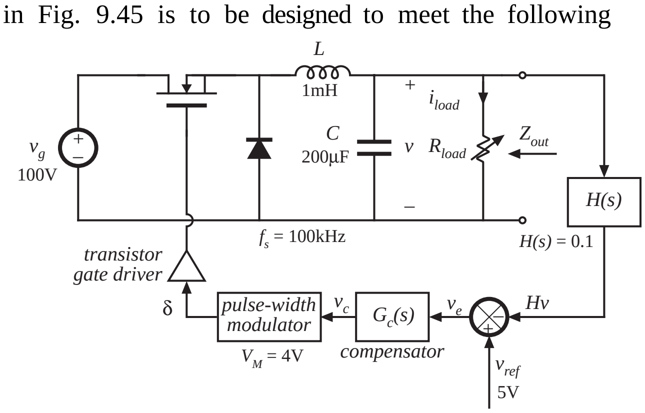

Fig. 9.45.

input voltage v_g does not vary. The loop gain crossover frequency f_c may be chosen to be no greater than f_s / 10, or 10kHz. You may also assume that all elements are ideal. The pulse-width modulator circuit obeys Eq. (7-132).

(a) What is the intended dc output voltage V? Over what range does the effective load resistance R_{LOAD} vary?

(b) Construct the magnitude asymptotes of the open-loop output impedance $Z_{out}(s)$. Over what range of frequencies is the output impedance specification not met? Hence, deduce how large the minimum loop gain $T(s)$ must be in magnitude, such that the closed-loop output impedance meets the specification. Choose a suitable crossover frequency f_c.

(c) Design a compensator network $G_c(s)$ such that all specifications are met. Additionally, the dc loop gain $T(s)$ should be at least 20dB. Specify the following:

(i) Your choice for the transfer function $G_c(s)$

(ii) The worst-case closed-loop Q

(iii) Bode plots of the loop gain $T(s)$ and the closed-loop output impedance, for load currents of 5A and 50A. What effect does variation of R_{LOAD} have on the closed-loop behavior of your design?

(d) Design a circuit using resistors, capacitors, and an op amp, to realize your compensator transfer function $G_c(s)$.

9.9 Design of a buck-boost voltage regulator. The buck-boost converter of Fig. 9.46 operates in the continuous conduction mode, with the element values shown. The nominal input voltage is V_g = 48V, and it is desired to regulate the output voltage at –15V. Design the best compensator that you can, which has high crossover frequency (but no greater than 10% of the switching frequency), large loop gain over the bandwidth of the feedback loop, and phase margin of at least 52˚.

(a) Specify the required value of H. Sketch Bode plots of the uncompensated loop gain magnitude and phase, as well as the magnitude and phase of your proposed compensator transfer function $G_c(s)$. Label the important features of your plots.

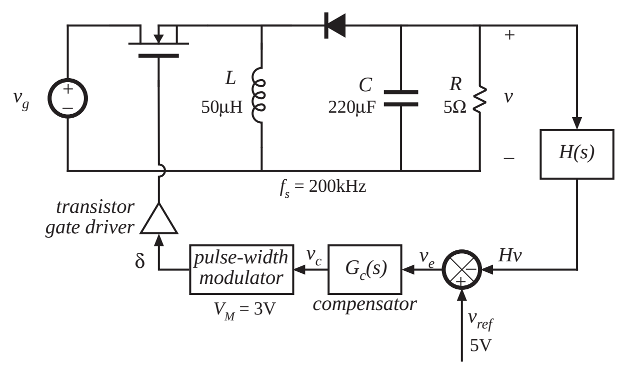

Fig. 9.46.

(b) Construct Bode diagrams of the magnitude and phase of your compensated loop gain $T(s)$, and also of the magnitude of the quantities T / (1 + T) and 1 / (1 + T).

(c) Discuss your design. What prevents you from further increasing the crossover frequency? How large is the loop gain at 120Hz? Can you obtain more loop gain at 120Hz?

9.10 The loop gain of a certain feedback system is measured, using voltage injection at a point in the forward path of the loop as illustrated in Fig. 9.47(a). The data in Fig. 9.47(b) is obtained. What is *T(s)*? Specify *T(s)* in factored pole-zero form, and give numerical values for all important features. Over what range of frequencies does the measurement give valid results?

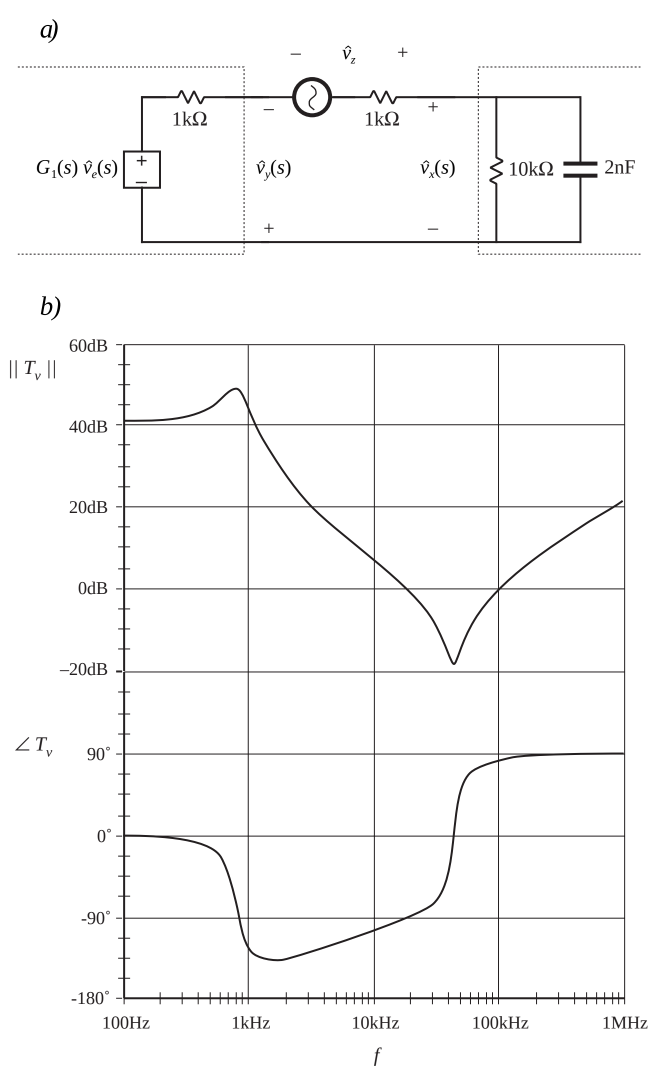

Fig. 9.47.