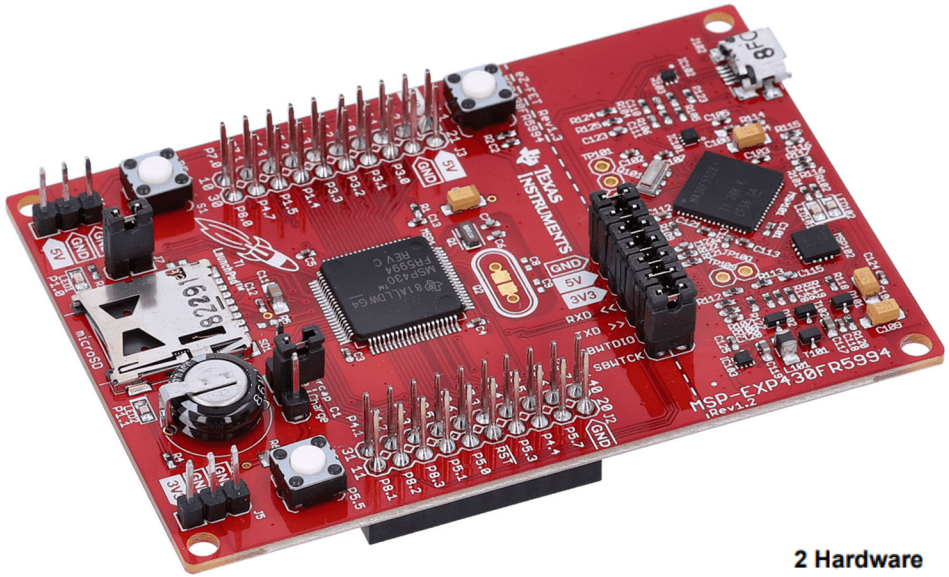
ECE 482: Experiment 2

THE UNIVERSITY OF
TENNESSEE
KNOXVILLE



2 Hardware

Figure 2-1 shows an overview of the MSP-EXP430FR5994 hardware.

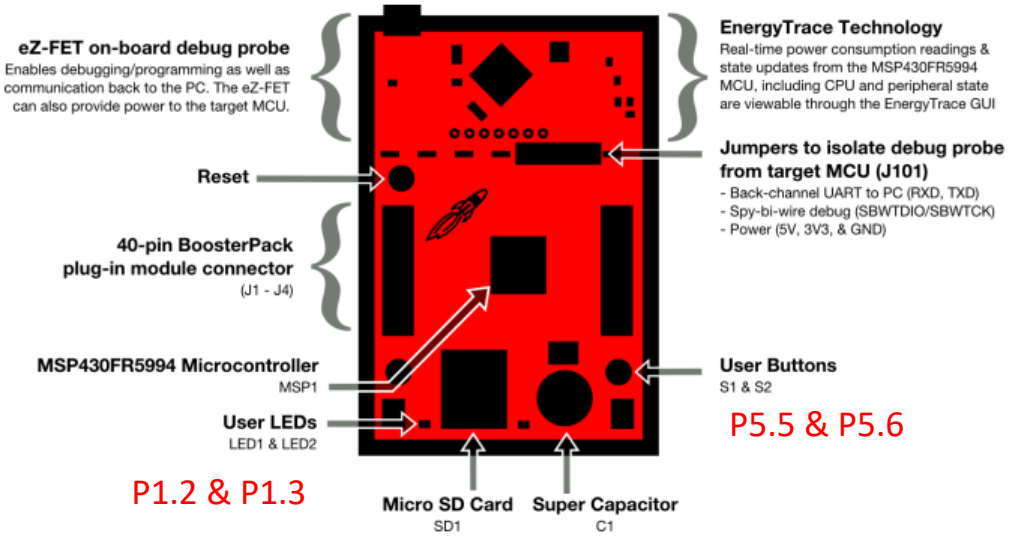


Figure 2-1. MSP-EXP430FR5994 Overview

Important Documents

- EXP430FR5994 (Launchpad Development Kit)
  - User Guide
  - Software Examples
  - https://www.ti.com/tool/MSP-EXP430FR5994

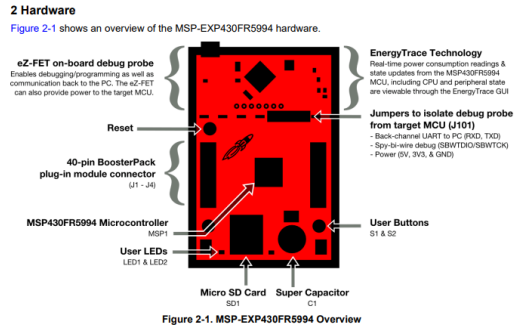
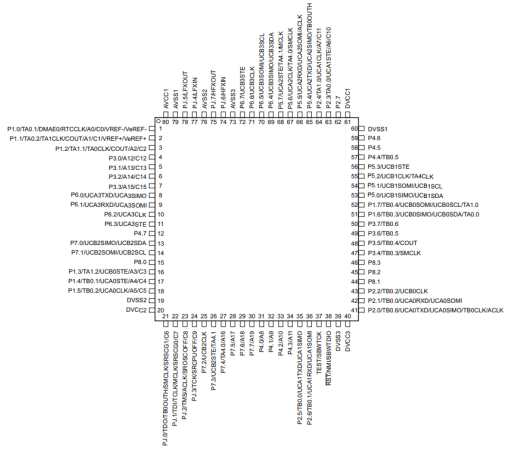


Figure 2-1. MSP-EXP430FR5994 Overview

- MSP430FR5994 (Microcontroller)
  - User Guide
  - Datasheet
  - Example Codes
  - https://www.ti.com/product/MSP430FR5994



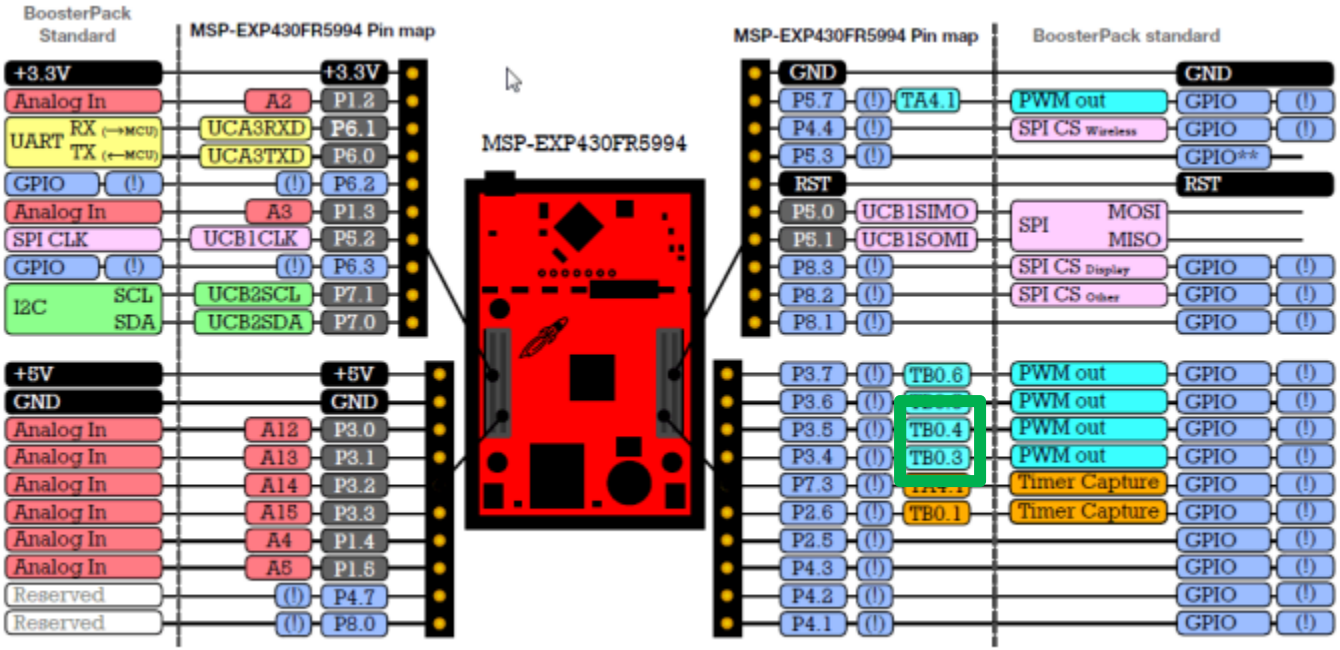
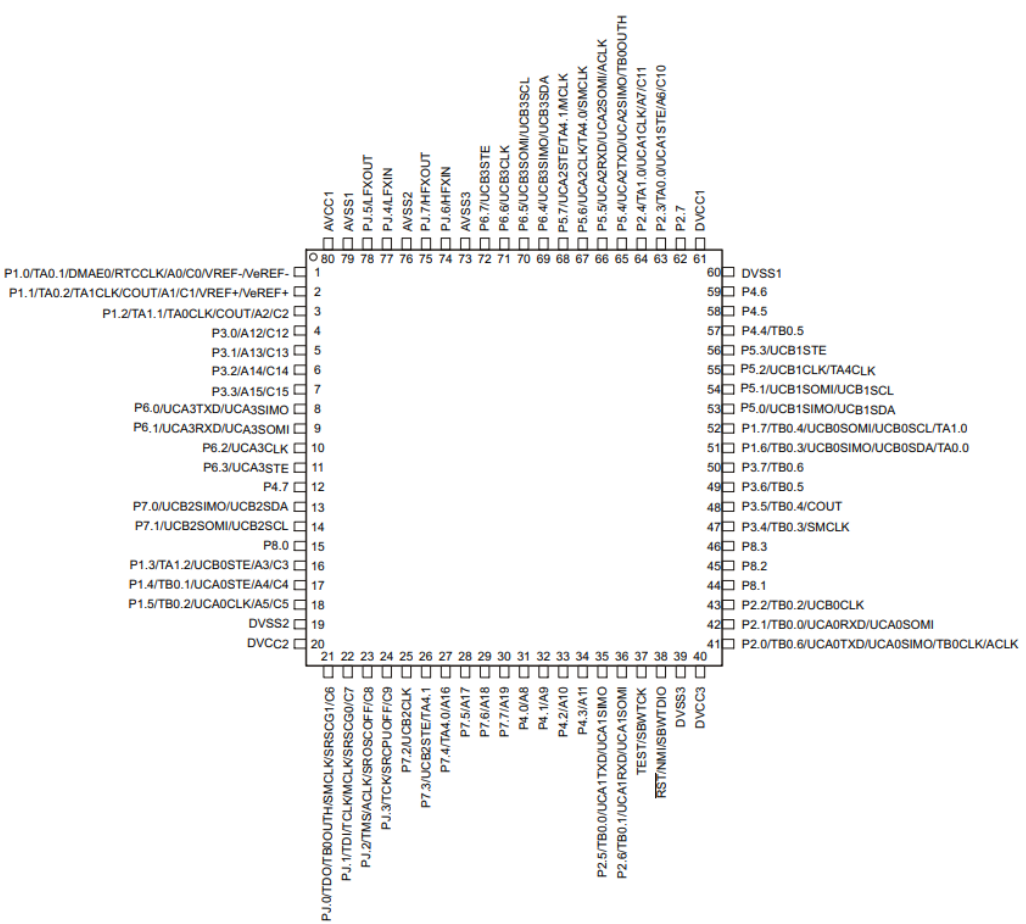


Figure 2-10. LaunchPad Development Kit to BoosterPack Plug-in Module Connector Pinout



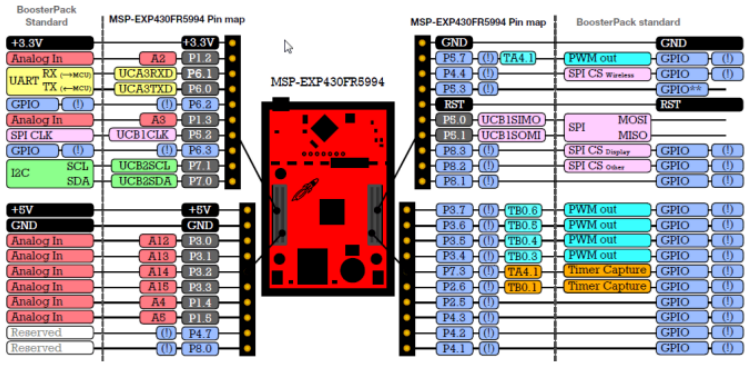
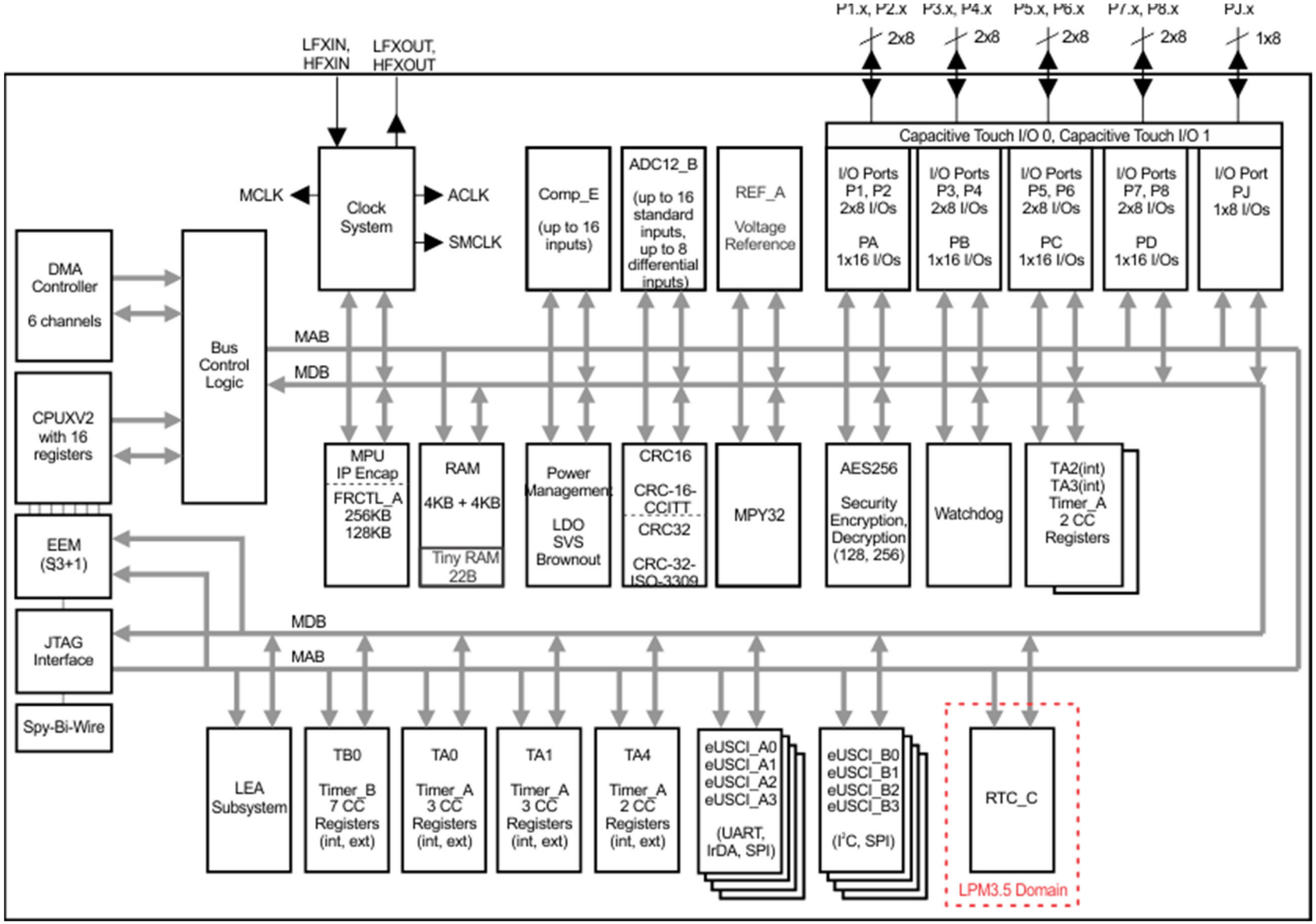


Figure 2-10. LaunchPad Development Kit to BoosterPack Plug-in Module Connector Pinout


P1.x, P2.x
P3.x, P4.x
P5.x, P6.x
P7.x, P8.x
PJ.x
2x8
2x8
2x8
2x8
1x8
LFXIN, HFXIN
LFXOUT, HFXOUT
Capacitive Touch I/O 0, Capacitive Touch I/O 1
MCLK
Clock System
ACLK
SMCLK
Comp_E (up to 16 inputs)
ADC12_B (up to 16 standard inputs, up to 8 differential inputs)
REF_A Voltage Reference
I/O Ports P1, P2 2x8 I/Os PA 1x16 I/Os
I/O Ports P3, P4 2x8 I/Os PB 1x16 I/Os
I/O Ports P5, P6 2x8 I/Os PC 1x16 I/Os
I/O Ports P7, P8 2x8 I/Os PD 1x16 I/Os
I/O Port PJ 1x8 I/Os
DMA Controller 6 channels
Bus Control Logic
MAB
MDB
CPUXV2 with 16 registers
MPU IP Encap FRCTL_A 256KB 128KB
RAM 4KB + 4KB
Tiny RAM 22B
Power Management LDO SVS Brownout
CRC16 CRC-16-CCITT CRC32 CRC-32-ISO-3309
MPY32
AES256 Security Encryption, Decryption (128, 256)
Watchdog
TA2(int) TA3(int) Timer_A 2 CC Registers
EEM (S3+1)
JTAG Interface
Spy-Bi-Wire
MDB
MAB
LEA Subsystem
TB0 Timer_B 7 CC Registers (int, ext)
TA0 Timer_A 3 CC Registers (int, ext)
TA1 Timer_A 3 CC Registers (int, ext)
TA4 Timer_A 2 CC Registers (int, ext)
eUSCI_A0 eUSCI_A1 eUSCI_A2 eUSCI_A3 (UART, IrDA, SPI)
eUSCI_B0 eUSCI_B1 eUSCI_B2 eUSCI_B3 (I²C, SPI)
RTC_C
LPM3.5 Domain

MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family

User's Guide

Literature Number: SLAU367P
October 2012–Revised April 2020

12.2 Digital I/O Operation

The digital I/O are configured with user software. The setup and operation of the digital I/O are discussed in the following sections.

12.2.1 Input Registers (PxIN)

Each bit in each PxIN register reflects the value of the input signal at the corresponding I/O pin when the pin is configured as I/O function. These registers are read only.

- Bit = 0: Input is low
- Bit = 1: Input is high

NOTE: Writing to read-only registers PxIN

Writing to these read-only registers results in increased current consumption while the write attempt is active.

12.2.2 Output Registers (PxOUT)

Each bit in each PxOUT register is the value to be output on the corresponding I/O pin when the pin is configured as I/O function, output direction.

- Bit = 0: Output is low
- Bit = 1: Output is high

If the pin is configured as I/O function, input direction and the pullup or pulldown resistor are enabled; the corresponding bit in the PxOUT register selects pullup or pulldown.

- Bit = 0: Pin is pulled down
- Bit = 1: Pin is pulled up

12.2.3 Direction Registers (PxDIR)

Each bit in each PxDIR register selects the direction of the corresponding I/O pin, regardless of the selected function for the pin. PxDIR bits for I/O pins that are selected for other functions must be set as required by the other function.

- Bit = 0: Port pin is switched to input direction
- Bit = 1: Port pin is switched to output direction

12.2.4 Pullup or Pulldown Resistor Enable Registers (PxREN)

Each bit in each PxREN register enables or disables the pullup or pulldown resistor of the corresponding I/O pin. The corresponding bit in the PxOUT register selects if the pin contains a pullup or pulldown.

- Bit = 0: Pullup or pulldown resistor disabled
- Bit = 1: Pullup or pulldown resistor enabled

Table 12-1 summarizes the use of PxDIR, PxREN, and PxOUT for proper I/O configuration.

Table 12-1. I/O Configuration

PxDIR	PxREN	PxOUT	I/O Configuration
0	0	x	Input
0	1	0	Input with pulldown resistor
0	1	1	Input with pullup resistor
1	x	x	Output

12.4.3 PxOUT Register

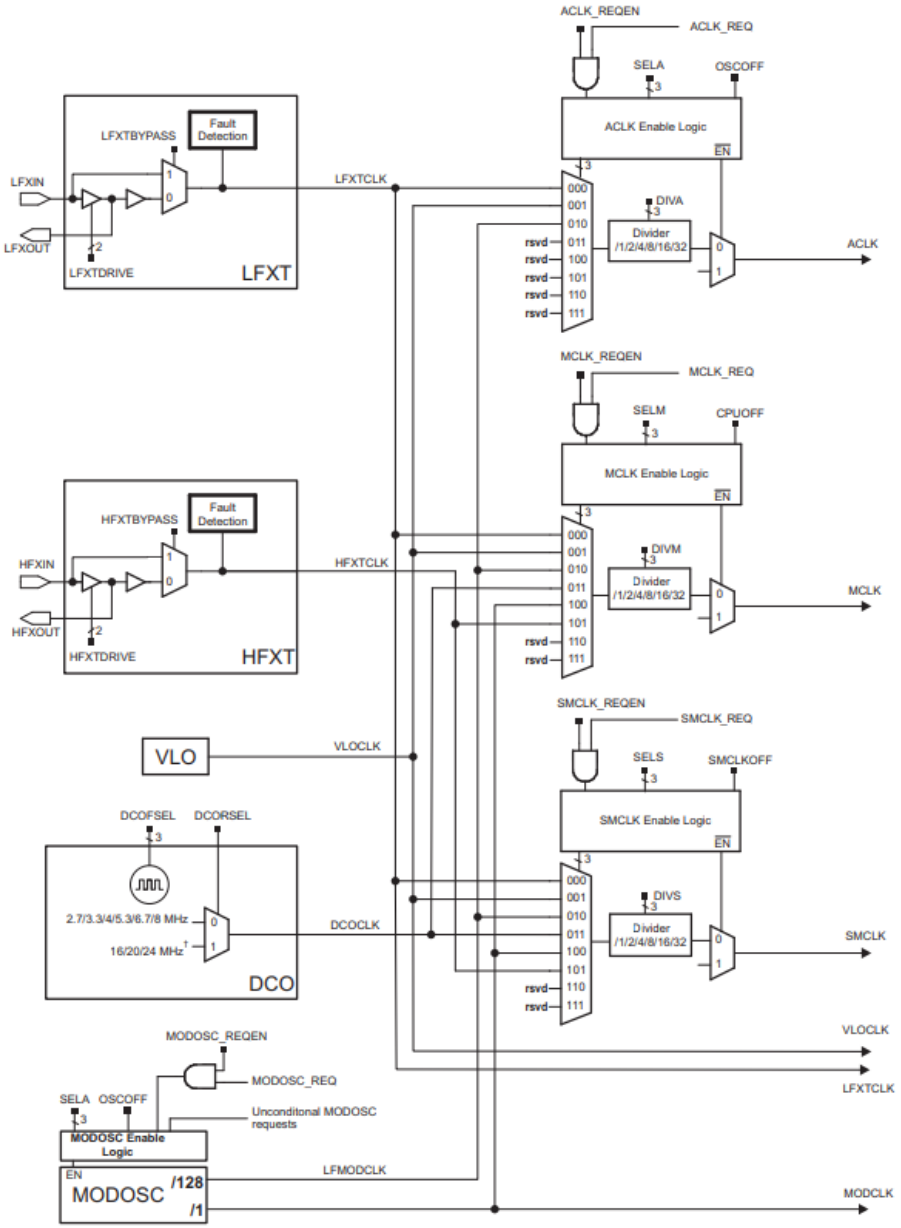
Port x Output Register

Figure 12-3. PxOUT Register

7	6	5	4	3	2	1	0
PxOUT							
rw	rw	rw	rw	rw	rw	rw	rw

Table 12-6. PxOUT Register Description

Bit	Field	Type	Reset	Description
7-0	PxOUT	RW	Undefined	Port x output When I/O configured to output mode: 0b = Output is low. 1b = Output is high. When I/O configured to input mode and pullups/pulldowns enabled: 0b = Pulldown selected 1b = Pullup selected



† Not available on all devices

Figure 3-1. Clock System Block Diagram

3.3 MemoryMap Registers

Table 3-3 lists the MemoryMap registers. All register offset addresses not listed in Table 3-3 should be considered as reserved locations and the register contents should not be modified.

Table 3-3. MEMORYMAP Registers

Offset	Acronym	Register Name	Section
0h	CTL0	Clock System Control 0	Section 3.3.1
2h	CTL1	Clock System Control 1	Section 3.3.2
4h	CTL2	Clock System Control 2	Section 3.3.3
6h	CTL3	Clock System Control 3	Section 3.3.4
8h	CTL4	Clock System Control 4	Section 3.3.5
Ah	CTL5	Clock System Control 5	Section 3.3.6
Ch	CTL6	Clock System Control 6	Section 3.3.7

3.3.1 CTL0 Register (Offset = 0h) [reset = 9600h]

CTL0 is shown in Figure 3-5 and described in Table 3-4.

Return to the Summary Table.

Clock System Control 0 Register

Figure 3-5. CTL0 Register

15	14	13	12	11	10	9	8
KEY							
R/W-96h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 3-4. CTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	KEY	R/W	96h	CSKEY password. Must always be written with A5h; a PUC is generated if any other value is written. Always reads as 96h. After the correct password is written, all CS registers are available for writing. A5h (W) = 0xA5
7-0	RESERVED	R	0h	Reserved. Always reads as 0.

3.3.2 CTL1 Register (Offset = 2h) [reset = Ch]

CTL1 is shown in Figure 3-6 and described in Table 3-5.

Return to the Summary Table.

Clock System Control 1 Register

Figure 3-6. CTL1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	DCORSEL	RESERVED		DCOFSEL			RESERVED
R-0h	R/W-0h	R-0h		R/W-6h			R-0h

Table 3-5. CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved. Always reads as 0.
6	DCORSEL	R/W	0h	DCO range select. For high speed devices, this bit can be written by the user. For low speed devices, it is always reset. See description of DCOFSEL bit for details.
5-4	RESERVED	R	0h	Reserved. Always reads as 0.
3-1	DCOFSEL	R/W	6h	DCO frequency select. Selects frequency settings for the DCO. Values shown below are approximate. Please refer to the device specific datasheet. 0h (R/W) = If DCORSEL = 0: 1 MHz; If DCORSEL = 1: 1 MHz 1h (R/W) = If DCORSEL = 0: 2.67 MHz; If DCORSEL = 1: 5.33 MHz 2h (R/W) = If DCORSEL = 0: 3.5 MHz; If DCORSEL = 1: 7 MHz 3h (R/W) = If DCORSEL = 0: 4 MHz; If DCORSEL = 1: 8 MHz 4h (R/W) = If DCORSEL = 0: 5.33 MHz; If DCORSEL = 1: 16 MHz 5h (R/W) = If DCORSEL = 0: 7 MHz; If DCORSEL = 1: 21 MHz 6h (R/W) = If DCORSEL = 0: 8 MHz; If DCORSEL = 1: 24 MHz 7h (R/W) = If DCORSEL = 0: Reserved. Defaults to 8. It is not recommended to use this setting; If DCORSEL = 1: Reserved. Defaults to 24. It is not recommended to use this setting
0	RESERVED	R	0h	Reserved. Always reads as 0.

3.3.3 CTL2 Register (Offset = 4h) [reset = 33h]

CTL2 is shown in Figure 3-7 and described in Table 3-6.

Return to the Summary Table.

Clock System Control 2 Register

Figure 3-7. CTL2 Register

15	14	13	12	11	10	9	8
RESERVED						SELA	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	SELS			RESERVED	SELM		
R-0h	R/W-3h			R-0h	R/W-3h		

Table 3-6. CTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved. Always reads as 0.
10-8	SELA	R/W	0h	Selects the ACLK source 0h (R/W) = LFXTCLK : LFXTCLK when LFXT available, otherwise VLOCLK 1h (R/W) = VLOCLK : VLOCLK 2h (R/W) = LFMODCLK : LFMODCLK
7	RESERVED	R	0h	Reserved. Always reads as 0.
6-4	SELS	R/W	3h	Selects the SMCLK source 0h (R/W) = LFXTCLK : LFXTCLK when LFXT available, otherwise VLOCLK. 1h (R/W) = VLOCLK : VLOCLK 2h (R/W) = LFMODCLK : LFMODCLK 3h (R/W) = DCOCLK : DCOCLK 4h (R/W) = MODCLK : MODCLK 5h (R/W) = HFXTCLK : HFXTCLK when HFXT available, otherwise DCOCLK.
3	RESERVED	R	0h	Reserved. Always reads as 0.
2-0	SELM	R/W	3h	Selects the MCLK source 0h (R/W) = LFXTCLK : LFXTCLK when LFXT available, otherwise VLOCLK 1h (R/W) = VLOCLK : VLOCLK 2h (R/W) = LFMODCLK : LFMODCLK 3h (R/W) = DCOCLK : DCOCLK 4h (R/W) = MODCLK : MODCLK 5h (R/W) = HFXTCLK : HFXTCLK when HFXT available, otherwise DCOCLK

3.3.4 CTL3 Register (Offset = 6h) [reset = 33h]

CTL3 is shown in Figure 3-8 and described in Table 3-7.

Return to the Summary Table.

Clock System Control 3 Register

Figure 3-8. CTL3 Register

15	14	13	12	11	10	9	8
RESERVED						DIVA	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	DIVS			RESERVED	DIVM		
R-0h	R/W-3h			R-0h	R/W-3h		

Table 3-7. CTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved. Always reads as 0.
10-8	DIVA	R/W	0h	ACLK source divider. Divides the frequency of the ACLK clock source 0h (R/W) = 1 : /1 1h (R/W) = 2 : /2 2h (R/W) = 4 : /4 3h (R/W) = 8 : /8 4h (R/W) = 16 : /16 5h (R/W) = 32 : /32
7	RESERVED	R	0h	Reserved. Always reads as 0.
6-4	DIVS	R/W	3h	SMCLK source divider. Divides the frequency of the SMCLK clock source 0h (R/W) = 1 : /1 1h (R/W) = 2 : /2 2h (R/W) = 4 : /4 3h (R/W) = 8 : /8 4h (R/W) = 16 : /16 5h (R/W) = 32 : /32
3	RESERVED	R	0h	Reserved. Always reads as 0.
2-0	DIVM	R/W	3h	MCLK source divider. Divides the frequency of the MCLK clock source 0h (R/W) = 1 : /1 1h (R/W) = 2 : /2 2h (R/W) = 4 : /4 3h (R/W) = 8 : /8 4h (R/W) = 16 : /16 5h (R/W) = 32 : /32

3.3.1 CTL0 Register (Offset = 0h) [reset = 9600h]

CTL0 is shown in Figure 3-5 and described in Table 3-4.

Return to the Summary Table.

Clock System Control 0 Register

Figure 3-5. CTL0 Register

15	14	13	12	11	10	9	8
KEY							
R/W-96h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 3-4. CTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	KEY	R/W	96h	CSKEY password. Must always be written with A5h; a PUC is generated if any other value is written. Always reads as 96h. After the correct password is written, all CS registers are available for writing. A5h (W) = 0xA5
7-0	RESERVED	R	0h	Reserved. Always reads as 0.

3.3.2 CTL1 Register (Offset = 2h) [reset = Ch]

CTL1 is shown in Figure 3-6 and described in Table 3-5.

Return to the Summary Table.

Clock System Control 1 Register

Figure 3-6. CTL1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	DCORSEL	RESERVED		DCOFSEL			RESERVED
R-0h	R/W-0h	R-0h		R/W-6h			R-0h

Table 3-5. CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved. Always reads as 0.
6	DCORSEL	R/W	0h	DCO range select. For high speed devices, this bit can be written by the user. For low speed devices, it is always reset. See description of DCOFSEL bit for details.
5-4	RESERVED	R	0h	Reserved. Always reads as 0.
3-1	DCOFSEL	R/W	6h	DCO frequency select. Selects frequency settings for the DCO. Values shown below are approximate. Please refer to the device specific datasheet. 0h (R/W) = If DCORSEL = 0: 1 MHz; If DCORSEL = 1: 1 MHz 1h (R/W) = If DCORSEL = 0: 2.67 MHz; If DCORSEL = 1: 5.33 MHz 2h (R/W) = If DCORSEL = 0: 3.5 MHz; If DCORSEL = 1: 7 MHz 3h (R/W) = If DCORSEL = 0: 4 MHz; If DCORSEL = 1: 8 MHz 4h (R/W) = If DCORSEL = 0: 5.33 MHz; If DCORSEL = 1: 16 MHz 5h (R/W) = If DCORSEL = 0: 7 MHz; If DCORSEL = 1: 21 MHz 6h (R/W) = If DCORSEL = 0: 8 MHz; If DCORSEL = 1: 24 MHz 7h (R/W) = If DCORSEL = 0: Reserved. Defaults to 8. It is not recommended to use this setting; If DCORSEL = 1: Reserved. Defaults to 24. It is not recommended to use this setting
0	RESERVED	R	0h	Reserved. Always reads as 0.

3.3.3 CTL2 Register (Offset = 4h) [reset = 33h]

CTL2 is shown in Figure 3-7 and described in Table 3-6.

Return to the Summary Table.

Clock System Control 2 Register

Figure 3-7. CTL2 Register

15	14	13	12	11	10	9	8
RESERVED						SELA	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	SELS			RESERVED	SELM		
R-0h	R/W-3h			R-0h	R/W-3h		

Table 3-6. CTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved. Always reads as 0.
10-8	SELA	R/W	0h	Selects the ACLK source 0h (R/W) = LFXTCLK : LFXTCLK when LFXT available, otherwise VLOCLK 1h (R/W) = VLOCLK : VLOCLK 2h (R/W) = LFMODCLK : LFMODCLK
7	RESERVED	R	0h	Reserved. Always reads as 0.
6-4	SELS	R/W	3h	Selects the SMCLK source 0h (R/W) = LFXTCLK : LFXTCLK when LFXT available, otherwise VLOCLK. 1h (R/W) = VLOCLK : VLOCLK 2h (R/W) = LFMODCLK : LFMODCLK 3h (R/W) = DCOCLK : DCOCLK 4h (R/W) = MODCLK : MODCLK 5h (R/W) = HFXTCLK : HFXTCLK when HFXT available, otherwise DCOCLK.
3	RESERVED	R	0h	Reserved. Always reads as 0.
2-0	SELM	R/W	3h	Selects the MCLK source 0h (R/W) = LFXTCLK : LFXTCLK when LFXT available, otherwise VLOCLK 1h (R/W) = VLOCLK : VLOCLK 2h (R/W) = LFMODCLK : LFMODCLK 3h (R/W) = DCOCLK : DCOCLK 4h (R/W) = MODCLK : MODCLK 5h (R/W) = HFXTCLK : HFXTCLK when HFXT available, otherwise DCOCLK

3.3.4 CTL3 Register (Offset = 6h) [reset = 33h]

CTL3 is shown in Figure 3-8 and described in Table 3-7.

Return to the Summary Table.

Clock System Control 3 Register

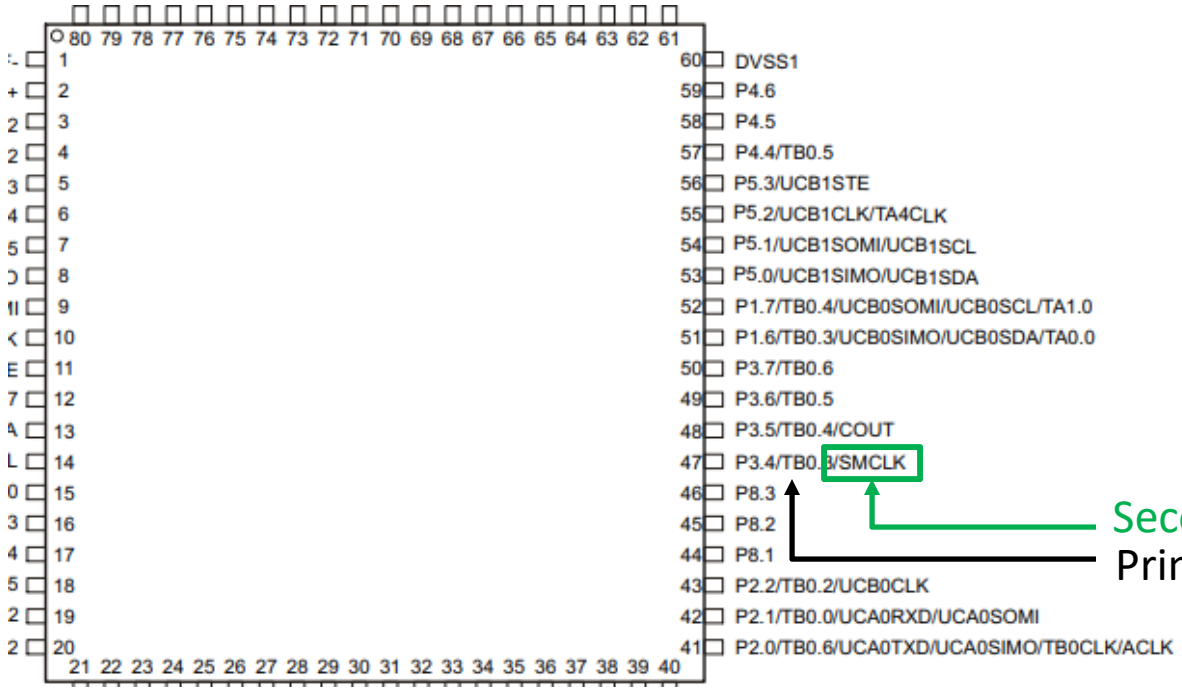
Figure 3-8. CTL3 Register

15	14	13	12	11	10	9	8
RESERVED						DIVA	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	DIVS			RESERVED	DIVM		
R-0h	R/W-3h			R-0h	R/W-3h		

Table 3-7. CTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved. Always reads as 0.
10-8	DIVA	R/W	0h	ACLK source divider. Divides the frequency of the ACLK clock source 0h (R/W) = 1 : /1 1h (R/W) = 2 : /2 2h (R/W) = 4 : /4 3h (R/W) = 8 : /8 4h (R/W) = 16 : /16 5h (R/W) = 32 : /32
7	RESERVED	R	0h	Reserved. Always reads as 0.
6-4	DIVS	R/W	3h	SMCLK source divider. Divides the frequency of the SMCLK clock source 0h (R/W) = 1 : /1 1h (R/W) = 2 : /2 2h (R/W) = 4 : /4 3h (R/W) = 8 : /8 4h (R/W) = 16 : /16 5h (R/W) = 32 : /32
3	RESERVED	R	0h	Reserved. Always reads as 0.
2-0	DIVM	R/W	3h	MCLK source divider. Divides the frequency of the MCLK clock source 0h (R/W) = 1 : /1 1h (R/W) = 2 : /2 2h (R/W) = 4 : /4 3h (R/W) = 8 : /8 4h (R/W) = 16 : /16 5h (R/W) = 32 : /32

CS12	***CS Module***
Category	Functional
Function	DCO overshoot at frequency change
Description	When changing frequencies (CSCTL1.DCOFSEL), the DCO frequency may overshoot and exceed the datasheet specification. After a time period of 10us has elapsed, the frequency overshoot settles down to the expected range as specified in the datasheet. The overshoot occur when switching to and from any DCOFSEL setting and impacts all peripherals using the DCO as a clock source. A potential impact can also be seen on FRAM accesses, since the overshoot may cause a temporary violation of FRAM access and cycle time requirements.
Workaround	When changing the DCO settings, use the following procedure: 1) Store the existing CSCTL3 divider into a temporary unsigned 16-bit variable 2) Set CSCTL3 to divide all corresponding clock sources by 4 or higher 3) Change DCO frequency 4) Wait ~10us 5) Restore the divider in CSCTL3 to the setting stored in the temporary variable. The following code example shows how to increase DCO to 16MHz.


80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61
1
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21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40
60 DVSS1
59 P4.6
58 P4.5
57 P4.4/TB0.5
56 P5.3/UCB1STE
55 P5.2/UCB1CLK/TA4CLK
54 P5.1/UCB1SOMI/UCB1SCL
53 P5.0/UCB1SIMO/UCB1SDA
52 P1.7/TB0.4/UCB0SOMI/UCB0SCL/TA1.0
51 P1.6/TB0.3/UCB0SIMO/UCB0SDA/TA0.0
50 P3.7/TB0.6
49 P3.6/TB0.5
48 P3.5/TB0.4/COUT
47 P3.4/TB0.3/SMCLK
46 P8.3
45 P8.2
44 P8.1
43 P2.2/TB0.2/UCB0CLK
42 P2.1/TB0.0/UCA0RXD/UCA0SOMI
41 P2.0/TB0.6/UCA0TXD/UCA0SIMO/TB0CLK/ACLK
Secondary module function
Primary module function

12.2.5 *Function Select Registers (PxSEL0, PxSEL1)*

Port pins are often multiplexed with other peripheral module functions. See the device-specific data sheet to determine pin functions. Each port pin uses two bits to select the pin function – I/O port or one of the three possible peripheral module function. Table 12-2 shows how to select the various module functions. See the device-specific data sheet to determine pin functions. Each PxSEL bit is used to select the pin function – I/O port or peripheral module function.

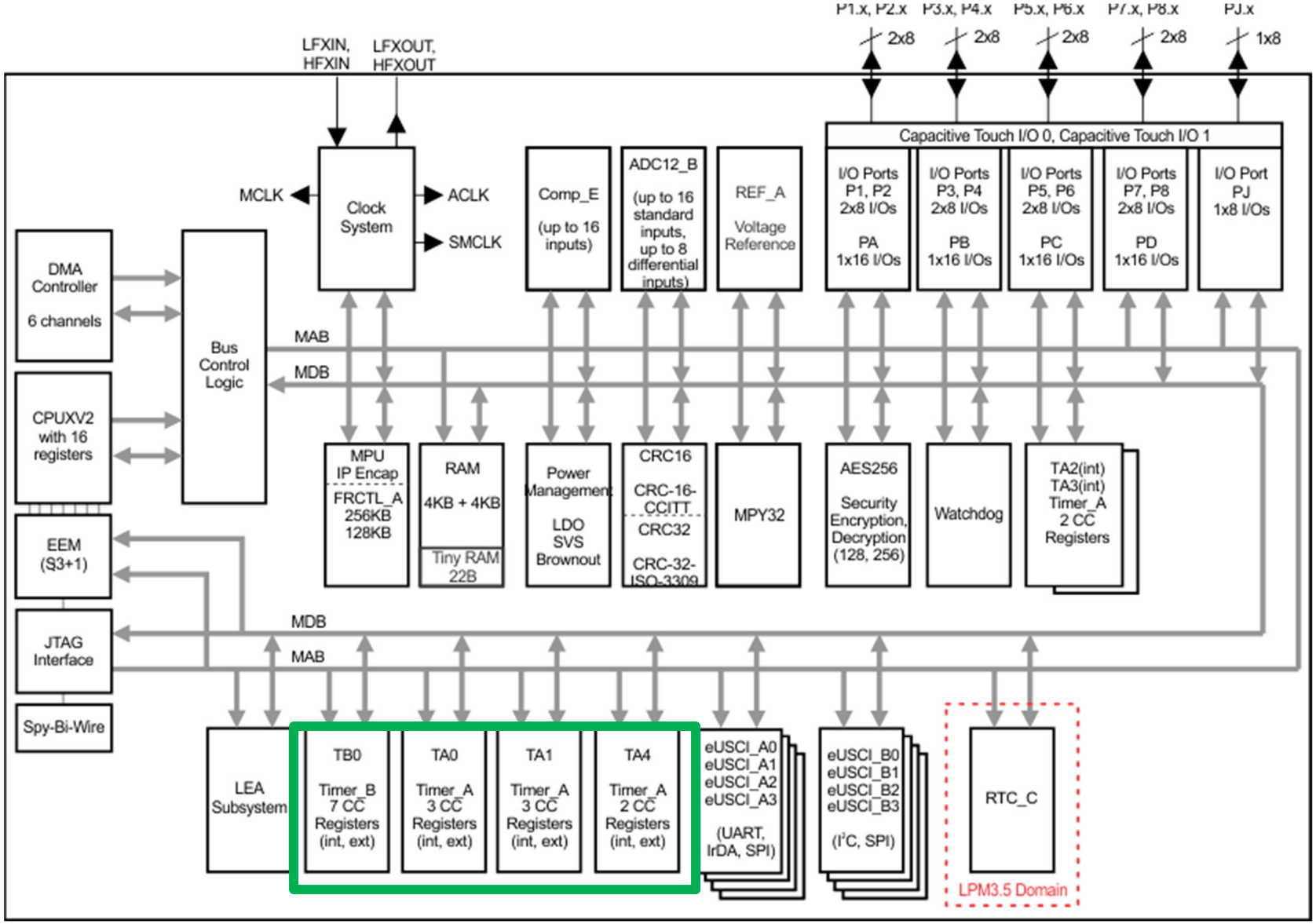
Table 12-2. I/O Function Selection

PxSEL1	PxSEL0	I/O Function
0	0	General purpose I/O is selected
0	1	Primary module function is selected
1	0	Secondary module function is selected
1	1	Tertiary module function is selected

Setting the PxSEL1 or PxSEL0 bits to a module function does not automatically set the pin direction. Other peripheral module functions may require the PxDIR bits to be configured according to the direction needed for the module function. See the pin schematics in the device-specific data sheet.

When a port pin is selected as an input to peripheral modules, the input signal to those peripheral modules is a latched representation of the signal at the device pin. While PxSEL1 and PxSEL0 is other than 00, the internal input signal follows the signal at the pin for all connected modules. However, if PxSEL1 and PxSEL0 = 00, the input to the peripherals maintain the value of the input signal at the device pin before the PxSEL1 and PxSEL0 bits were reset.

Because the PxSEL1 and PxSEL0 bits do not reside in contiguous addresses, changing both bits at the same time is not possible. For example, an application might need to change P1.0 from general purpose I/O to the tertiary module function residing on P1.0. Initially, P1SEL1 = 00h and P1SEL0 = 00h. To change the function, it would be necessary to write both P1SEL1 = 01h and P1SEL0 = 01h. This is not possible without first passing through an intermediate configuration, and this configuration may not be desirable from an application standpoint. The PxSELC complement register can be used to handle such situations. The PxSELC register always reads 0. Each set bit of the PxSELC register complements the corresponding respective bit of the PxSEL1 and PxSEL0 registers. In the example, with P1SEL1 = 00h and P1SEL0 = 00h initially, writing P1SELC = 01h causes P1SEL1 = 01h and P1SEL0 = 01h to be written simultaneously.


P1.x, P2.x
P3.x, P4.x
P5.x, P6.x
P7.x, P8.x
PJ.x
2x8
2x8
2x8
2x8
1x8
LFXIN, HFXIN
LFXOUT, HFXOUT
Capacitive Touch I/O 0, Capacitive Touch I/O 1
MCLK
Clock System
ACLK
SMCLK
Comp_E
(up to 16 inputs)
ADC12_B
(up to 16 standard inputs, up to 8 differential inputs)
REF_A
Voltage Reference
I/O Ports P1, P2 2x8 I/Os
PA 1x16 I/Os
I/O Ports P3, P4 2x8 I/Os
PB 1x16 I/Os
I/O Ports P5, P6 2x8 I/Os
PC 1x16 I/Os
I/O Ports P7, P8 2x8 I/Os
PD 1x16 I/Os
I/O Port PJ 1x8 I/Os
DMA Controller 6 channels
Bus Control Logic
MAB
MDB
CPUXV2 with 16 registers
MPU IP Encap
FRCTL_A 256KB 128KB
RAM
4KB + 4KB
Tiny RAM 22B
Power Management
LDO SVS Brownout
CRC16
CRC-16-CCITT
CRC32
CRC-32-ISO-3309
MPY32
AES256
Security Encryption, Decryption (128, 256)
Watchdog
TA2(int) TA3(int) Timer_A 2 CC Registers
EEM (S3+1)
JTAG Interface
Spy-Bi-Wire
MDB
MAB
LEA Subsystem
TB0
Timer_B 7 CC Registers (int, ext)
TA0
Timer_A 3 CC Registers (int, ext)
TA1
Timer_A 3 CC Registers (int, ext)
TA4
Timer_A 2 CC Registers (int, ext)
eUSCI_A0
eUSCI_A1
eUSCI_A2
eUSCI_A3
(UART, IrDA, SPI)
eUSCI_B0
eUSCI_B1
eUSCI_B2
eUSCI_B3
(I²C, SPI)
RTC_C
LPM3.5 Domain

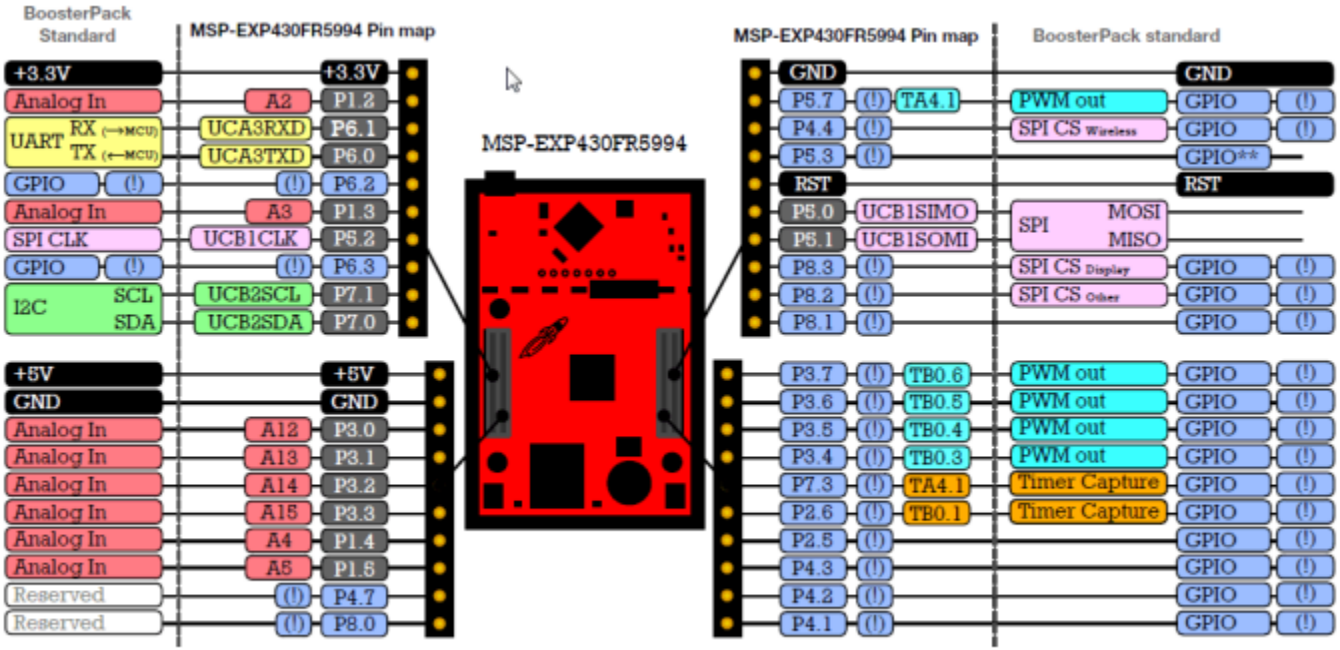


Figure 2-10. LaunchPad Development Kit to BoosterPack Plug-in Module Connector Pinout

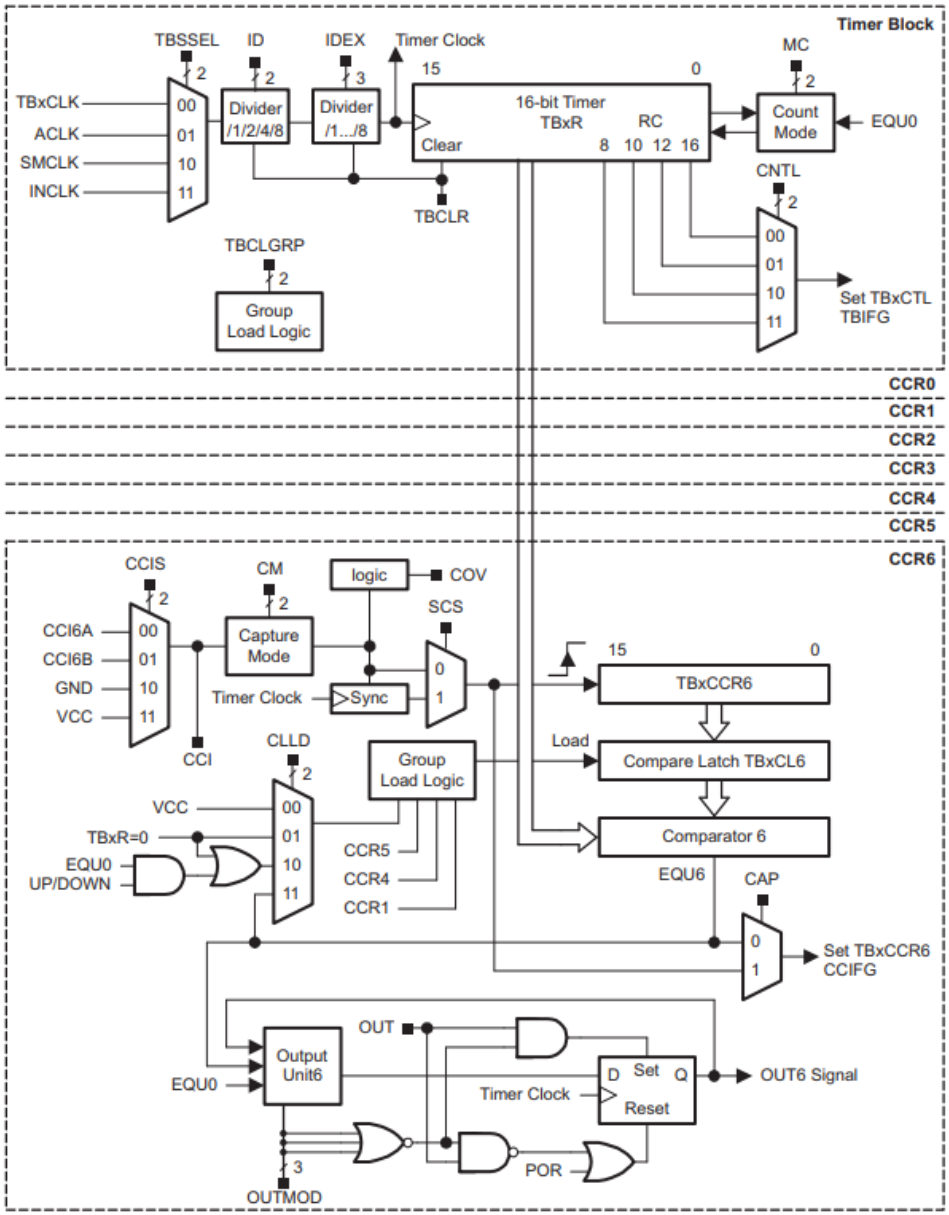


Figure 26-1. Timer_B Block Diagram

26.2.5.1.1 Output Example – Timer in Up Mode

The OUTn signal is changed when the timer *counts* up to the TBxCLn value, and rolls from TBxCL0 to zero, depending on the output mode. An example is shown in Figure 26-12 using TBxCL0 and TBxCL1.

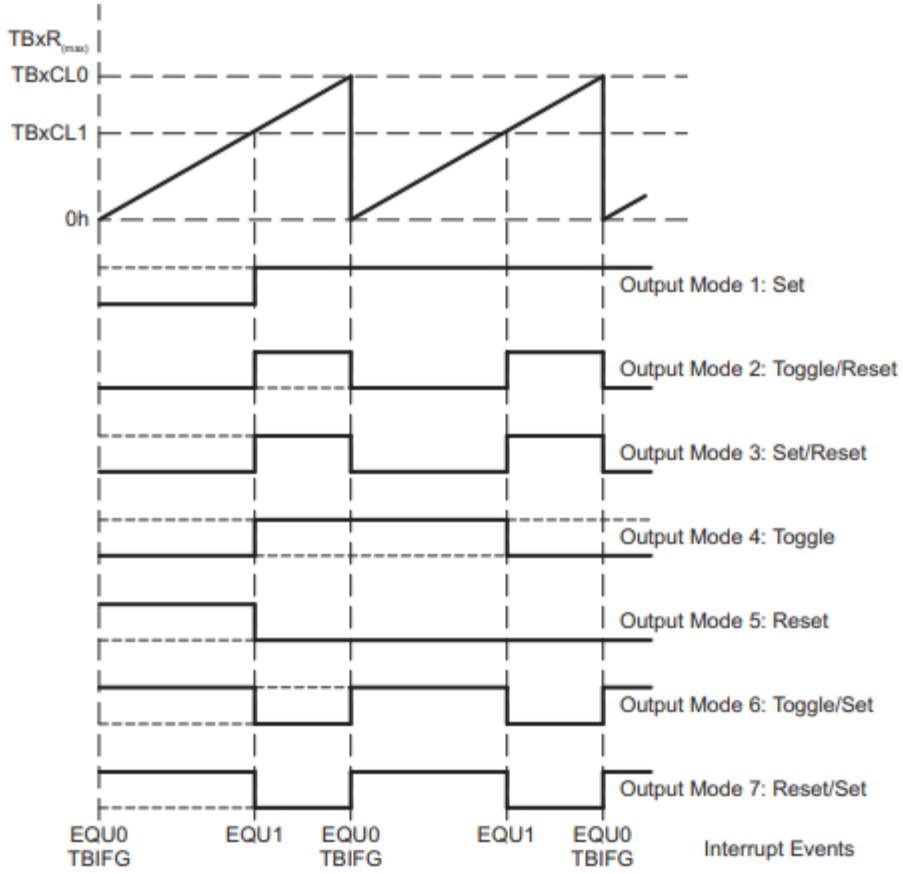


Figure 26-12. Output Example – Timer in Up Mode

26.3 Timer_B Registers

The Timer_B registers are listed in Table 26-5. The base address can be found in the device-specific data sheet. The address offset is listed in Table 26-5.

Table 26-5. Timer_B Registers

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	TBxCTL	Timer_B Control	Read/write	Word	0000h	Section 26.3.1
02h	TBxCCTL0	Timer_B Capture/Compare Control 0	Read/write	Word	0000h	Section 26.3.3
04h	TBxCCTL1	Timer_B Capture/Compare Control 1	Read/write	Word	0000h	Section 26.3.3
06h	TBxCCTL2	Timer_B Capture/Compare Control 2	Read/write	Word	0000h	Section 26.3.3
08h	TBxCCTL3	Timer_B Capture/Compare Control 3	Read/write	Word	0000h	Section 26.3.3
0Ah	TBxCCTL4	Timer_B Capture/Compare Control 4	Read/write	Word	0000h	Section 26.3.3
0Ch	TBxCCTL5	Timer_B Capture/Compare Control 5	Read/write	Word	0000h	Section 26.3.3
0Eh	TBxCCTL6	Timer_B Capture/Compare Control 6	Read/write	Word	0000h	Section 26.3.3
10h	TBxR	Timer_B Counter	Read/write	Word	0000h	Section 26.3.2
12h	TBxCCR0	Timer_B Capture/Compare 0	Read/write	Word	0000h	Section 26.3.4
14h	TBxCCR1	Timer_B Capture/Compare 1	Read/write	Word	0000h	Section 26.3.4
16h	TBxCCR2	Timer_B Capture/Compare 2	Read/write	Word	0000h	Section 26.3.4
18h	TBxCCR3	Timer_B Capture/Compare 3	Read/write	Word	0000h	Section 26.3.4
1Ah	TBxCCR4	Timer_B Capture/Compare 4	Read/write	Word	0000h	Section 26.3.4
1Ch	TBxCCR5	Timer_B Capture/Compare 5	Read/write	Word	0000h	Section 26.3.4
1Eh	TBxCCR6	Timer_B Capture/Compare 6	Read/write	Word	0000h	Section 26.3.4
2Eh	TBxIV	Timer_B Interrupt Vector	Read only	Word	0000h	Section 26.3.5
20h	TBxEX0	Timer_B Expansion 0	Read/write	Word	0000h	Section 26.3.6

26.3.1 TBxCTL Register

Timer_B x Control Register

Figure 26-16. TBxCTL Register

15	14	13	12	11	10	9	8
Reserved	TBCLGRPx		CNTL		Reserved	TBSSEL	
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
ID		MC		Reserved	TBCLR	TBIE	TBIFG
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	w-(0)	rw-(0)	rw-(0)

Table 26-6. TBxCTL Register Description

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads as 0.
14-13	TBCLGRP	RW	0h	TBxCLn group 00b = Each TBxCLn latch loads independently. 01b = TBxCL1+TBxCL2 (TBxCCR1 CLLD bits control the update); TBxCL3+TBxCL4 (TBxCCR3 CLLD bits control the update); TBxCL5+TBxCL6 (TBxCCR5 CLLD bits control the update); TBxCL0 independent 10b = TBxCL1+TBxCL2+TBxCL3 (TBxCCR1 CLLD bits control the update); TBxCL4+TBxCL5+TBxCL6 (TBxCCR4 CLLD bits control the update); TBxCL0 independent 11b = TBxCL0+TBxCL1+TBxCL2+TBxCL3+TBxCL4+TBxCL5+TBxCL6 (TBxCCR1 CLLD bits control the update)
12-11	CNTL	RW	0h	Counter length 00b = 16-bit, TBxR(max) = 0FFFFh 01b = 12-bit, TBxR(max) = 0FFFh 10b = 10-bit, TBxR(max) = 03FFh 11b = 8-bit, TBxR(max) = 0FFh
10	Reserved	R	0h	Reserved. Always reads as 0.
9-8	TBSSEL	RW	0h	Timer_B clock source select 00b = TBxCLK 01b = ACLK 10b = SMCLK 11b = INCLK
7-6	ID	RW	0h	Input divider. These bits, along with the TBIDEX bits, select the divider for the input clock. 00b = /1 01b = /2 10b = /4 11b = /8
5-4	MC	RW	0h	Mode control. Setting MC = 00h when Timer_B is not in use conserves power. 00b = Stop mode: Timer is halted 01b = Up mode: Timer counts up to TBxCL0 10b = Continuous mode: Timer counts up to the value set by CNTL 11b = Up/down mode: Timer counts up to TBxCL0 and down to 0000h
3	Reserved	R	0h	Reserved. Always reads as 0.
2	TBCLR	RW	0h	Timer_B clear. Setting this bit clears TBR, the clock divider logic (the divider setting remains unchanged), and the count direction. The TBCLR bit is automatically reset and is always read as zero.
1	TBIE	RW	0h	Timer_B interrupt enable. This bit enables the TBIFG interrupt request. 0b = Interrupt disabled 1b = Interrupt enabled

26.3.3 TBxCCTLn Register

Timer_B x Capture/Compare Control Register n

Figure 26-18. TBxCCTLn Register

15	14	13	12	11	10	9	8
CM		CCIS		SCS	CLLD		CAP
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
OUTMOD			CCIE	CCI	OUT	COV	CCIFG
rw-(0)	rw-(0)	rw-(0)	rw-(0)	r	rw-(0)	rw-(0)	rw-(0)

Table 26-8. TBxCCTLn Register Description

Bit	Field	Type	Reset	Description
15-14	CM	RW	0h	Capture mode 00b = No capture 01b = Capture on rising edge 10b = Capture on falling edge 11b = Capture on both rising and falling edges
13-12	CCIS	RW	0h	Capture/compare input select. These bits select the TBxCCRn input signal. See the device-specific data sheet for specific signal connections. 00b = CCIxA 01b = CCIxB 10b = GND 11b = VCC
11	SCS	RW	0h	Synchronize capture source. This bit is used to synchronize the capture input signal with the timer clock. 0b = Asynchronous capture 1b = Synchronous capture
10-9	CLLD	RW	0h	Compare latch load. These bits select the compare latch load event. 00b = TBxCLn loads on write to TBxCCRn 01b = TBxCLn loads when TBxR counts to 0 10b = TBxCLn loads when TBxR counts to 0 (up or continuous mode). TBxCLn loads when TBxR counts to TBxCL0 or to 0 (up/down mode). 11b = TBxCLn loads when TBxR counts to TBxCLn
8	CAP	RW	0h	Capture mode 0b = Compare mode 1b = Capture mode
7-5	OUTMOD	RW	0h	Output mode. Modes 2, 3, 6, and 7 are not useful for TBxCL0 because EQUn = EQU0. 000b = OUT bit value 001b = Set 010b = Toggle/reset 011b = Set/reset 100b = Toggle 101b = Reset 110b = Toggle/set 111b = Reset/set
4	CCIE	RW	0h	Capture/compare interrupt enable. This bit enables the interrupt request of the corresponding CCIFG flag. 0b = Interrupt disabled 1b = Interrupt enabled
3	CCI	R	Undef	Capture/compare input. The selected input signal can be read by this bit.