Revision summary:

October 14th – Original document

TiNY BOX CHALLENGE

Introduction

The Tiny Box Competition is a hardware design competition, part of ECE 581: Power Electronics in Fall 2020. The goal of the competition is to design, build, and test in open-loop a high efficiency, high power-density DC-DC converter leveraging techniques discussed in class.

Questions regarding the competition requirements should be discussed in class or in the public Slack channel, so that all competitors have equal knowledge of the competition expectations. Questions may be e-mailed to the instructor at any time, and will be discussed at the start of class the following lecture. Answers to select questions will be posted on the course website.

This document may be modified periodically to reflect questions/clarifications/alterations in response to questions. All students in the course will receive an e-mail when this document is updated.

High Level Competition Specifications

The winning converter will be the unit which achieves the highest power density, i.e. fits in the smallest rectangular volume, while meeting the following specifications. All specifications must be demonstrated experimentally. In the event of a tie on volume, efficiency will be used to determine the winner.

Parameter	Requirement	Comment
Voltage Input	48 Vdc	
Maximum Output Power	36 W	
Output Voltage	12 ± 0.1 Vdc	
Output Ripple Voltage	< 1%	Measured as $V_{pk\text{-}pk}/V_{avg}$ from the DC supply, in steady state, at full output power
TPE Efficiency	> 95%	Measured using TPE method[1]
No-load Power Loss	< 2W	Measured with load disconnected, but output voltage within specified range
Volume	< 3.6 in^3	Volume of minimum rectangle enclosing power stage

[1]Tennessee Power Electronics (TPE) efficiency is a weighted power efficiency defined as:

$$\eta_{TPEF} = 0.1\eta_{P_{out}=0.25\cdot P_{max}} + 0.15\eta_{P_{out}=0.5\cdot P_{max}} + 0.25\eta_{P_{out}=0.75\cdot P_{max}} + 0.5\eta_{P_{out}=P_{max}}$$

Required Construction Details

For this competition, the design and prototype construction considers only the power stage, consisting of power semiconductor devices, passives, and gate drivers. Any requirements for additional isolated/non-isolated gate driver power supplies do not count towards total converter volume. No closed-loop control is

required; the converter can be tested in open-loop at the various operating points necessary for the TPEF efficiency measurement, one-at-a-time.

The assessed volume of your converter is the volume of the minimum rectangular volume which encloses all components listed above. You may choose to make your PCB larger than this volume in order to include additional test points or connections for signals. If you choose to do so, a rectangle on the top silkscreen layer must be used to indicate the extent of the power stage.

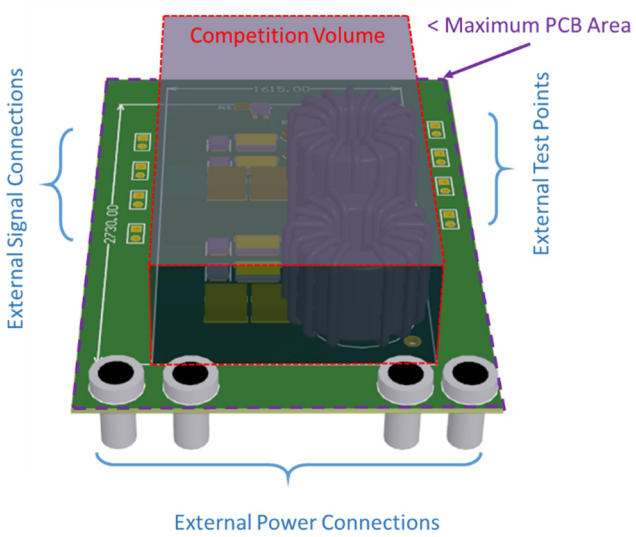

Fig. 1: Example hardware entry

Converter Realization

Converter Components

All components used in the initial converter design must be commercially available, and in stock at the time of purchasing. Digikey and Mouser are preferred vendors for general components.

Magnetics

If your converter contains magnetics of your own design, the cores must be available for commercial purchase in low quantities. Vendors of magnetic cores from multiple companies include

- Elna Magnetics (http://www.elnamagnetics.com/)
- Allstar Magnetics (http://allstarmagnetics.com/)
- Dexter Magnetics (http://www.dextermag.com/)

A limited selection of magnetic cores, as well as discrete inductors, are available from Digikey and Mouser.

The total cost of components for your converter is not to exceed **$100**.

PCB

Printed Circuit Boards will be ordered on the date specified on the course schedule. All circuit boards will be ordered with Sierra Circuits' NoTouch, 4-layer specifications. Details are given at https://www.protoexpress.com/NoTouch-pcb/product-specs.jsp, except as specified below

Parameter	Requirement
Maximum Area[1]	10 in^2
Maximum single dimension[1]	6 in
Minimum trace/space	6 mil
Minimum finished hole size	15 mil
Board Outline	Top Soldermask; Must be a closed rectangle

[1]maximum dimensions apply to the complete board, including power stage and any additional testing/connection in the layout.

Each competitor will receive one (1) copy of their PCB layout. Prior to submission, each layout must successfully pass the AFV check here: https://www.protoexpress.com/orderProc/noTouchNew.jsp, with no issues found.

The total cost of the PCB for your converter is not to exceed **$200**.

Total Cost of Prototype

Total construction of the prototype converter is limited to $300, for both components and PCB. With permission, you may exceed the components or PCB budget above, but the total must be under $300. Discuss with the instructor if you feel this limit impedes your ability to realize your design

Measurement Procedure

All measurements taken in order to verify the converter performance experimentally must be taken after the converter has been operating in steady-state for more than 60 seconds to ensure thermal stability. Ripple requirements need only be measured at full output power.

To obtain accurate measurements, be sure to employ Kelvin voltage sensing, particularly at the high-current output port.

Additional Resources

Each competitor will be given access to sufficient testing equipment as needed outside of students' current access

Additionally, a modulator board will be provided upon request to competitors choosing to use it to generate (signal-level) modulation signals. Competitors electing not to use this board may use any source of modulation signals and auxiliary power they choose, so long as all other requirements are met. The available platform consists of

1. 8 isolated power and signal connectors each containing
    a. a 5V digital modulation signal
    b. a 15V supply

    c. an adjustable voltage-level supply, derived using a linear regulator from (b)
    d. an isolated ground ("common")
2. A Mojo v3 FPGA board, using a Xilinx Spartan-6 FPGA
3. Code for the Mojo v3 to produce eight arbitrary pulsating signals

The 8 isolated connectors are arranged as follows

- 4 connectors are independently isolated, each to their own separate "common"
- 4 connectors are isolated relative to the FPGA, but all share a single common ground

In all cases, loads powered by an individual connector can consume no more than 70mAdc.

To connect to the board, competitors may choose to employ a mating connection on their PCB using 100mil-spacing, 4-position, single-row female headers, or by purchasing wires with equivalent housing. In any event, any components needed for connection must be included in the submitted BOMs.

PCB layout for mating connection spacing is available in the PCB starter files on the course website.

Assignments and Schedule

Due to the COVID-19 pandemic, the Tiny Box Challenge has been revised in Fall 2020. Students may choose either Option 1 (Full prototyping) or Option 2 (design only + written final exam), below. This decision must be made prior to November 13th and cannot be changed thereafter.

Option 1: Full Prototyping

In this option, students **will not** take a written final exam. The testing report will take the place of the final exam grade.

Competition Schedule

- October 14th – Competition Begins
- October 30th – Paper Design and Comparison Report Due
- November 13th – PCB Layout Due
- December 9th – Testing Report Due

All assignments are completed individually. All deliverables are due at the start of class on the specified date.

Paper Design and Comparison Report (*Due October 30th*)

A minimum of three (3) topologies must be considered. Among the topologies selected for consideration, at least one must be from each of Class III and Class IV, as defined by the table below. Selection of a Class IV topology will likely require examination of the relevant literature.

	Class I	Class II	Class III	Class IV
Definition	Two-switch PWM topologies*	Isolated variants of PWM topologies	AC-link topologies	Any topology not conforming to Class I-III
Examples	Buck, Boost, Buck-Boost, Cuk, SEPIC, etc.	Flyback, Forward, push-pull, half-bridge, full-bridge	DAB, DAHB, SRC, LLC, Full Bridge, etc.	Switched capacitor, sigma-delta, multilevel, etc.

* a hard-switched Class-I topology may not be used.

For each topology, the competitor must solve the converter operation for all parameters necessary to examine operation in steady-state (Average and RMS currents, modulation signals, peak voltage stresses, passive sizing, etc.). Additionally, competitors must state and justify predictions for converter performance in terms of

1. Efficiency at full power
2. Power loss at zero load
3. Output voltage ripple
4. Volume of main passive components

Optimization (component selection, switching frequency, passive realization) *does not* need to be completed, but the predictions must be made for real component values and a specific operating scenario.

In addition to the analysis of these three topologies, the competitors must provide a discussion of the relative merits of each, and propose one of the selected topologies for construction.

For the single, selected topology, competitors must report on the process and results of optimization to meet all specifications with the minimum total volume. This includes justification and final selection of

1. Power Devices
2. Gate Driver Circuitry
3. Passive Devices and implementation

4. Switching Frequency

The report must include a complete converter schematic with part numbers for all devices. No additional narrative is required for this report other than the technical results mentioned in this document

PCB Layout Submission (*Due November 13nd*)

Competitors must submit, through canvas, one .zip archive of the completed PCB layout. The layout must successfully pass Sierra Circuits' AFV check prior to submission. The zip archive should contain the following file types from the Altium project:

1. PrjPcb
2. SchDoc
3. SchLib
4. PcbLib
5. PcbDoc

Also in canvas, submit your username and password (make sure to change your password to something not used for any other personal account) to the Sierra Circuits webpage. Prior to submission, move all quotes *except* the one final board which has passed AFV to your old/hidden folder. The quote should be specified with

- 4-day turn
- 6 mil minimum trace/space
- 15 mil hole size
- 1 board quantity
- (up to) 4 layers

Note: Sierra Circuits' AFV process may be unable to complete outside of business hours if the board has issues that cannot be resolved in an automated manner. Plan to complete your layout well before the deadline to ensure that an error-free AFV can be submitted before the deadline.

Additionally, competitors must submit one (1) spreadsheet containing the parts required to construct the PCB. An example file will be posted on the course webpage. The columns, order, and formatting must match the example file exactly, and must show that the sum of costs for all components ordered is such that the total cost with PCB fabrication is below $300.

For all parts that the competitors are requesting to be ordered, competitors must submit immediately actionable resources for ordering. For vendors including Digikey and Mouser, this can be achieved by links to carts. For other vendors, quote documentation with ordering information will suffice.

Testing Report (*Due December 9th*)

The testing report contains only a listing of the objective testing results of the converter. An example template is posted to the course website. The submitted document must follow the template format exactly.

Option 2: Design Only

In this option, students **will** take a final written exam.

Competition Schedule

- October 14th – Competition Begins
- October 30th – Paper Design and Comparison Report Due
- November 13th – *Partial* PCB Layout Due
- December 2nd – 9th – Final Written Exam

All assignments are completed individually. All deliverables are due at the start of class on the specified date.

Paper Design and Comparison Report (*Due October 30th*)

Requirements for this deliverable are the same as given in Option I

PCB Layout Submission (*Due November 13nd*)

Competitors must submit, through canvas, one .zip archive of the completed PCB layout. The zip archive should contain the following file types from the Altium project:

6. PrjPcb
7. SchDoc
8. SchLib
9. PcbLib
10. PcbDoc

Additionally, competitors must submit one (1) spreadsheet containing the parts required to construct the PCB. An example file is posted on the course webpage. The columns, order, and formatting must match the example file exactly, and must show that the sum of costs for all components ordered is such that the total cost with PCB fabrication is below $300.

The layout **does not** need to be complete/routed, but must have all major components included and arranged in a manner that would allow a well-routed solution. The total board area and height should be clearly labeled in the layout. This PCB **will no**t be fabricated, but serves as the final design in this option to show the approximated volume of the solution, and show that the cost requirements have been met.

Final Written Exam (*Due December 9th*)

A written take-home exam will be administered, starting on December 2nd. Students selecting Option 2 will be required to complete the exam by December 9th.