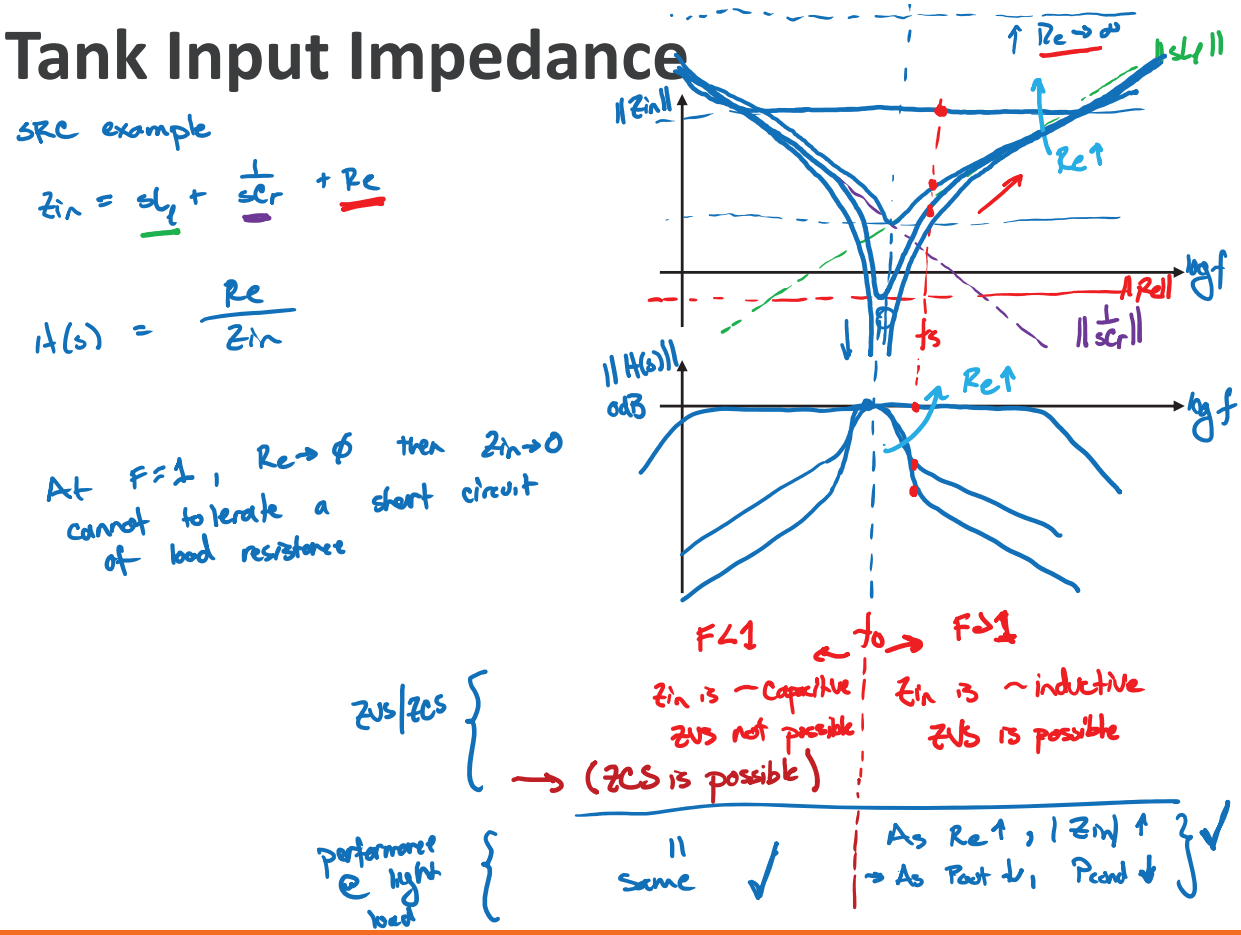
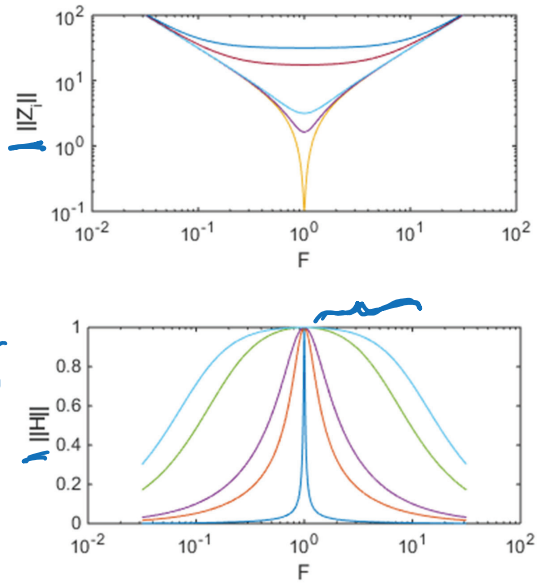
Tank Input Impedance



Series Resonant Tank



TiNY BOX CHALLENGE

Competition Specifications

The **winning converter** will be the unit which achieves the **highest power density**, i.e. fits in the smallest rectangular volume, while meeting the following specifications.

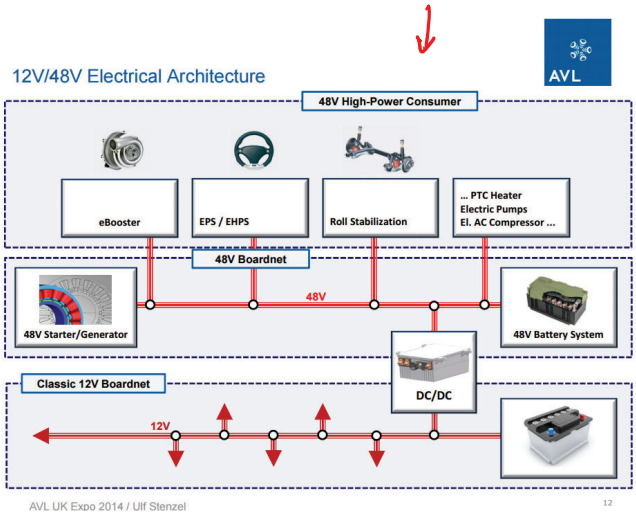
Parameter	Requirement	Comment
Voltage Input	48 Vdc	
Maximum Output Power	36 W	
Output Voltage	12 ± 0.1 Vdc	
Output Ripple Voltage	< 1%	Measured as $V_{pk\text{-}pk}/V_{avg}$ from the DC supply, in steady state, at full output power
TPE Efficiency	> 95%	Measured using TPE method[1]
No-load Power Loss	< 2W	Measured with load disconnected, but output voltage within specified range
Volume	< 3.6 in^3	Volume of minimum rectangle enclosing power stage

[1]Tennessee Power Electronics (TPE) efficiency is a weighted power efficiency defined as:

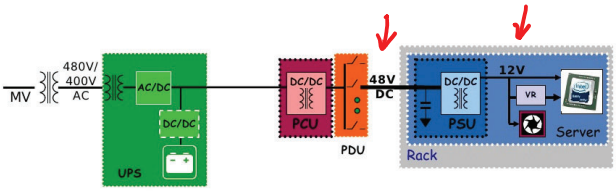
$$\eta_{TPEF} = 0.1\eta_{P_{out}=0.25\cdot P_{max}} + 0.15\eta_{P_{out}=0.5\cdot P_{max}} + 0.25\eta_{P_{out}=0.75\cdot P_{max}} + 0.5\eta_{P_{out}=P_{max}}$$

Example Applications

EV 48V Architectures



Data Centers / Telecom



NXP Semi, "Semiconductors – enablers of future mobility concepts", 2011
Audi, "Electric biturbo and hybridization", 2014
AVL, "48V Mild Hybrid Systems"

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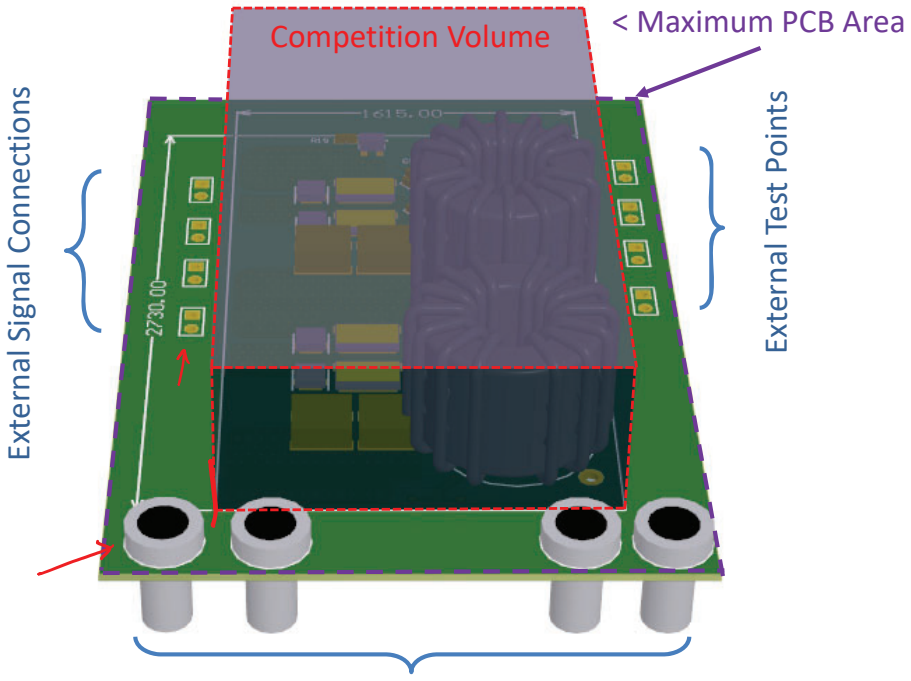
How Volume is Measured



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Additional Details

- Full competition specifications and example testing report on course webpage
- No regulation requirements
- Deliverables:
  - Written design comparison of 3 topologies (10/30)
  - PCB Layout of single design (11/13)*
  - Testing Report of prototype (12/9)**

Pandemic Modifications

- Traditionally, ECE 581 has experimental testing of converter (in groups of 2-3) and Final written Exam
- This semester, you may
  - Prototype and test converter design (individual)

    - or -

  - Take final written exam
- Everyone must complete the initial design comparison report and “block” PCB layout

Design and Comparison Report (10/30)

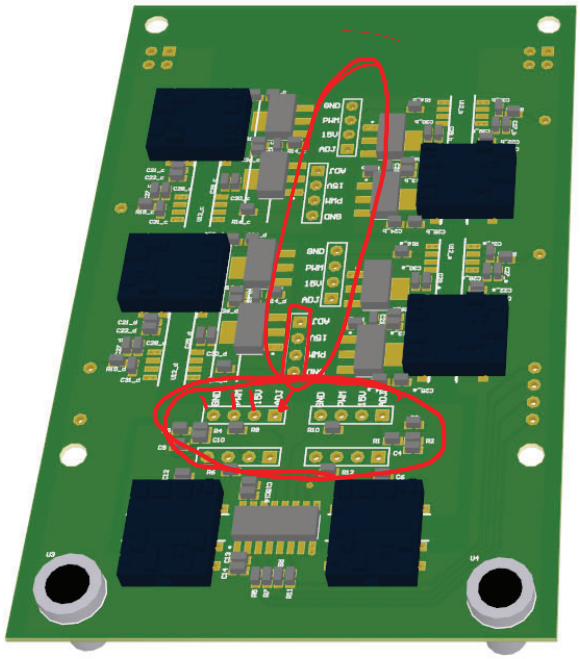
1. Select three topologies from the table and compare based on
   I. Efficiency at full power
   II. Power loss at zero load
   III. Output voltage ripple
   IV. Volume of main passive components

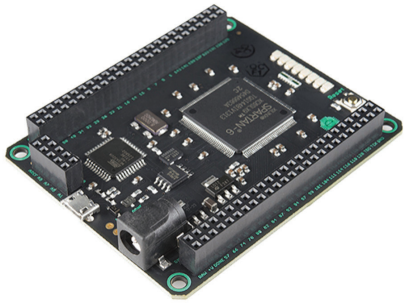
	Class I	Class II	Class III	Class IV
Definition	Two-switch PWM topologies*	Isolated variants of PWM topologies	AC-link topologies	Any topology not conforming to Class I-III
Examples	Buck, Boost, Buck-Boost, Cuk, SEPIC, etc.	Flyback, Forward, push-pull, half-bridge, full-bridge	DAB, DAHB, SRC, LLC, Full Bridge, etc.	Switched capacitor, sigma-delta, multilevel, etc.
Required number	--	--	1	1

*you may **not** use a hard-switched variant of a Class I topology

2. Select (and justify) one topology, and provide a complete design including (but not limited to)
   I. Power Devices
   II. Gate Driver Circuitry
   III. Passive Devices and implementation
   IV. Switching Frequency

Modulation Signal Board





- FPGA + PWM isolation
  - 4 low-side (common ground)
  - 4 high-side (isolated grounds)
- Reference code to generate open-loop PWM signals
- Layout in Altium starter package on course website