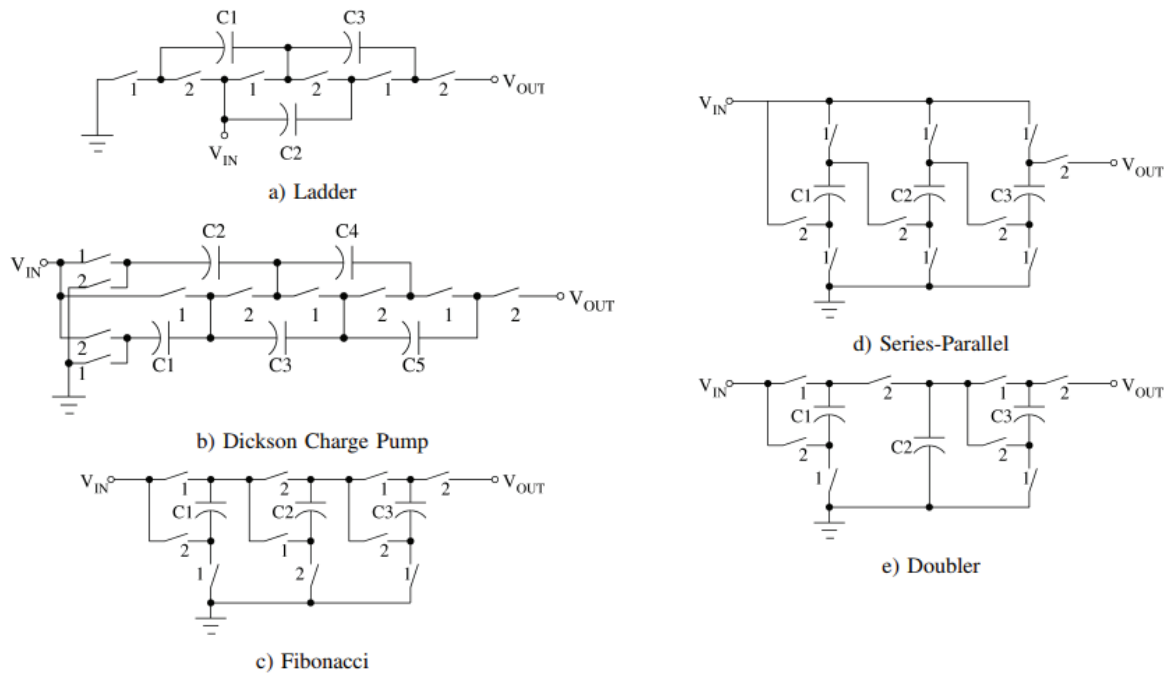
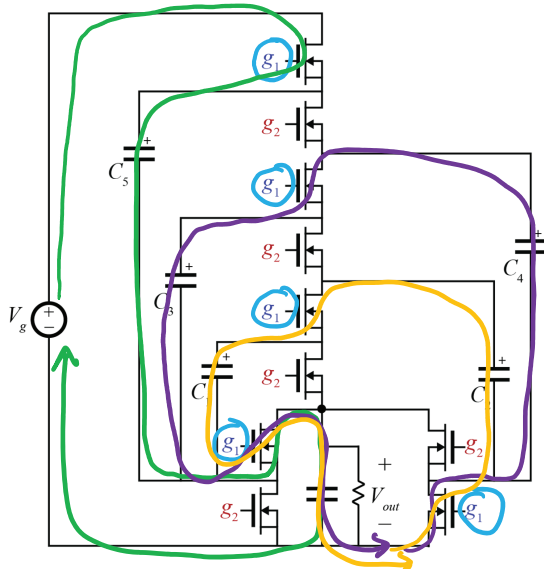


# SC Converter Topologies

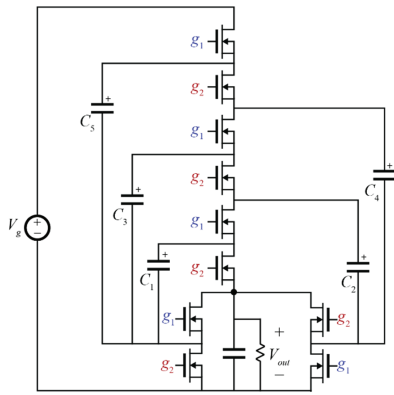


M Seeman and S. Sanders, "Analysis and Optimization of Switched-Capacitor DC-DC Converters"

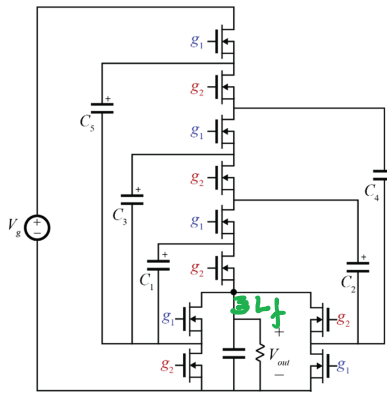
## Dickson Converter



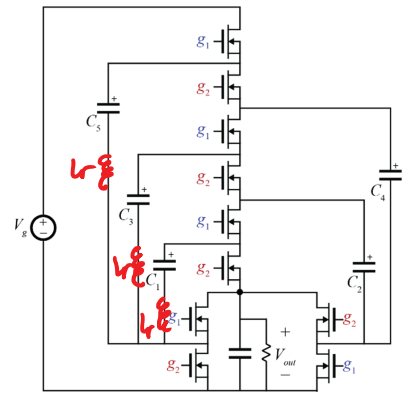
# Dickson Converter Variants



Standard Dickson  
(SSL / FSL)



Hybrid Dickson  
Add  $L_f \rightarrow$  can't get  
current-source type  
charging of all caps  
w/ just one inductor  
Regulation possible

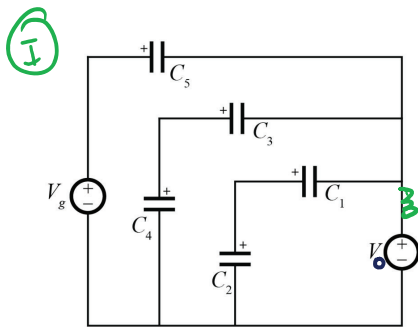


Switched Tank Converter  
Unregulated for high?  
Resonant charging of  
all caps.

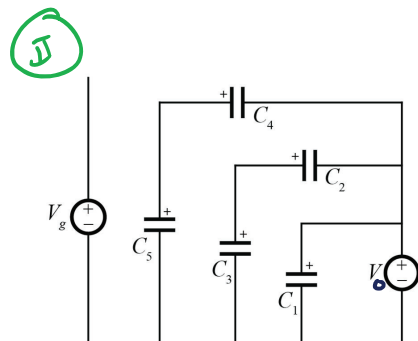
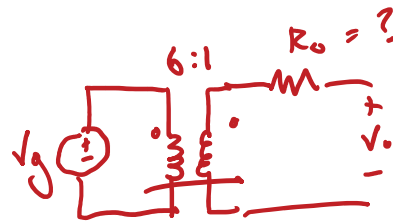
Y. Lei, R. May, and R. Pilawa-Podgurski, "Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter," 2016

Y. Li, X. Lyu, D. Cao, S. Jiang and C. Nan, "A 98.55% Efficiency Switched-Tank Converter for Data Center Application," 2018.

## Dickson Subintervals



Ideal Analysis  
- All caps have  $\sim$  zero ripple  
 $V_g = 6V_0$   
 $V_{C4} = 4V_0$   
 $V_{C2} = 2V_0$   
 $\rightarrow$  This is a 6:1 implementation



$V_{C5} = 5V_0$   
 $V_{C3} = 3V_0$   
 $V_{C1} = V_0$

# Charge Vector Analysis: Notation

Finds  $M$  &  $R_o$  for arbitrary switched cap converter  
 - Applies cap-charge balance to every capacitor in circuit

$q_x^I$  = charge into capacitor  $x$  during switching subinterval  $I$   
 $a_x^I = \frac{q_x^I}{q_{out}^I} \rightarrow$  normalized with respect to  $q_{out}^I = q_{out}^I + q_{out}^{II} + \dots$

$$\bar{a}^I = [a_{in}^I, \underbrace{a_{c1}^I, a_{c2}^I, \dots, a_{cN}^I}_{\bar{a}_c^I}, a_{out}^I]$$

$N$  = total # of caps in converter

$$\bar{v}^I = [v_g, v_{c1}^I, v_{c2}^I, \dots, v_{cN}^I, v_{out}^I]$$

$v_{c1}^I \equiv$  Voltage on  $C_1$  at the end of subinterval  $I$   
 (assumed operation in SSL)

M. Makowski and D. Maksimovic, "Performance Limits of Switched-Capacitor DC-DC Converters," 1995  
 M Seeman and S. Sanders, "Analysis and Optimization of Switched-Capacitor DC-DC Converters," 2008

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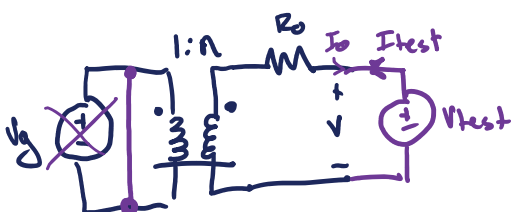
# Charge Vector Analysis: Rules

- KVL & KCL apply always
  - for all caps  $\langle i_{ci} \rangle_{T_s} = 0$  in steady-state (cap-charge balance)
- $$\frac{1}{T_s} \int_0^{T_s} i_{ci} dt = 0 \iff q_{ci}^I + q_{ci}^{II} + \dots = 0$$
- also,  $a_{ci}^I + a_{ci}^{II} + \dots = 0$

ex/ for just two subintervals,  $a_{ci}^I = -a_{ci}^{II}$

To find output resistance

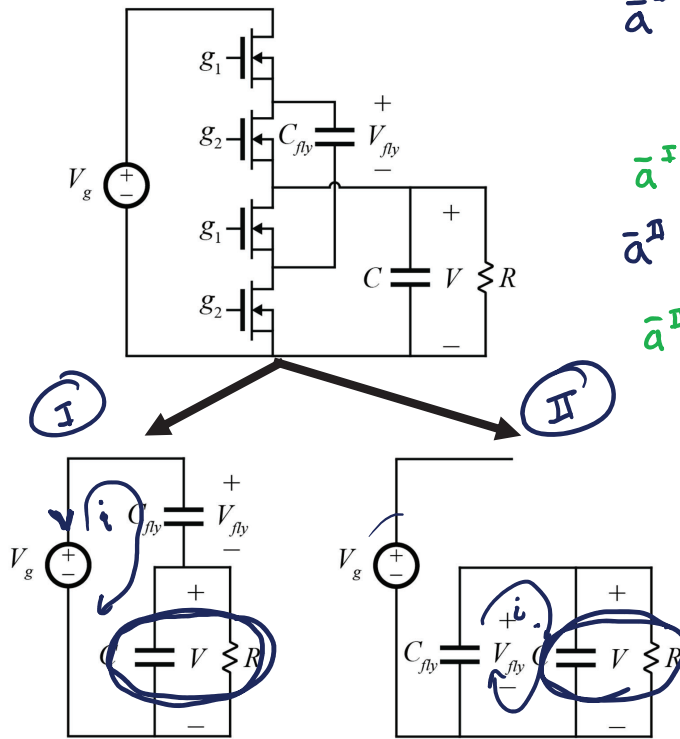
turn off  $v_g$ , apply test source at output



$$R_o = \frac{v_{test}}{i_{test}} = \frac{v}{-i_o}$$

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## 2:1 Converter Charge Vector Analysis



$$\bar{a}^I = [g_{in}^I \quad g_{fly}^I \quad g_{out}^I] / g_{out}$$

$$= [-1, 1, 1] / g_{out}$$

$$\bar{a}^I = [-1/2, 1/2, 1/2]$$

$$\bar{a}^{II} = [\phi, -1, 1] / g_{out}$$

$$\bar{a}^{II} = [0, -1/2, 1/2]$$

$$g_{out} = g_{out}^I + g_{out}^{II} = 2$$

$$a_{out} = 1 \quad (\text{always, by normalize})$$

$$a_{in} = -1/2$$

$$\rightarrow \text{Ideal conversion ratio}$$

$$m = \frac{V_g}{V_y} = -\frac{a_{in}}{a_{out}} = \frac{1}{2}$$