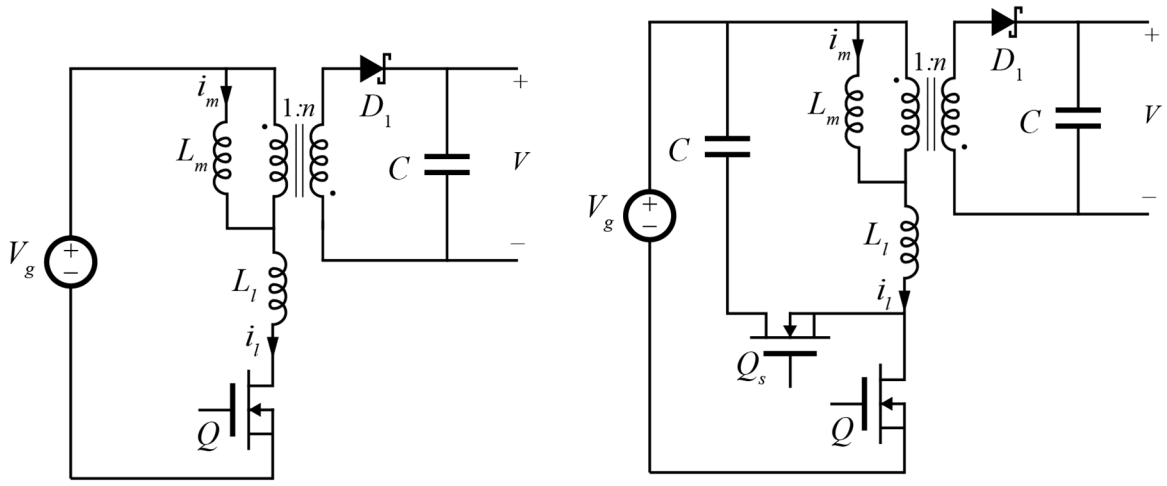
ECE581

Comparison of ZVS Flyback Topologies

Fig. 1 shows two different topologies for the flyback converter capable of achieving ZVS. In Fig. 1(a), L_m is small, allowing for greater than 100% ripple in i_m. In Fig. 1(b), L_m is large, operating with small ripple, and an active clamp circuit is included to facilitate ZVS of the main switch Q.

The transformer is modeled as illustrated: the model contains an ideal 1:n transformer, n = 0.2, a magnetizing inductance L_m, and a leakage inductance $L_l = 0.01 * L_m$. For each design, the value of L_m is different. The MOSFET output capacitance is modeled as a linear capacitance having constant value C_{ds} = 1 nF. The input voltage is V_g = 60 V, the output DC voltage is V = 12 V. Each converter has an output power of P = 60 W.

For both converters, the MOSFET drain-to-source voltage must remain below 200 V. CCM equations for flyback operation do not apply, but small-ripple approximation can be made on filter elements, where appropriate.



(a) (b)

Figure 1: Two options for soft-switching Flyback converter; QSW ZVS flyback (a) and active clamp flyback (b)

For the Active Clamp Flyback of Fig. 1(b), complete the following assuming nominal operation with ZVS, and a clamping voltage V_s = 200 V

a) Sketch time-domain waveforms of the drain-to-source voltage v_{ds} of transistor Q, and the leakage inductor current i_l.
b) Sketch the j_l-m_{ds} state. Label all salient features.
c) Derive a complete set of equations in normalized state plane notation which model the behavior of the active clamp flyback.
d) Solve for the value of L_m such that the switching frequency of the converter is 1 MHz at the specified operating point.

Note: Keep in mind that $L_l = 0.01 * L_m$. As is often the case, the equations from state plane notation may not result in closed form solution, so iterative solutions using e.g. Matlab are acceptable.

For the QSW flyback of Fig. 1(a), complete the following, assuming nominal operation with ZVS. For parts (e)-(h), you may neglect L_l (i.e. assume $L_l = 0$);

e) Sketch time-domain waveforms of the drain-to-source voltage v_{ds} of transistor Q, and the magnetizing inductor current i_m.
f) Sketch the j_m-m_{ds} state. Label all salient features.
g) Derive a complete set of equations in normalized state plane notation which model the behavior of the QSW flyback.
h) Solve for the value of L_m such that the switching frequency of the converter is 1 MHz at the specified operating point.

i) Again take $L_l = 0.01 * L_m$. Assume that the ringing resulting from the L_l-C_{ds} resonance dies out before the end of the subinterval in which it occurs. Solve for the power lost due to this damped ringing, and the peak voltage on v_{ds}. Does this satisfy the design constraint?

For both converters:

j) Compare the two designs. Consider, for each, the potential to achieve high efficiency and high power density. Solve for the current stresses in each component, and comment on the suitability of each topology for this application.