Course Info

- Course focuses on design an modeling of “high frequency” power electronics
  - Course website: http://web.eecs.utk.edu/~dcostine/ECE581
  - Goal of course is understanding of motivations and issues with high frequency power electronics; analysis and design techniques; applications
- Prerequisites: undergraduate Circuits sequence, Microelectronics, ECE 481 – Power Electronics, or equivalent

Contact Info

- **Instructor:** Daniel Costinett
  - Office: MK504
  - Office Hours: TBD
  - E-mail: Daniel.Costinett@utk.edu
  - Email questions will be answered within 24 hours (excluding weekends)
  - Please use **[ECE 581]** in the subject line

Course Structure

- Course meets MWF 10:20-11:10 am
- Plan to spend ~9 hours per week on course outside of lectures
- Grading:
  - Homework/Lab: 40%
    - One homework per week
    - Assignments due on Fridays unless otherwise noted on course website
    - Homework 1 posted, due Sept 1st
  - Midterm: 25%
    - Tentatively scheduled for October 28th
  - Final: 35%

Assignments

- Assignments due *at the start of lecture* on the day indicated on the course schedule
- All assignments submitted through canvas
  - https://utk.instructure.com/courses/104569
- No late work will be accepted except in cases of documented medical emergences
- Collaboration is encouraged on all assignments except exams; Turn in your own work
- All work to be turned in through canvas

Textbook and Materials

- The textbook

  R.Erickson, D.Maksimovic, *Fundamentals of Power Electronics*, Springer 2001

  will cover some of chapters 19-20 of 2nd Edition and reference materials from prior chapters. The textbook is available on-line from campus network. Purchase is not required for this course.
- MATLAB/Simulink, LTSpice will be used; All installed in on-campus labs, free, available through apps@UT, or on EECS servers
- Lecture slides and notes, additional course materials, homework, due dates , etc. posted on the course website
- Additional information on course website

Office Hours

- No formal scheduled office hours
- Stop by my office or e-mail me to schedule a time
- Will revisit later in the semester if my availability is sufficient for everyone

TINY BOX CHALLENGE

- Design competition to build and test an optimized dc-dc converter
  - Fall ‘16 – 60-to-12V, 60W
  - Fall ‘18 – 48-to-1.2V, 12W
  - Fall ‘20 – 48-to-12V, 36W
- Specs and details TBD
  - Usually ~October-November
  - Usually in groups of 2

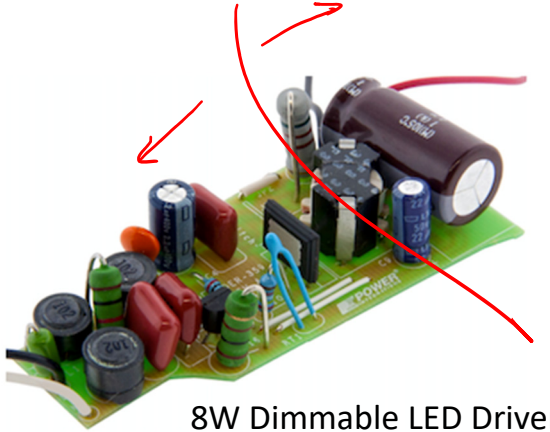
Course Topics

- High Frequency Power Conversion
  - Switching losses and device selection
  - Nonlinear device capacitances
  - Resonance in power electronics
  - Soft switching (ZVS and ZCS)
- Resonant Converters
  - State-plane analysis
  - Resonant converter topologies
  - Sinusoidal analysis
  - AC-modeling and frequency modulation
- Non-resonant soft switching converters
  - State-plane analysis
  - Constant frequency control
  - Resonant switches
  - Modeling and Simulation
  - Discrete time models
- Switched capacitor converters
  - SSL and FSL operation
  - Charge vector modeling
  - Soft-charging operation
- Applications and practical issues of high frequency converters

COURSE INTRODUCTION

Introduction

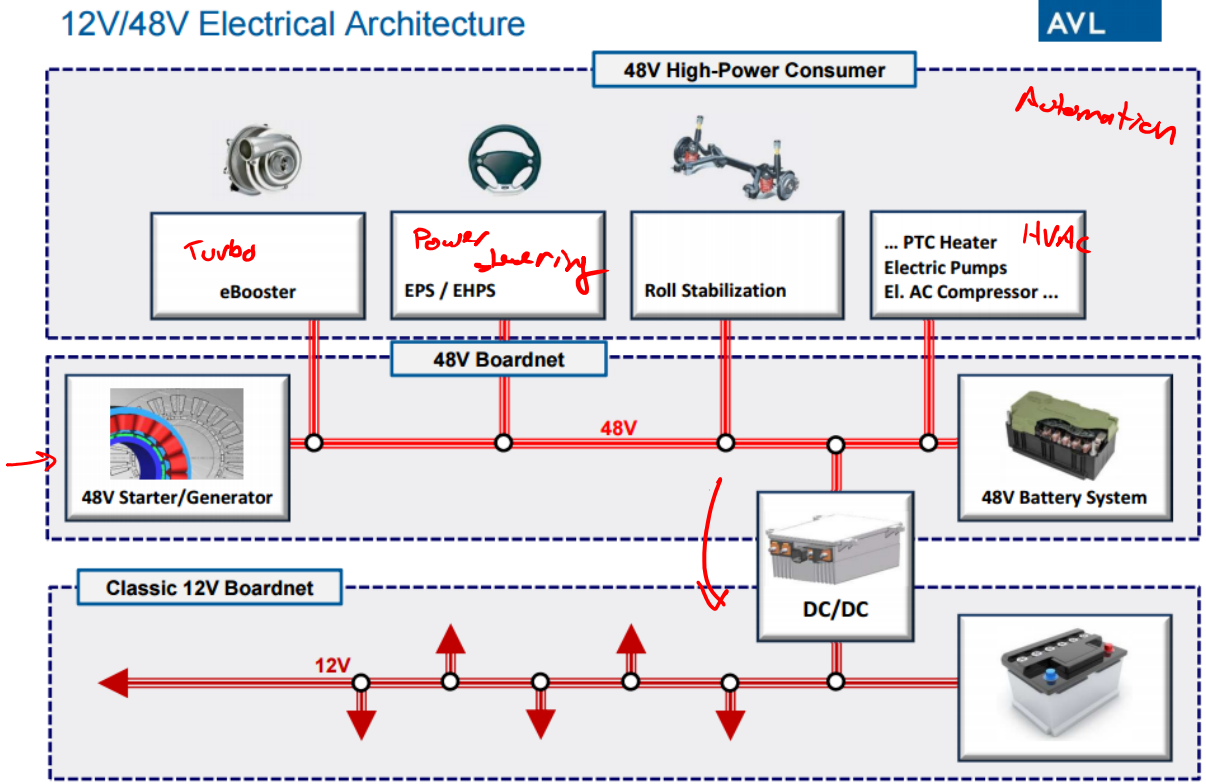
- Why high frequency?
  - Power Density
  - Control Bandwidth
  - Enabling Applications
- Techniques
  - Devices
  - Control
  - Topologies
  - Passives



8W Dimmable LED Driver

Voltage Regulation Module

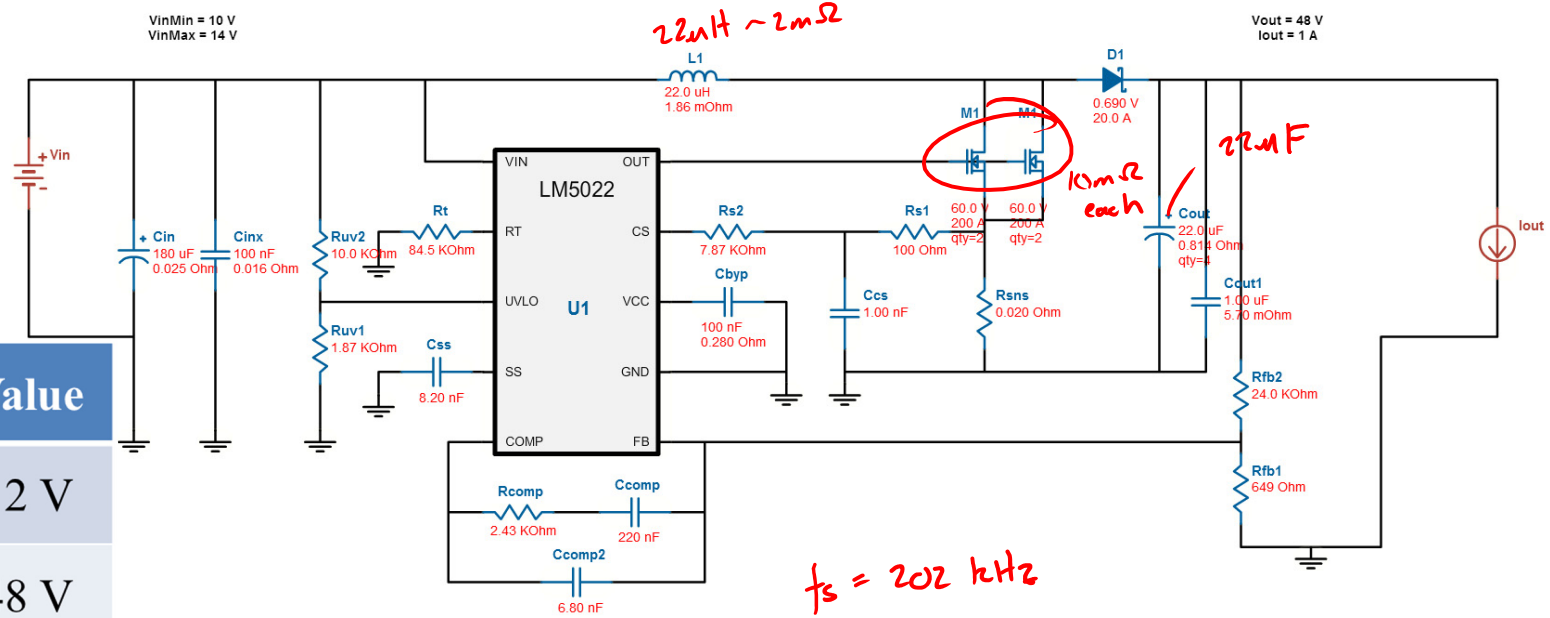
Motivating Example



NXP Semi, "Semiconductors – enablers of future mobility concepts", 2011
Audi, "Electric biturbo and hybridization", 2014
AVL, "48V Mild Hybrid Systems"

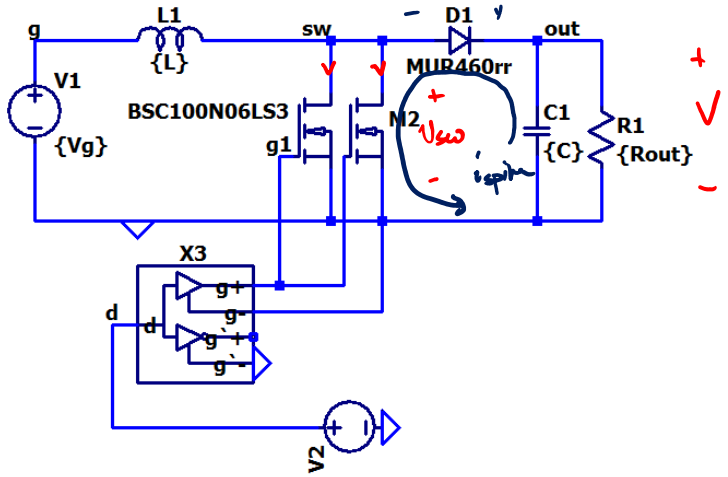
Baseline Design

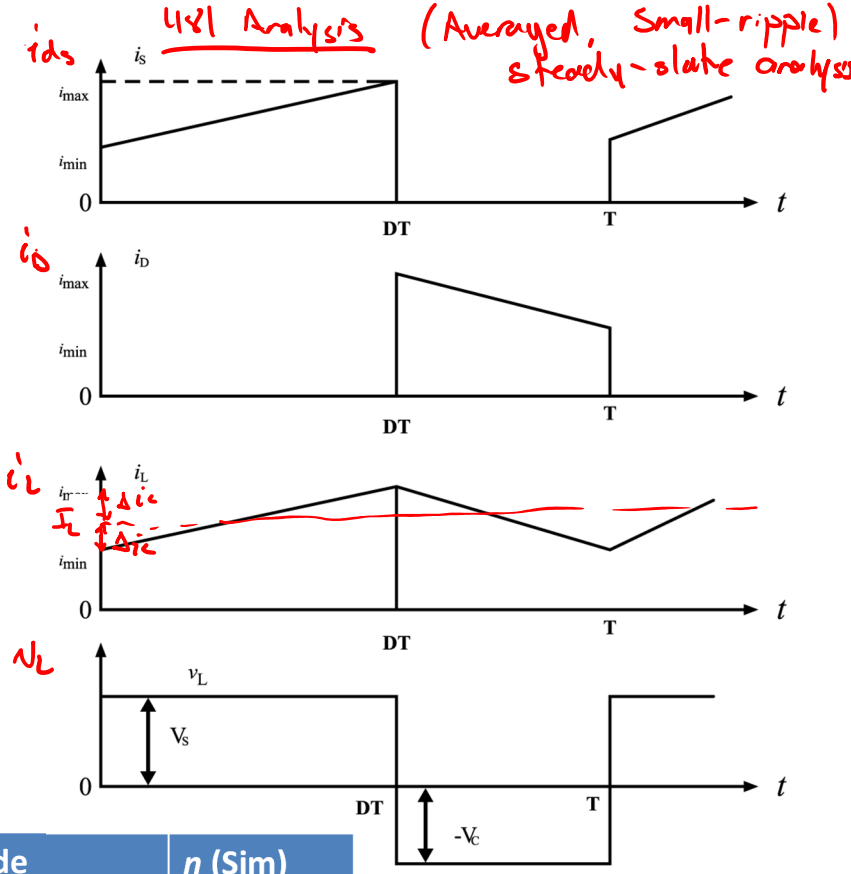
- Use TI WebBench (webench.ti.com) to get a baseline design



Param	Value
V_g	12 V
V_{out}	48 V
R_{out}	48 Ω
ΔV_{out}	0.1 V

LTSpice Simulation





$\langle v_L \rangle = D(V_g) + D'(V_g - V) = V_g - D'V = 0$

$D' = \frac{V_g}{V}$ $\quad D = 1 - \frac{V_g}{V}$

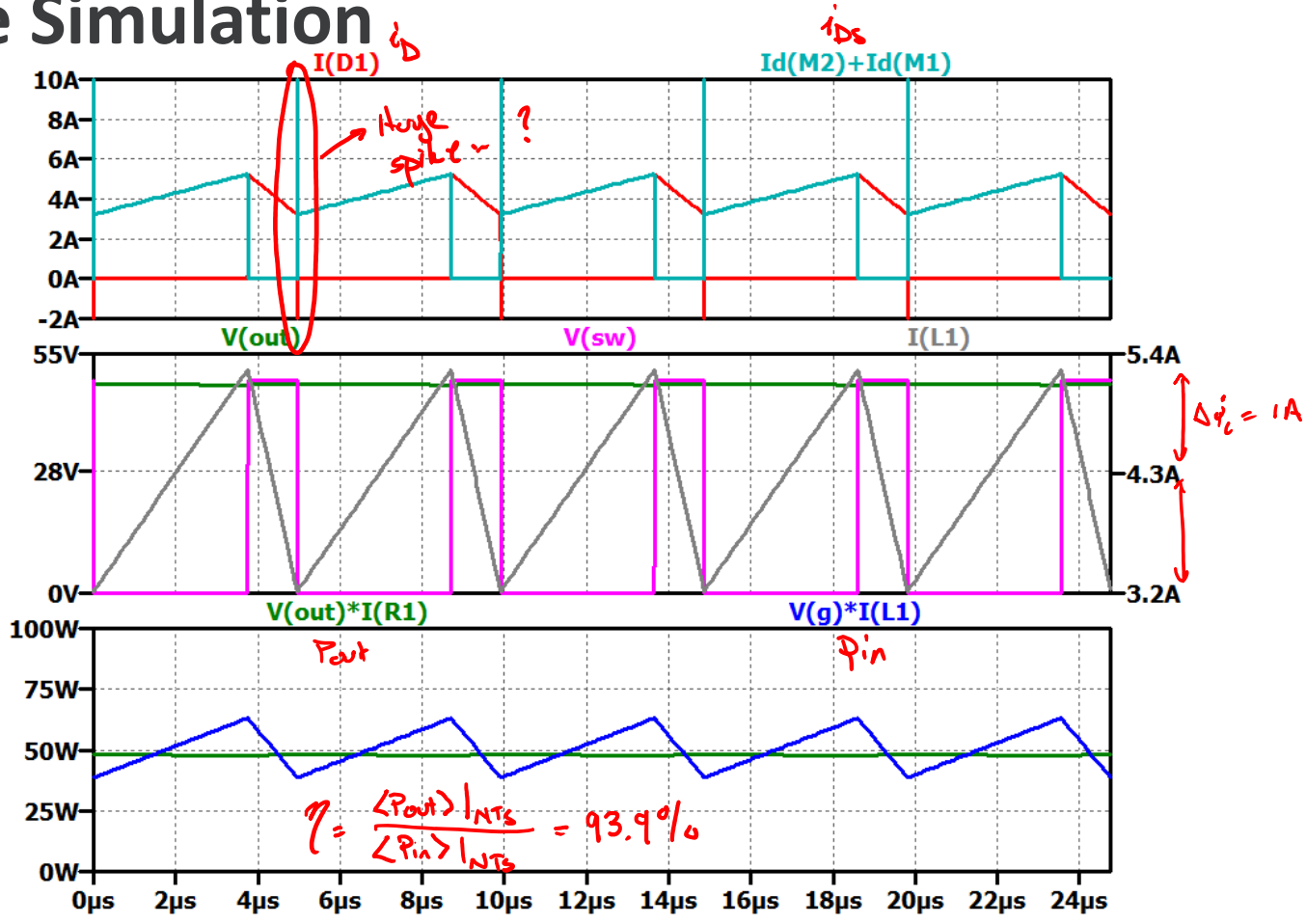
$P_{out} = \frac{V^2}{R} = 48W$

$I_L = \frac{P_{out}}{V_g} = 4A$

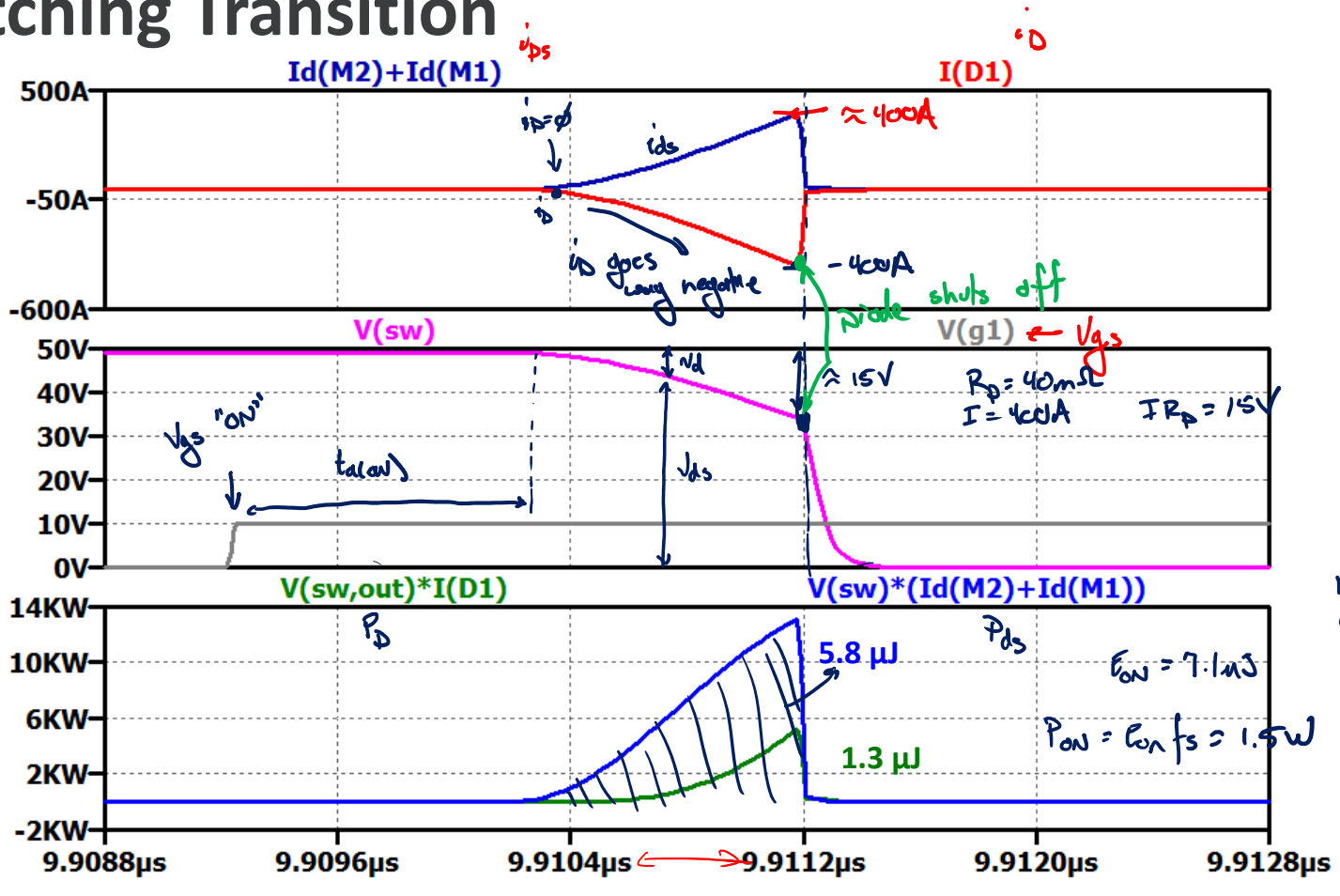
$\Delta i_L = \frac{1}{2}\frac{V_g}{L}\Delta T_s = 1A$

L	C_{out}	f_s	Diode	η (Sim)
22uH	22uF	202k	Si (FR)	93.9%

LTSpice Simulation



Switching Transition



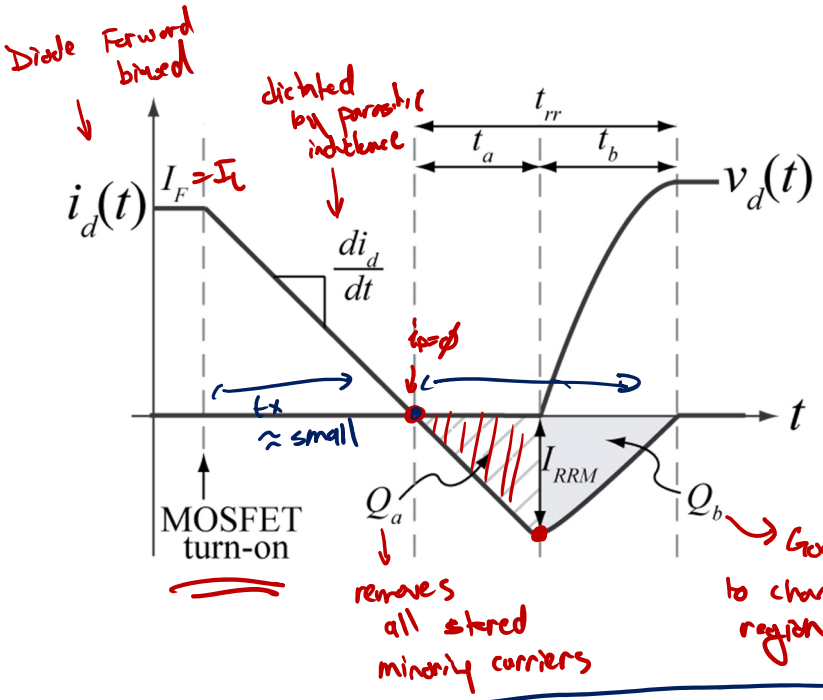
$\frac{1.5W}{48W} = 3\%$

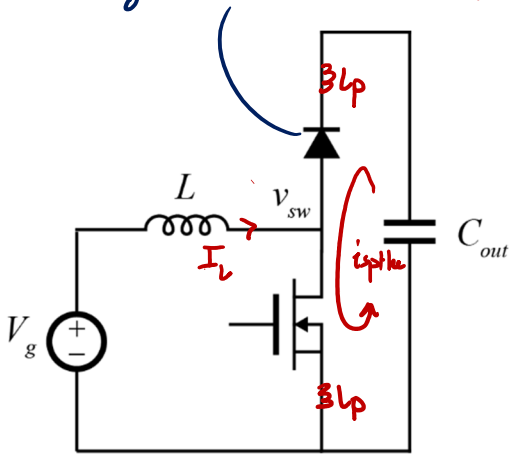
or

half of total losses in the converter

Diode Reverse Recovery

Minority carrier device
"conductivity modulation"
→ Need to be removed before diode can reverse biased





$Q_{rr} = Q_a + Q_b$

$$P_{rr} = E_{rr} f_s \approx \left[Q_{rr} V + I_L V t_{rr} \right] f_s$$

Datasheet RR Characteristics

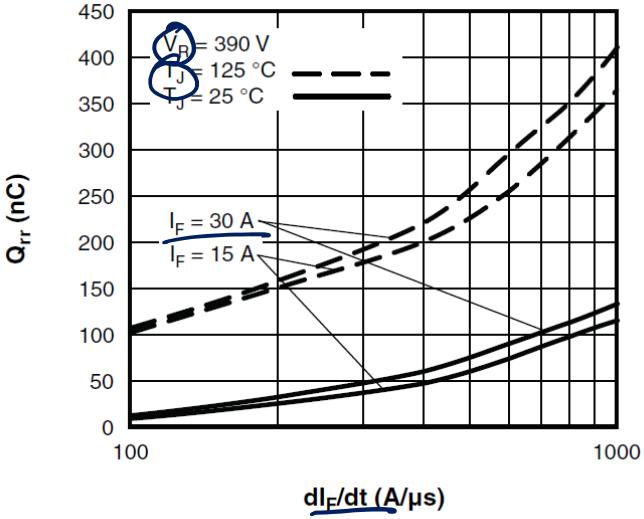


Fig. 10 - Typical Stored Charge vs. dI_F/dt

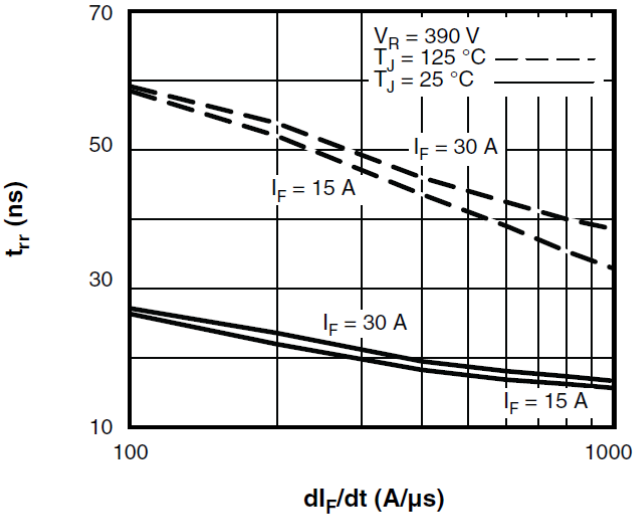
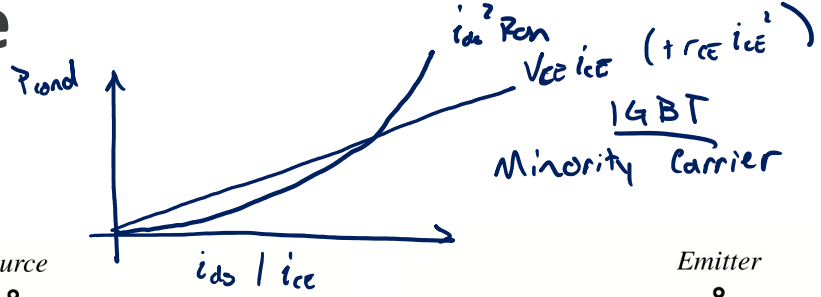
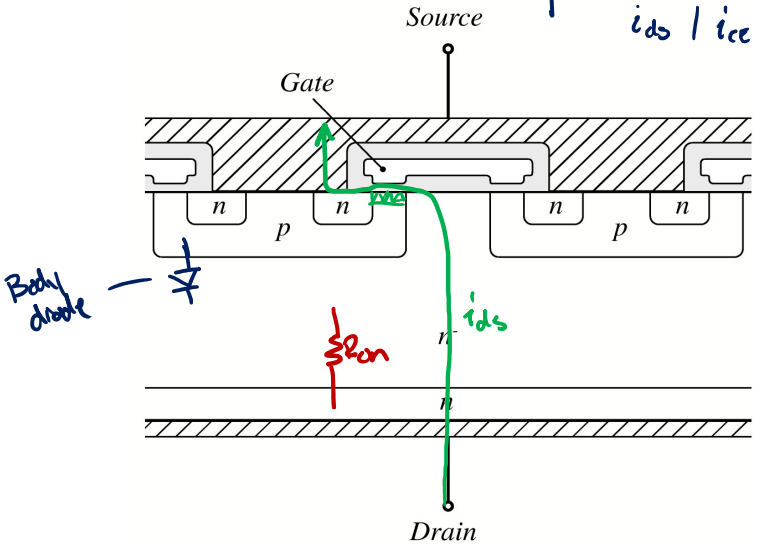


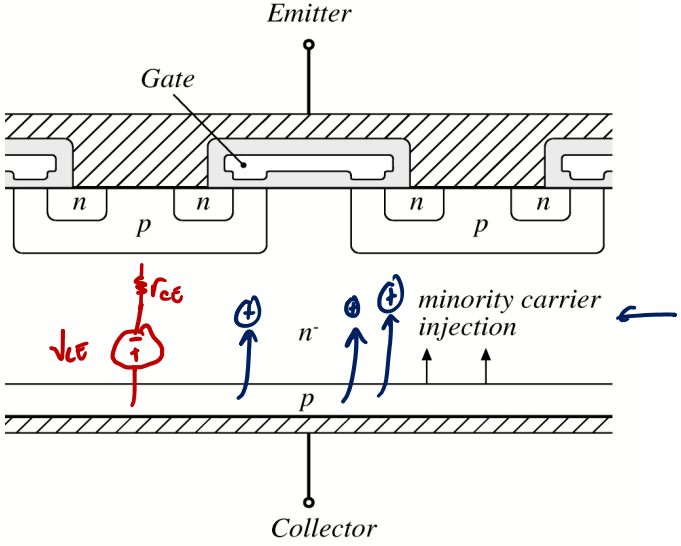
Fig. 9 - Typical Reverse Recovery Time vs. dI_F/dt

$$Q_{rr} \text{ \& } t_{rr} = f\left(V_R, T, \frac{di_F}{dt}, I_F\right)$$

Charge Storage







+ Conductivity Modulation