Course Schedule

Course Planning

Oct. 9 Fall Break	L19 - Oct. 11 The SRC converter	L20 - Oct. 13 Today SRC converter examples and MATLAB comparison Homework 7 Due
L21 - Oct. 16	L22 - Oct. 18	L23 - Oct. 20 Homework 8 Due
L24 - Oct. 23 Midterm Exam Begins	L25 - Oct. 25	L26 - Oct. 27 Midterm Exam Due
Oct. 30 ECCE (no class)	Nov. 1 ECCE (no class)	L27 - Nov. 3

Midterm Exam

- 5-day take-home exam
  - Week of Oct 23-27th
  - Absolutely no collaboration
  - No materials other than notes and course website

- Covers material to date, HWs 1-8
  - Switching Loss
  - Nonlinear C_{oss}
  - State Plane Analysis

TiNY BOX CHALLENGE

Competition Specifications

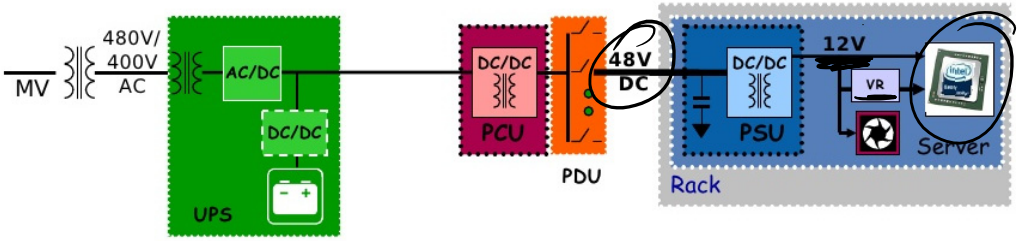
The **winning converter** will be the unit which achieves the **highest power density**, i.e. fits in the smallest rectangular volume, while meeting the following specifications.

Parameter	Requirement	Comment
Voltage Input	48 Vdc	
Maximum Output Power	12 W	
Output Voltage	1.2 ± 0.1 Vdc	
Output Ripple Voltage	< 2%	Measured as $V_{pk\text{-}pk}/V_{avg}$ from the DC supply, in steady state, at full output power
TPE Efficiency	> 85%	Measured using TPE method[1]
No-load Power Loss	< 3W	Measured with load disconnected, but output voltage within specified range
Volume	< 2 in^3	Volume of minimum rectangle enclosing power stage

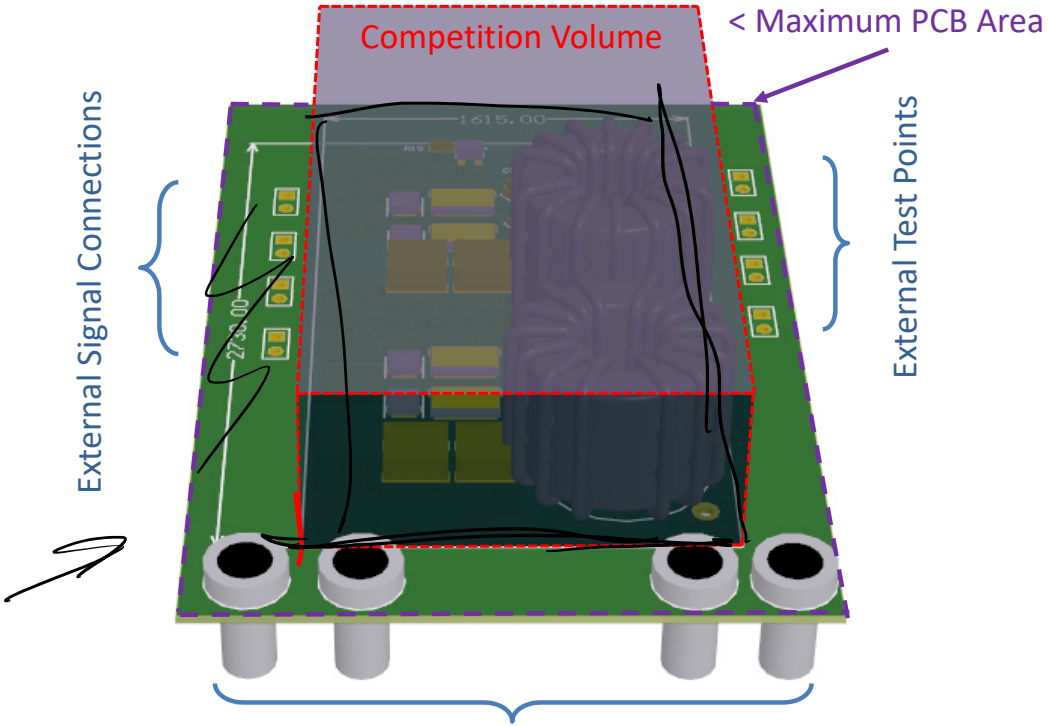
[1]Tennessee Power Electronics (TPE) efficiency is a weighted power efficiency defined as:

$$\eta_{TPEF} = 0.1\eta_{P_{out}=0.25\cdot P_{max}} + 0.15\eta_{P_{out}=0.5\cdot P_{max}} + 0.25\eta_{P_{out}=0.75\cdot P_{max}} + 0.5\eta_{P_{out}=P_{max}}$$

Example Application



How Volume is Measured



Additional Details

- Full competition specifications and example testing report on course webpage
- No regulation requirements
- Deliverables:
  - Written design comparison of 3 topologies (11/10)
  - PCB Layout of single design (11/17)
  - Testing Report of prototype (12/6)

Design and Comparison Report (11/10)

1. Select three topologies from the table and compare based on
   - I. Efficiency at full power
   - II. Power loss at zero load
   - III. Output voltage ripple
   - IV. Volume of main passive components

	Class I	Class II	Class III	Class IV
Definition	Two-switch PWM topologies*	Isolated variants of PWM topologies	AC-link topologies	Any topology not conforming to Class I-III
Examples	Buck, Boost, Buck-Boost, Cuk, SEPIC, etc.	Flyback, Forward, push-pull, half-bridge, full-bridge	DAB, DAHB, SRC, LLC, Full Bridge, etc.	Switched capacitor, sigma-delta, multilevel, etc.
Required number	**0**	**≤1***	**--**	**1**

* Fully small-ripple, hard-switched Class-II topologies may not be used.

2. Select (and justify) one topology, and provide a complete design including (but not limited to)
   - I. Power Devices
   - II. Gate Driver Circuitry
   - III. Passive Devices and implementation
   - IV. Switching Frequency

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L28 - Nov. 6	L29 - Nov. 8	L30 - Nov. 10 Design Comparison Report
L31 - Nov. 13	L32 - Nov. 15	L33 - Nov. 17 PCB Layout Due
L34 - Nov. 20	Nov. 22 No Class Day	Nov. 24 Thanksgiving Break
L35 - Nov. 27	L36 - Nov. 29	L37 - Dec. 1
L38 - Dec. 4	L39 - Dec. 6 Testing Report Due	Dec. 8 Final Exam Period Final Exam