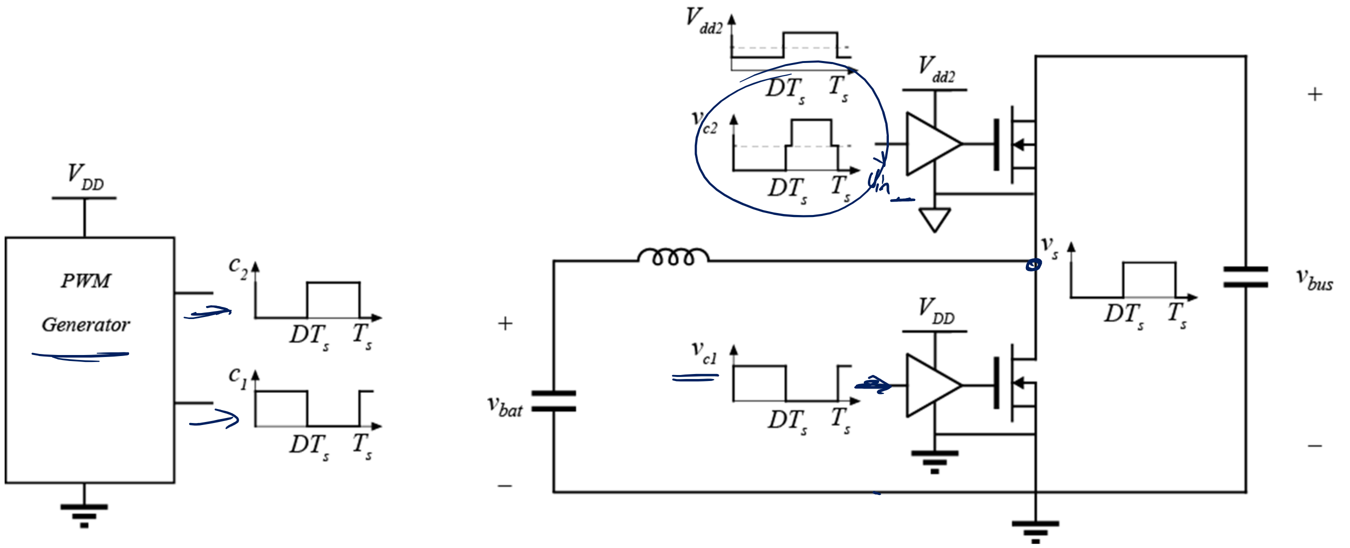
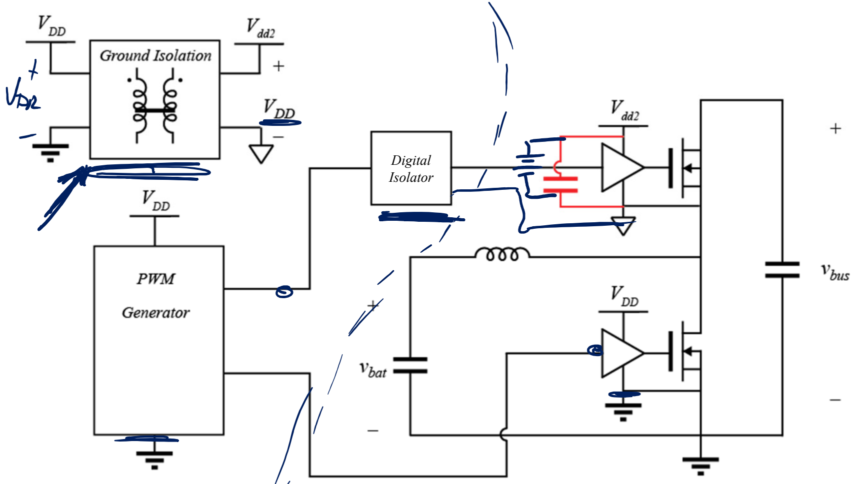
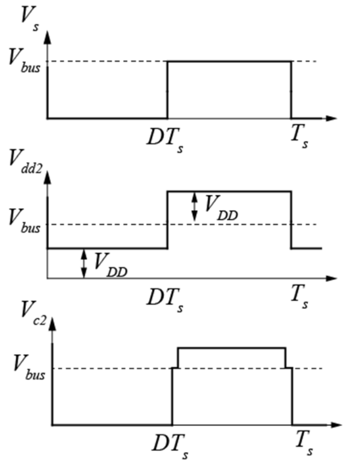
High Side Signal Ground



- Gate driver chip must implement v_{gs} waveforms
- Issue: source of Q_2 is not grounded

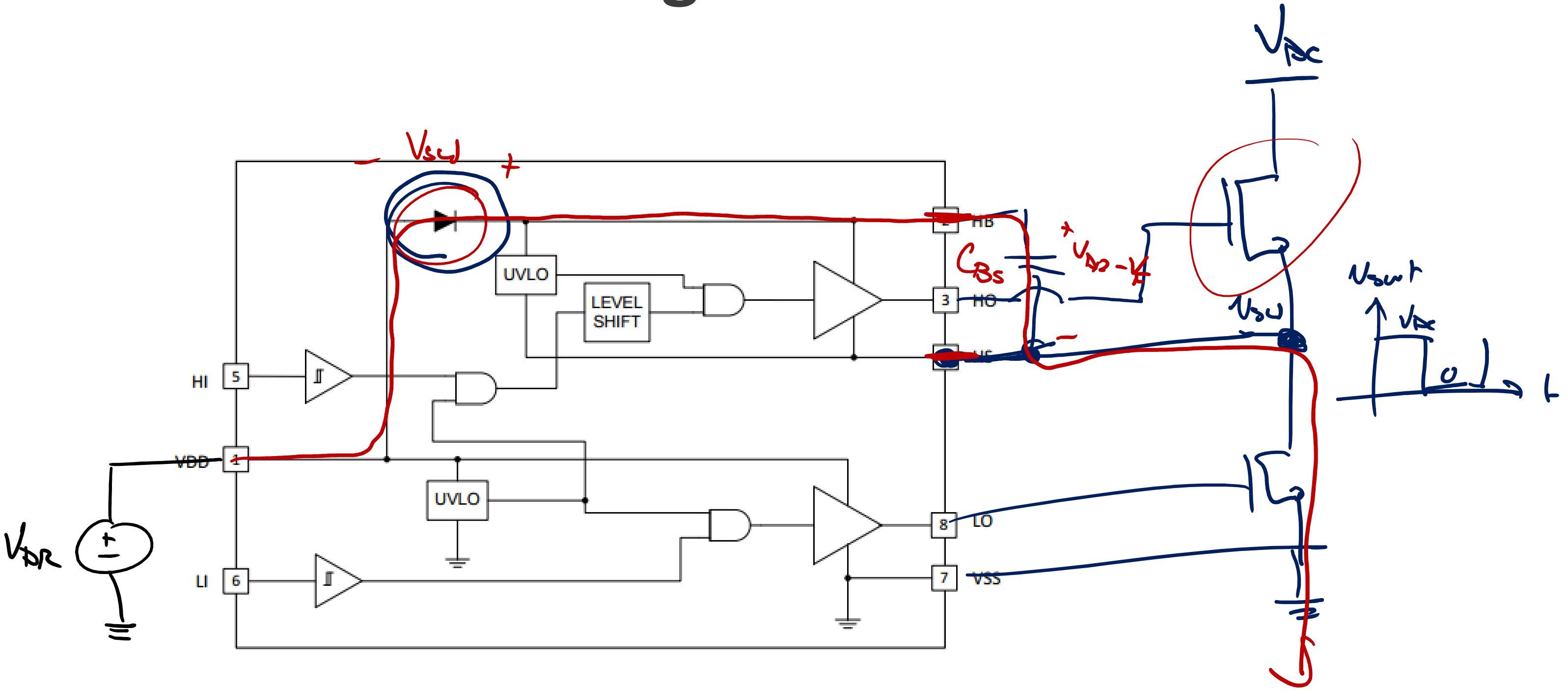
Generating Floating Supply



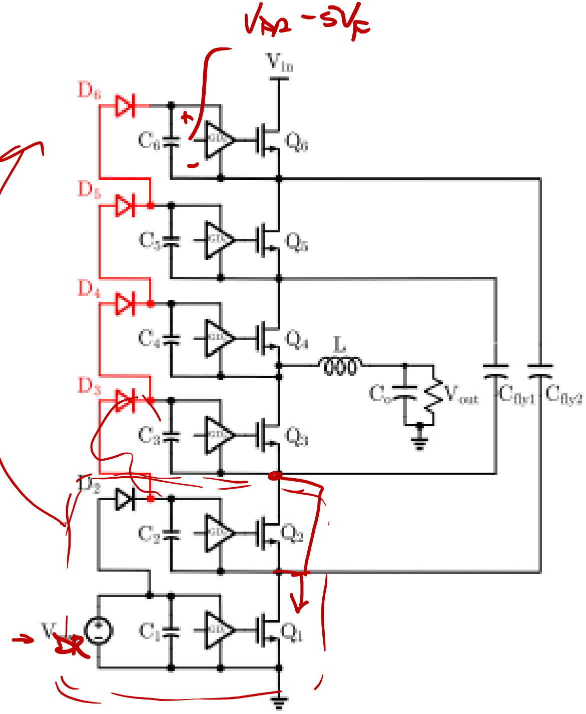


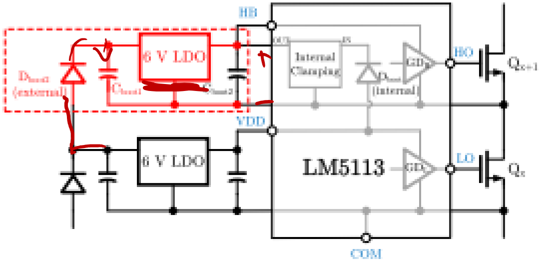
- Isolated supplies sometimes used; Isolated DC-DC, batteries
- Bootstrap concept: capacitor can be charged when V_s is low, then switched

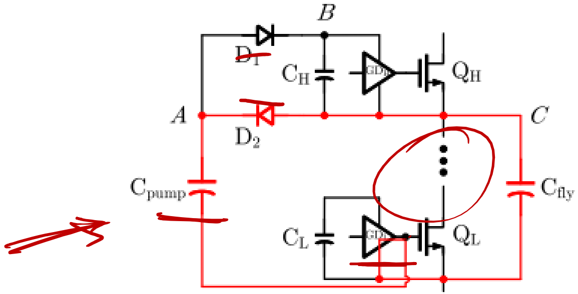
UCC27211a Internal Diagram



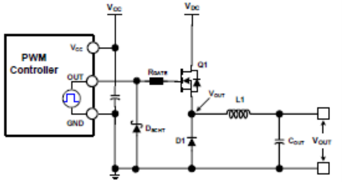
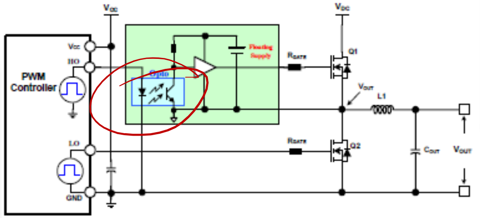
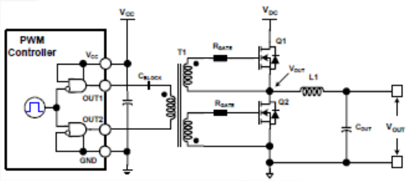
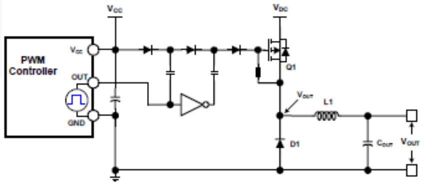
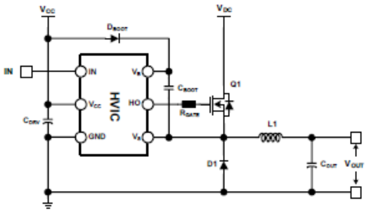
Cascaded Bootstrapping







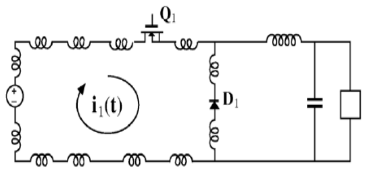
Z. Ye, Y. Lei, W. -C. Liu, P. S. Shenoy and R. . Pilawa-Podgurski, "Improved Bootstrap Methods for Powering Floating Gate Drivers of Flying Capacitor Multilevel Converters and Hybrid Switched-Capacitor Converters," in *IEEE Transactions on Power Electronics*, June 2020, doi: 10.1109/TPEL.2019.2951116.

Direct Drive		Easiest high-side application the MOSFEF and can be driven directly by the PWM controller or by a ground referenced driver, but it must meet two conditions, as follows: $V_{CC} < V_{GS,MAX}$ *and* $V_{DC} < V_{CC} - V_{GS,Miller}$
Floating Supply Gate Drive		Cost impact of isolated supply is significant. Opto-coupler tends to be relatively expensive, limited in bandwidth, and noise sensitive.
Transformer Coupled Drive		Gives full gate control for an indefinite period of time, but is somewhat limited in switching performance. This can be improved with added complexity.
Charge Pump Drive		The turn-on times tend to be long for switching applications. Inefficiencies in the voltage multiplication circuit may require more than low stages of pumping.
Bootstrap Drive		Simple and inexpensive with limitations; such as, the duty cycle and on-time are both constrained by the need to refresh the bootstrap capacitor. Requires level shift, with the associated difficulties.

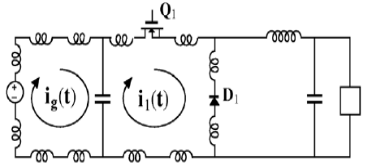
Fairchild Semi App Note AN-6076

Half Bridge Loop Inductance

Parasitic inductances of input loop explicitly shown:

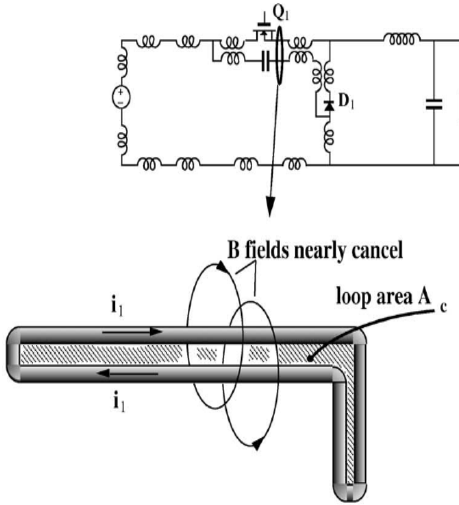


Addition of bypass capacitor confines the pulsating current to a smaller loop:

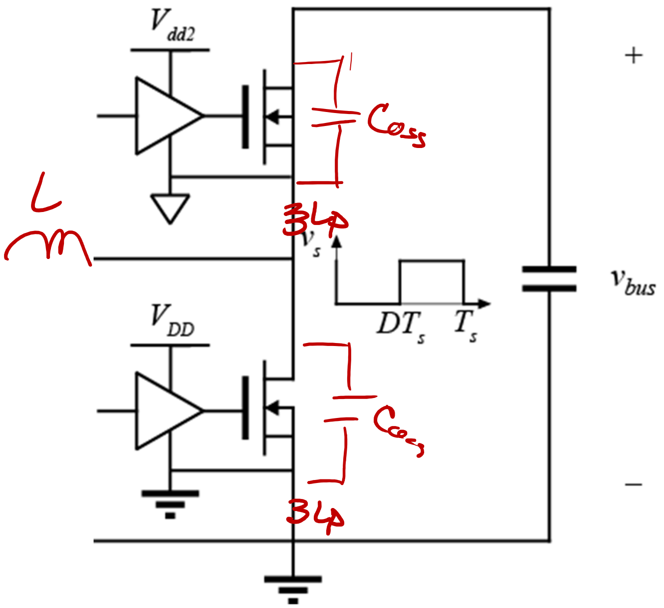


high frequency currents are shunted through capacitor instead of input source

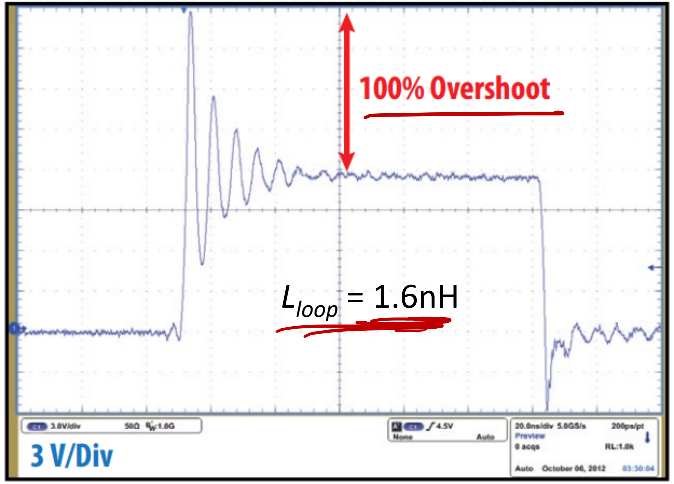
Even better: minimize area of the high frequency loop, thereby minimizing its inductance

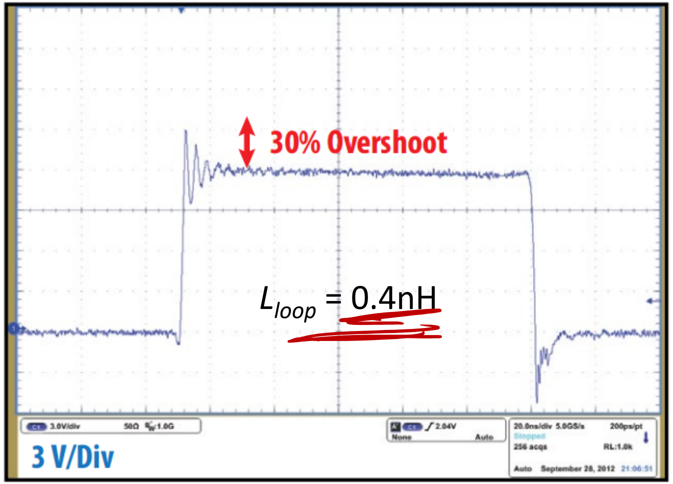


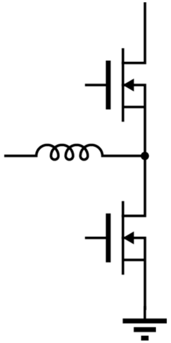
Bridge Layout

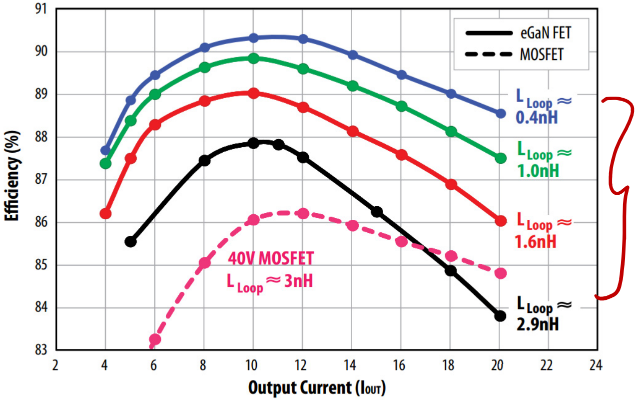


Effect of Loop Inductance



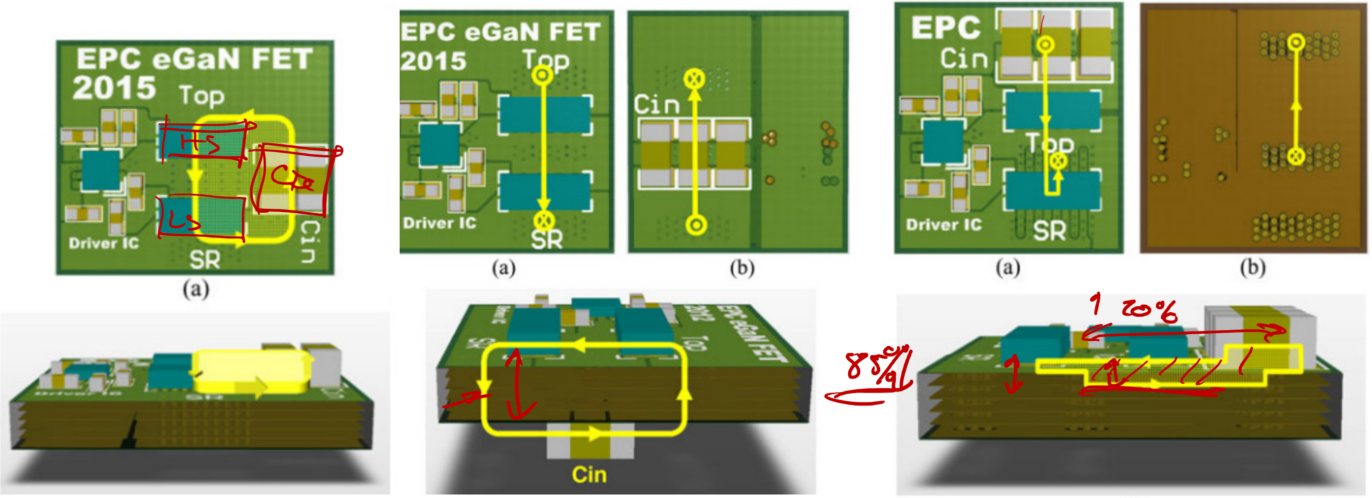






D Reusch, “Optimizing PCB Layout”

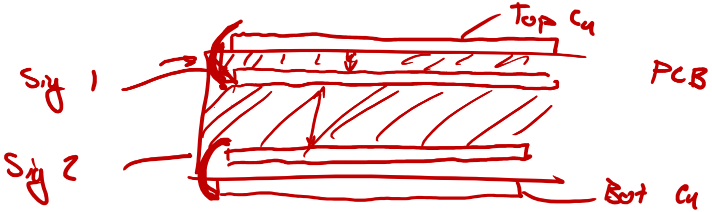
Half Bridge Layout: Another Example



Lateral

Vertical

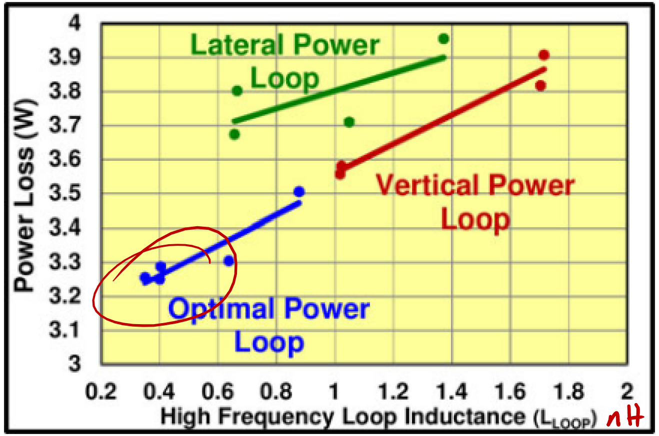
“Optimal”

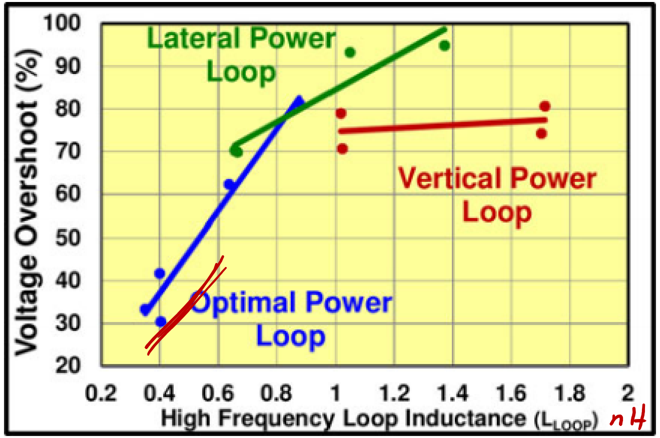


D. Reusch & J Strydom, “Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter”

THE UNIVERSITY OF TENNESSEE KNOXVILLE

Layout Impact Measurements



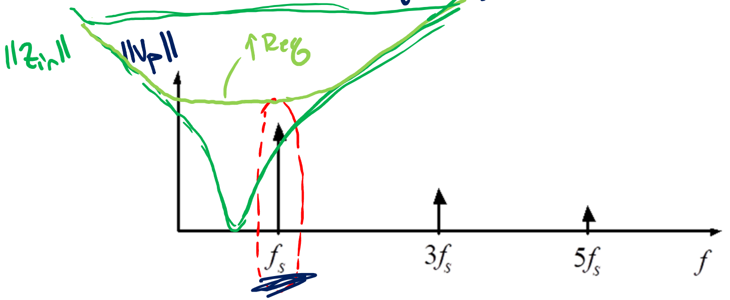


- Smallest Loop Area results in
  - Smaller overvoltage
  - Lower switching loss

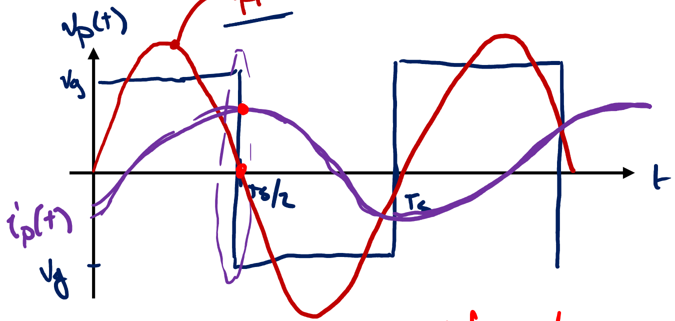
Sinusoidal Analysis (Ch 19)

(Fundamental Harmonic Analysis)

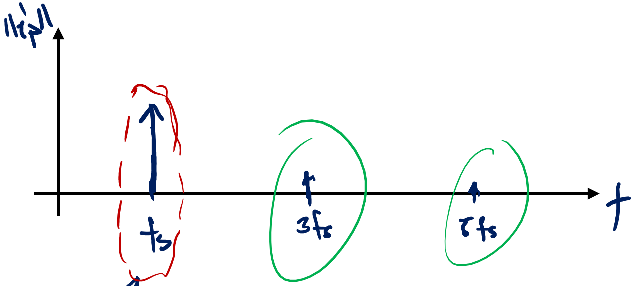
Fundamentals of Pwr Elec (2nd) Ch 22 in 3rd Ed.



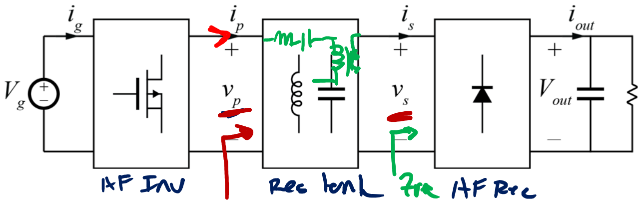
$v_{p1}(t)$ – component of v_p @ f_s



will lose exact ZVS information
- can check current polarity for possible ZVS



even more fundamental dominated due to ~bandpass characteristics of the tank



e.g. for SRC $Z_{in} = sL_r + \frac{1}{sC} + \left(\frac{Z_{rec}}{n^2} \approx R_{eq}\right)$

Sinusoidal Analysis: Comments

- Generally most accurate when operating near resonance with a high Q
- Effective quality factor Q_e depends not only on resonant tank, but also on loading
- Analysis neglects switching intervals; can only predict where ZVS **cannot** be obtained

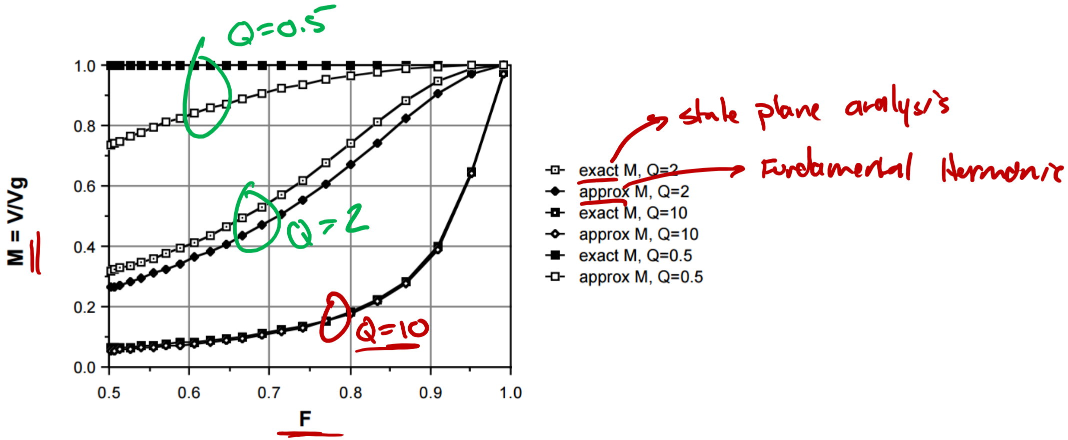
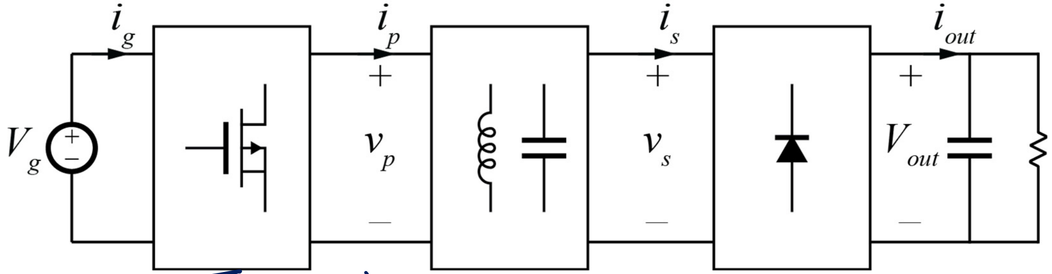


Fig. 2.14. Comparison of exact and approximate series resonant converter characteristics, below resonance.

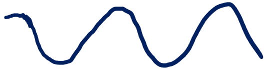
AC Link Waveforms



DC Average — AC waveforms, fundamental Harmonic — DC Average

$v_p(t) \rightarrow$ full/actual signal

$v_{p1}(t) \rightarrow$ fundamental Harmonic



$V_{p1} \cos(\omega_s t + \varphi_{vp})$