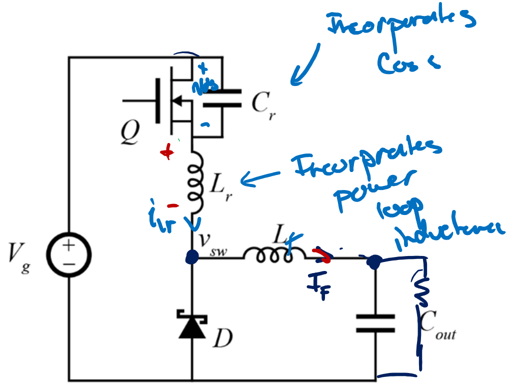
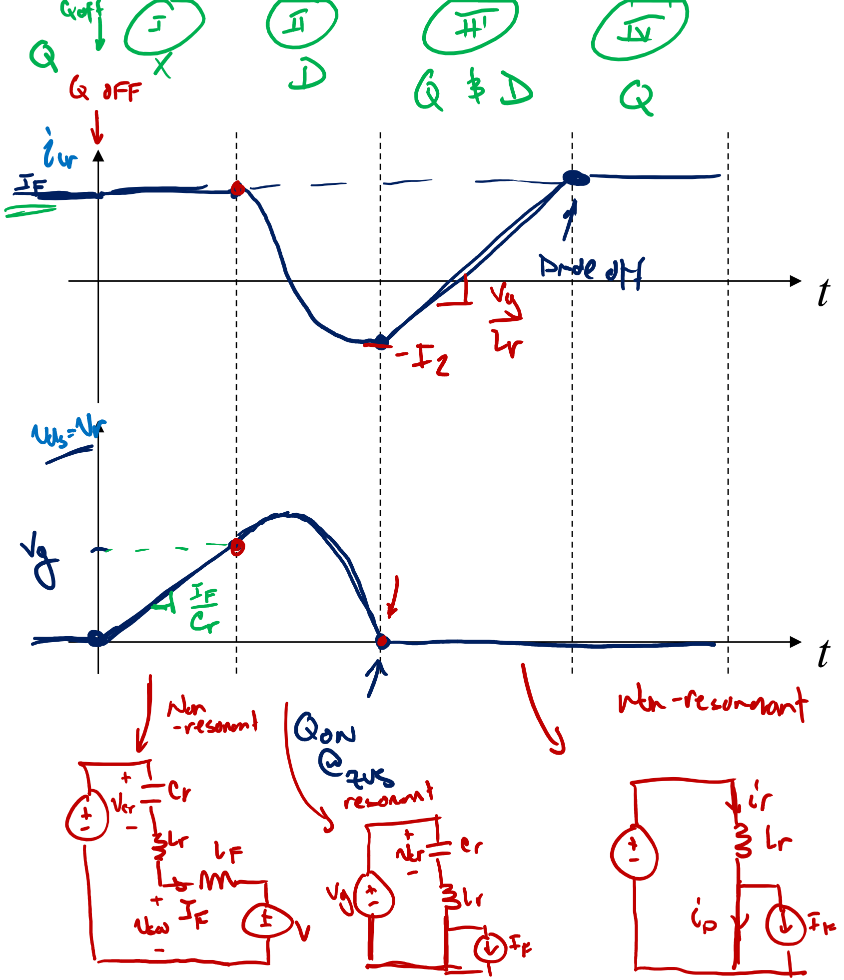
ZVS-QR Buck





Characteristics :

+ C_{oss} & $L_{power\ loop}$ are incorporated into operation
+ Peak inductor current is the peak FET current
- C_D is not part of operation
- Peak FET stresses > V_g

ZVS-QR State Plane

$V_{base} = V_g \qquad R_0 = \sqrt{\frac{L_r}{C_r}} \qquad I_{base} = \frac{V_{base}}{R_0}$

I

$$\frac{I_F}{C_r} t_1 = V_g$$

$$\boxed{\theta_1 = \frac{1}{J_F}}$$

II

$$\boxed{J_F^2 = 1 + J_2^2}$$

$$\boxed{\beta = \pi + \sin^{-1}\left(\frac{1}{J_F}\right)}$$

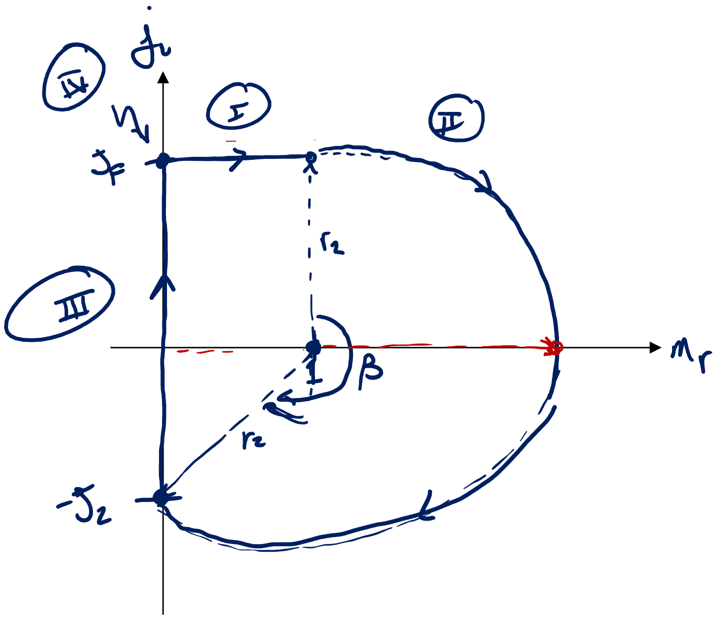
III

$$\frac{V_g}{L_r} t_3 = (I_F + I_2)$$

$$\boxed{\theta_3 = J_F + J_2}$$

IV

$$\boxed{\theta_1 + \beta + \theta_3 + \theta_4 = \frac{2\pi}{F}}$$



ZVS condition: $r_2 \geq 1$

$$\boxed{J_F \geq 1}$$

Averaging

Cap-Q balance on C_{out}

$$\langle i_{Cout}\rangle\big|_{T_s} = 0 \rightarrow I_2 = \frac{V}{R}$$

Volt-sec balance on L_F

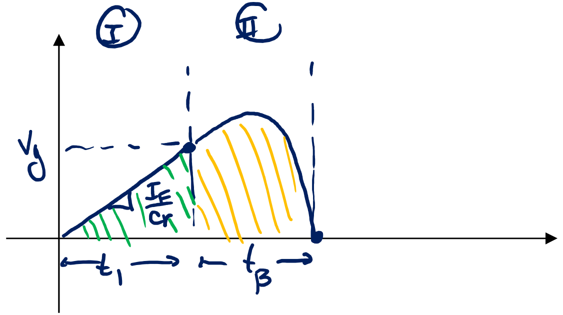
$$\langle v_{LF}\rangle\big|_{T_s} = 0 = V_g - \langle v_{Cr}\rangle\big|_{T_s} - \cancel{\langle v_{Lr}\rangle\big|_{T_s}}^{\,0} - V$$

$$V = V_g - \frac{1}{T_s}\int_0^{T_s} v_{Cr}\,dt$$

$$V = V_g - \frac{1}{T_s}\left[\lambda_1 + \lambda_2\right]$$

$$V = V_g - \frac{1}{T_s}\left[\frac{1}{2}t_1 V_g + V_g t_\beta + L_r(I_F + I_2)\right]$$

$$\boxed{M = 1 - \frac{F}{2\pi}\left[\frac{1}{2}\theta_1 + \beta + J_F + J_2\right]}$$



$$\lambda_1 = \frac{1}{2}t_1 V_g$$

$$\lambda_2 = \int_{II} v_{Cr}\,dt = \int_{II}\left(V_g - L_r\frac{di_{Lr}}{dt}\right)dt$$

$$= V_g t_\beta - L_r(-I_F - I_2)$$

$$= V_g t_\beta + L_r(I_F + I_2)$$

Complete Solution

$$M = 1 - \frac{F}{2\pi}\left[\frac{\theta_1}{2} + \beta + J_2 + J_F\right]$$

$$\boxed{M = 1 - \frac{F}{2\pi}\left[\frac{1}{2J_F} + \pi + \sin^{-1}\left(\frac{1}{J_F}\right) + \sqrt{J_p^2 - 1} + J_F\right]}$$

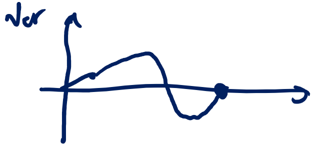
→ same as 20.46 in 2nd Ed Fundamentals of Pwr Elec
" 23.46 in 3rd Ed

$1 - FP_{1/2}(J_L) = M$ of ZCS-QR Buck

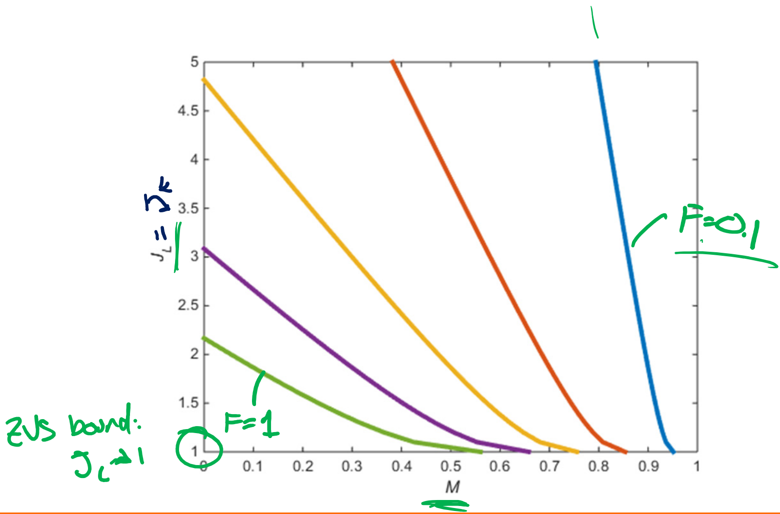
$$M = 1 - F\,\underline{\underline{P_{1/2}}}\left(\frac{1}{J_L}\right) \longrightarrow \frac{1}{J_L} \leftrightarrow J_L$$

This is half-wave ZVS-QR Buck

Full-wave ZVS-QR Buck



→ Requires bidirectional voltage blocking Q



MOSFET Voltage Stresses

Peak voltage on Q:

$$M_{pk} = 1 + J_F$$

$$V_{pk} = V_g + \underline{\underline{J_F V_{base}}}$$

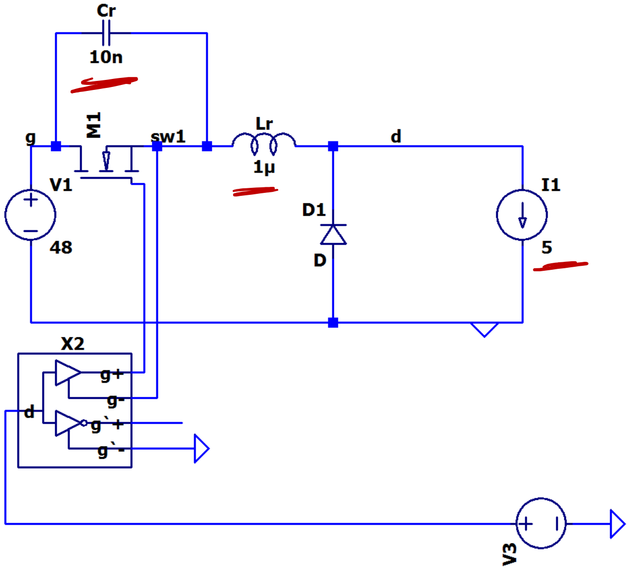
@ Minimum ZVS power $J_F = 1$

$$\boxed{V_{pk} = 2V_g}$$ @ minimum ZVS power

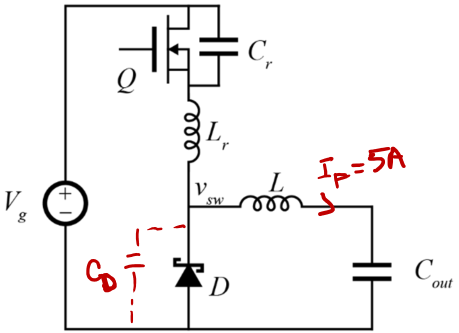
ex/ If we want to keep ZVS from full power down to 20% of P_{max}

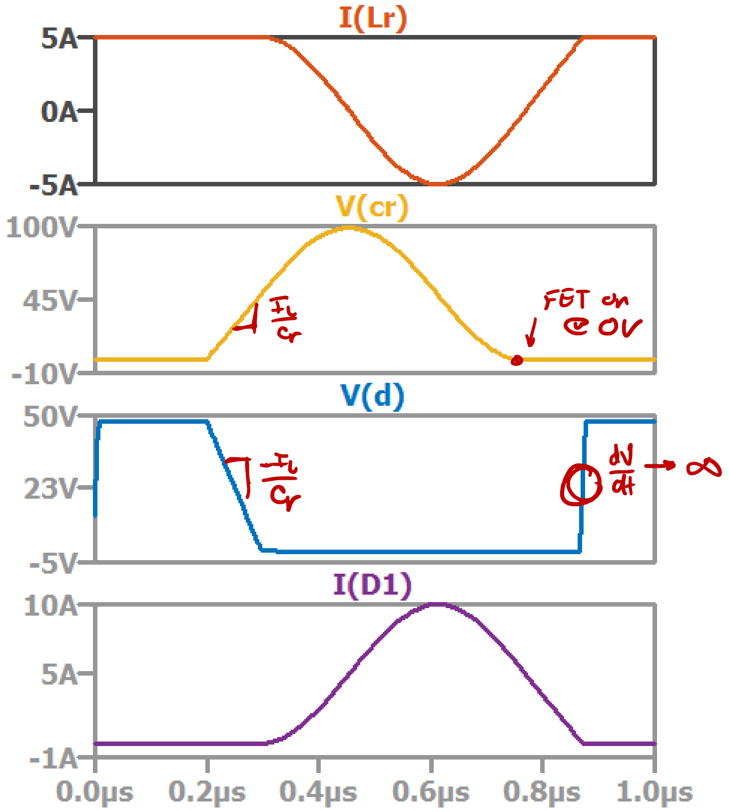
$$V_{pk} = (5+1)V_g = \underline{\underline{6V_g}}$$

Test Circuit

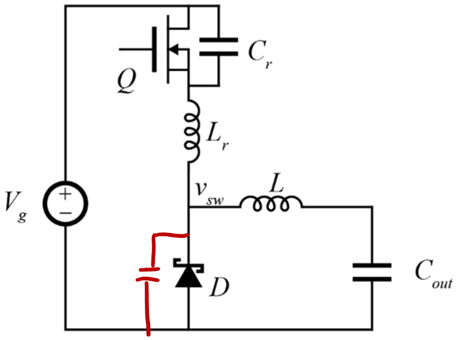


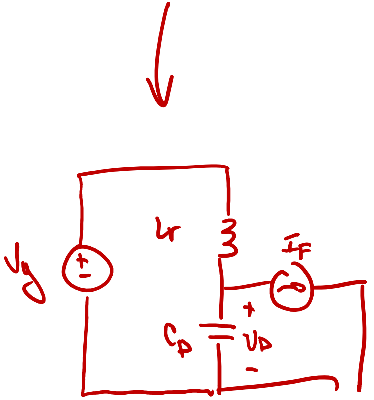
Simulation Results



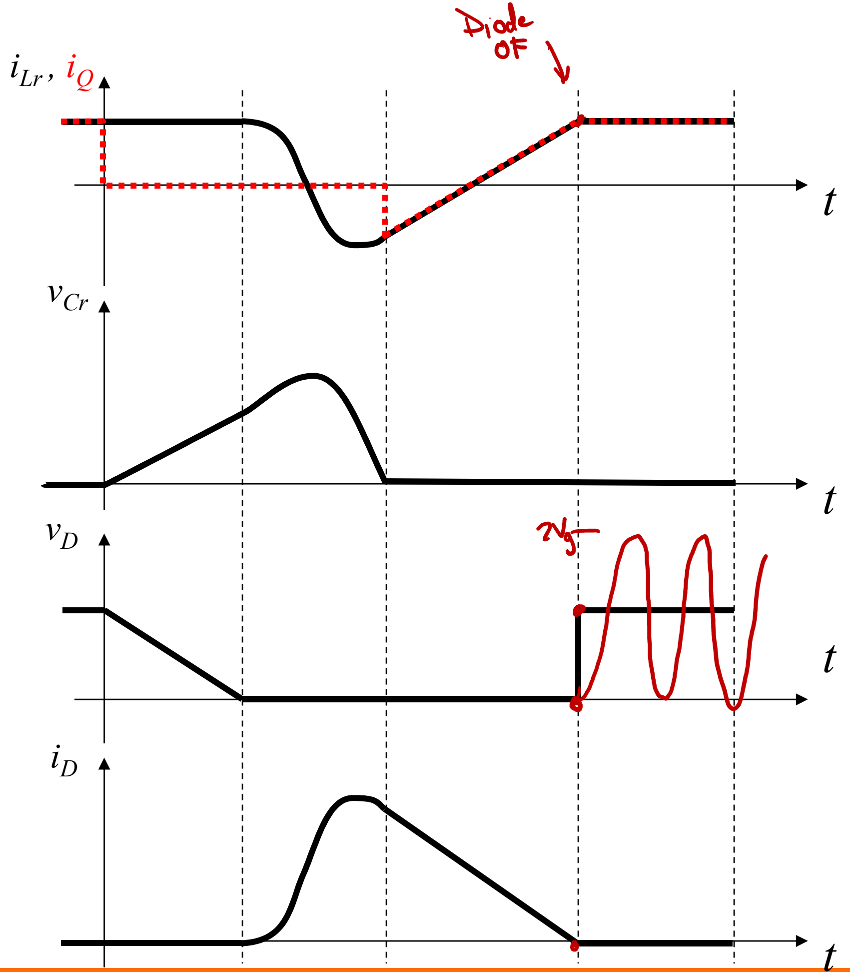


Diode Capacitance





IC: $\begin{cases} V_D = \phi \\ I_{Lr} = I_F \end{cases}$ DC: $\begin{cases} I_{Lr} = I_F \\ V_D = V_g \end{cases}$



Simulation Results: Diode Capacitance