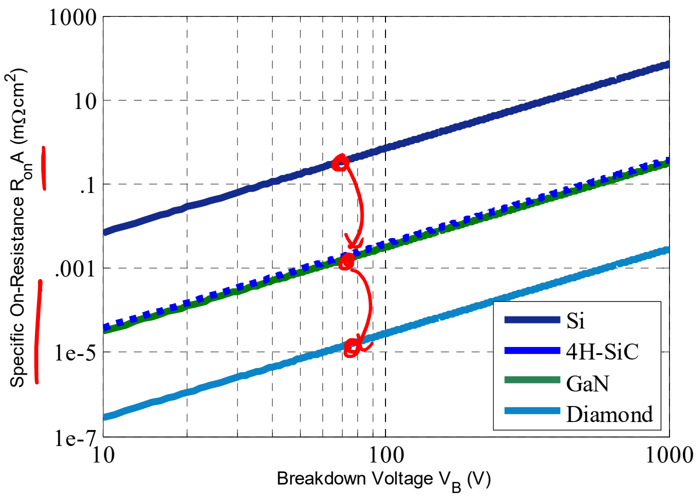
WBG Materials

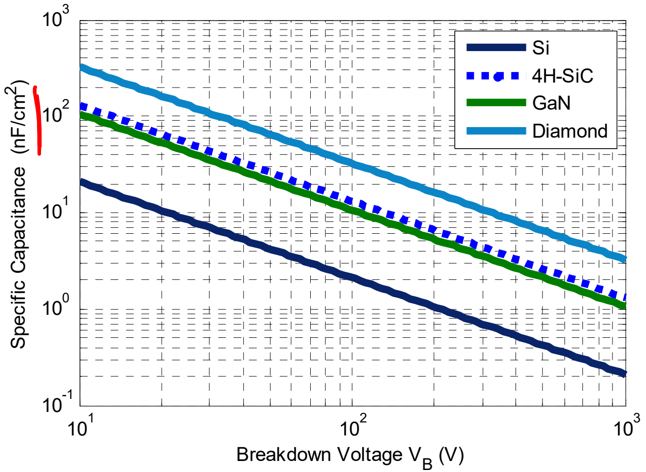
Table 2.1. Physical characteristics of Si and the major WBG semiconductors

Property	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap, E_g (eV)	1.12	1.43	3.03	3.26	3.45	5.45
Dielectric constant, ε_r [a]	11.9	13.1	9.66	10.1	9	5.5
Electric breakdown field, E_c (kV/cm)	300	400	2,500	2,200	2,000	10,000
Electron mobility, μ_n (cm^2/V·s)	1,500	8,500	500 80	1,000	1,250	2,200
Hole mobility, μ_p (cm^2/V·s)	600	400	101	115	850	850
Thermal conductivity, λ (W/cm·K)	1.5	0.46	4.9	4.9	1.3	22
Saturated electron drift velocity, v_{sat} ($\times 10^7$ cm/s)	1	1	2	2	2.2	2.7

[a] $\varepsilon = \varepsilon_r \cdot \varepsilon_o$ where $\varepsilon_o = 8.85\times10^{-14}$ F/cm.

B Ozpineci, L M Tolbert, "Comparison of Wide-Bandgap Semiconductors for Power Electronics Applications"





Supplemental Materials

Online Course Delivery

Additional References

Semiconductor design

Archived lecture slides from ECE 581 in Fall 2014:

- Review of Semiconductor Physics
- Specific resistance and capacitance
- FET resistance and WBG materials
- Die size selection example
- Trench and Superjunction Devices
- Superjunction on-resistance

Simulation/Analysis Software

Course Materials

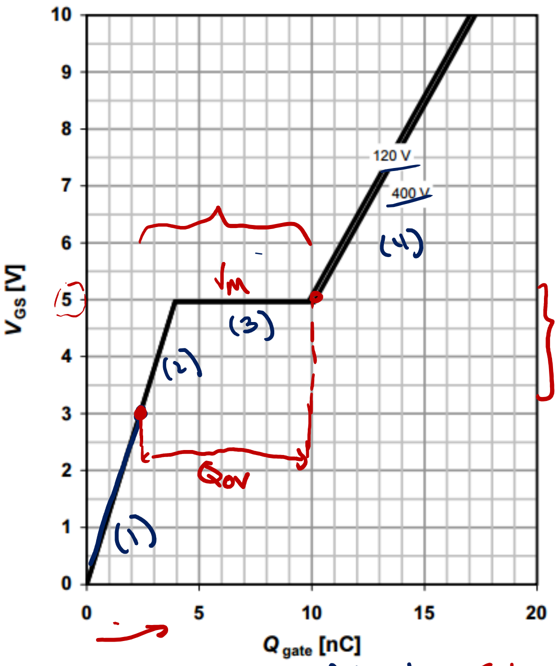
Overlap Time

Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, I_D=0.34 mA	2.5	3	3.5	
Gate resistance	R_G	f=1 MHz, open drain	-	1.8	-	Ω

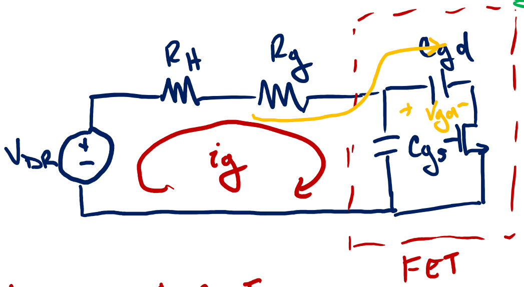
9 Typ. gate charge

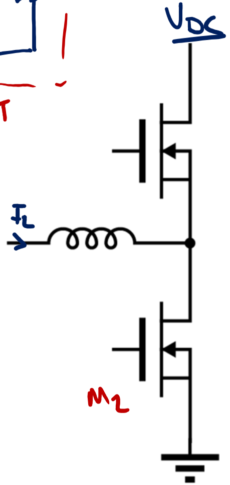
$V_{GS}=f(Q_{gate})$; I_D=5.2 A pulsed

parameter: V_{DD}



$Q_g = \int i_g \, dt \approx I_g t$





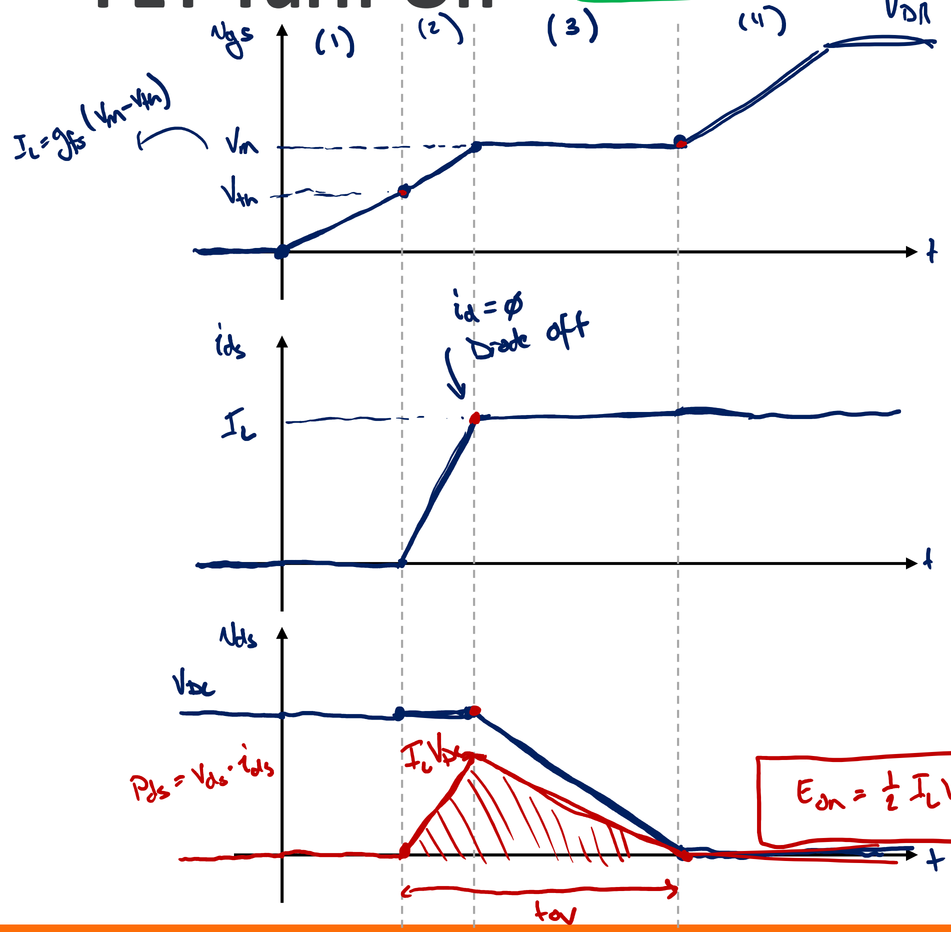
Approx $i_g \approx I_g$

$$i_g \approx \frac{V_{DR} - V_M}{R_H + R_g}$$

$$Q_{ov} \approx I_g t_{ov}$$

FET Turn-On

(M_2, w/ $I_L \to \emptyset$)



(1) Cutoff, Vgs rising

↓

$V_{gs} > V_{th}$

↓

(2) Act/sat, Vgs rising

↓

$V_{gs} \to V_m = \frac{I_L}{g_{fs}} + V_{th}$

↓

(3) Act/sat Vds falling

↓

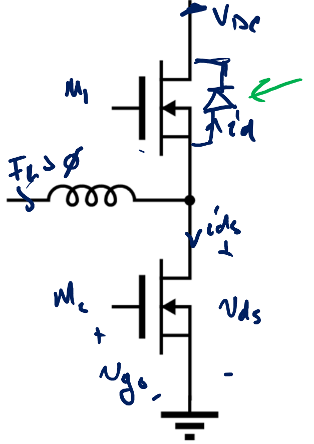
$V_{ds} \approx \emptyset$

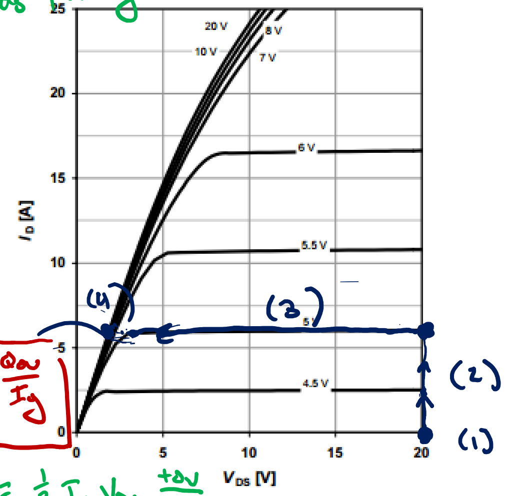
↓

(4) Triode

↓

$V_{gs} \to V_{DR}$



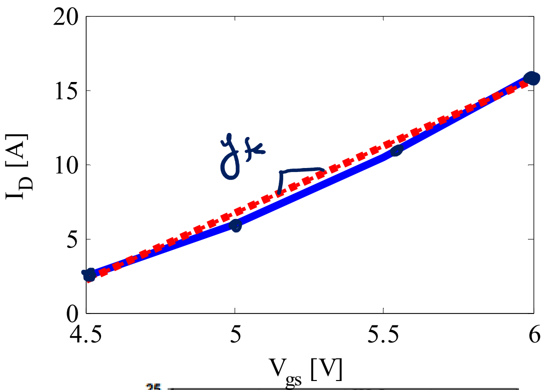


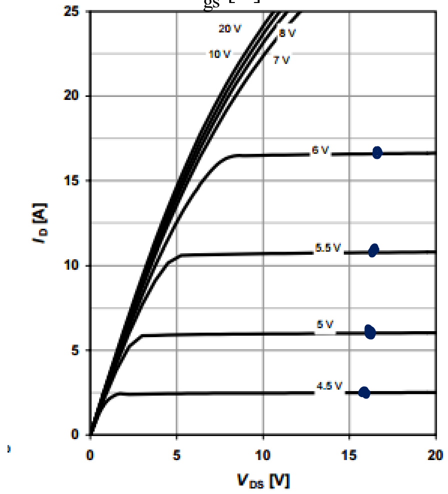
$E_{on} = \frac{1}{2} I_L V_{DC} t_{ov} = \frac{1}{2} I_L V_{DC} \frac{Q_{ov}}{I_g}$

$P_{ov} = E_{on} f_s = \frac{1}{2} I_L V_{DC} \frac{t_{ov}}{T_s}$

Device Transconductance

$\hat{i}_{ds} \approx g_{fs} (\hat{v}_{gs} - V_{th})$

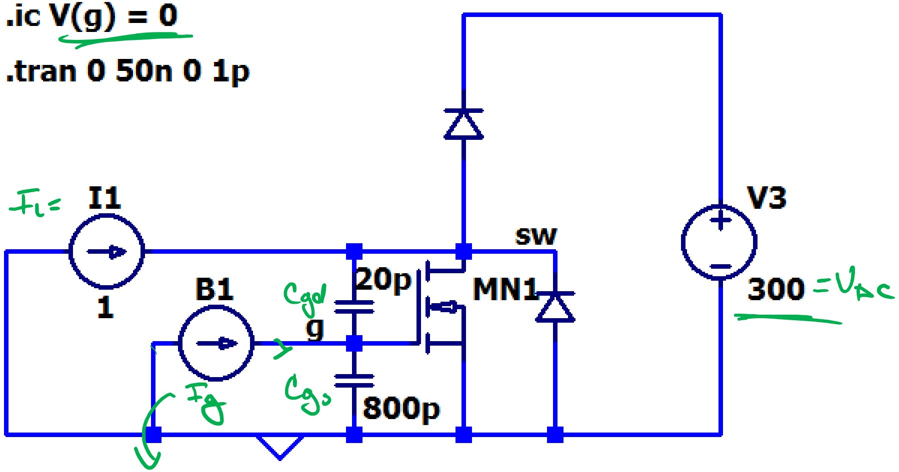




Example Simulation

.ic V(g) = 0

.tran 0 50n 0 1p

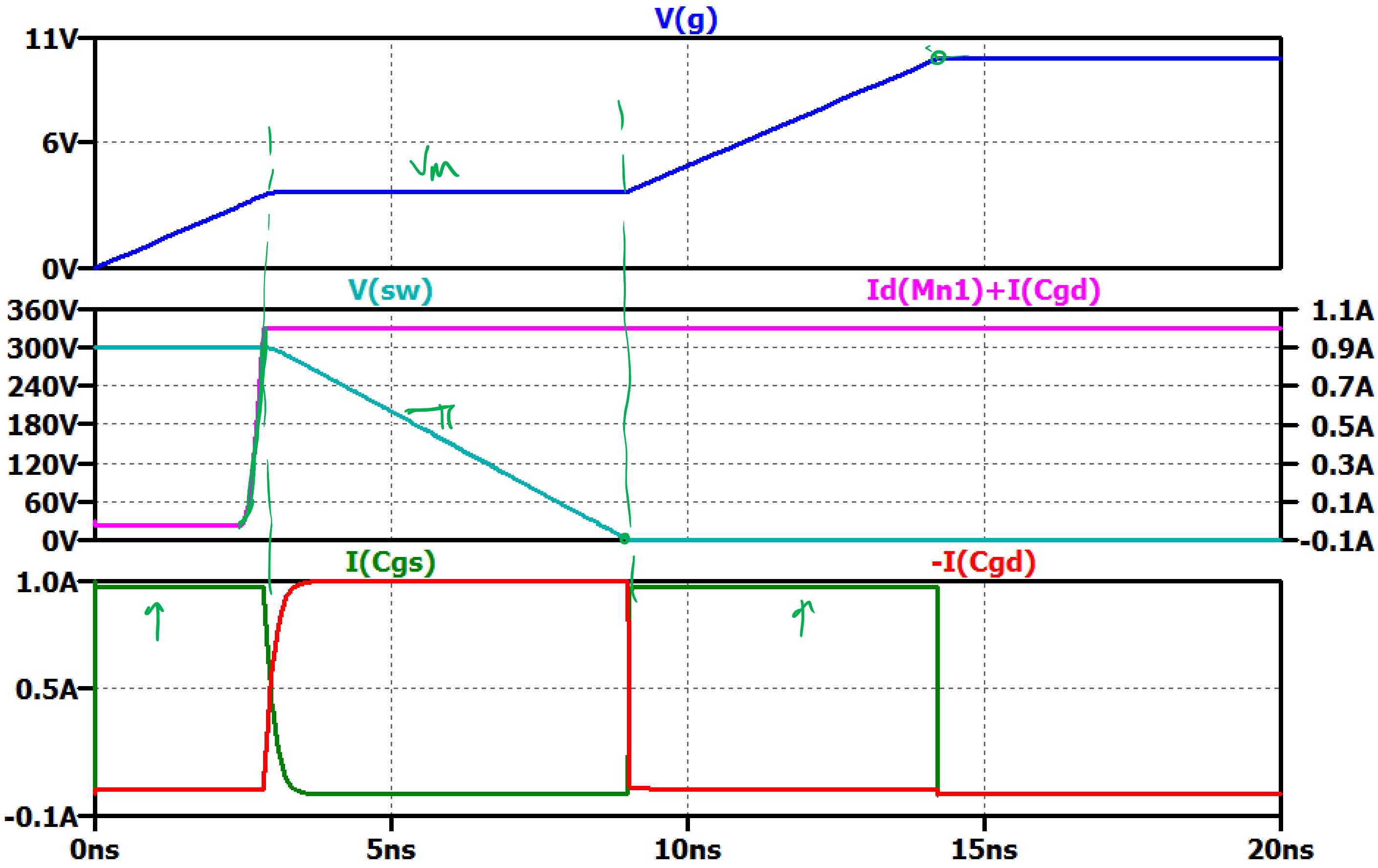


I=IF(V(g)<10,1,0)

.model myD D(n=.01)

.model testFET VDMOS(Rg=.1 Rd=0 Rs=0 Vto=3 Kp=9 Cgdmax=0p
+ Cgdmin=0p Cgs=0p Cjo=1.5f Is=26p Rb=0m Vds=600 Ron=385m Qg=0n)

Simulation Waveforms – Turn On



Turn-Off Transition

(M_2, $I_L > 0$)

Note: Not clamped Voltage

Neglecting