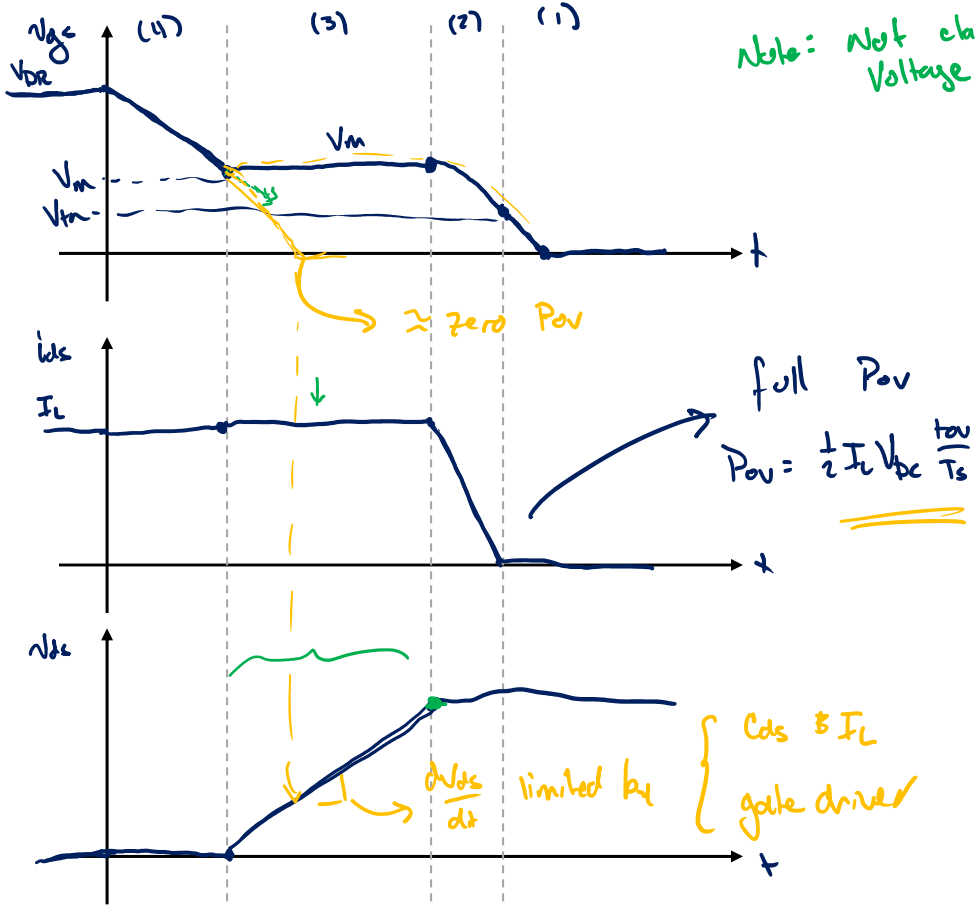
Turn-Off Transition

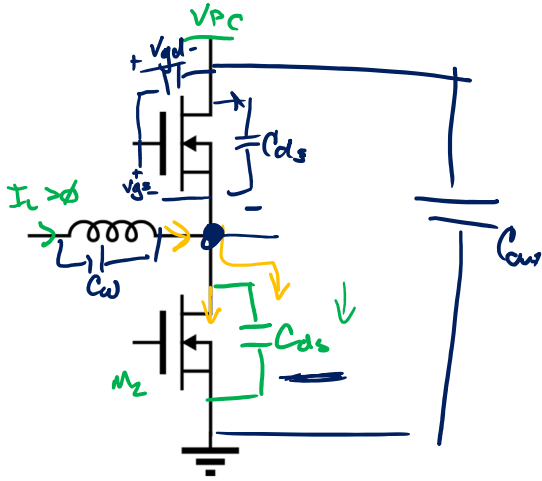


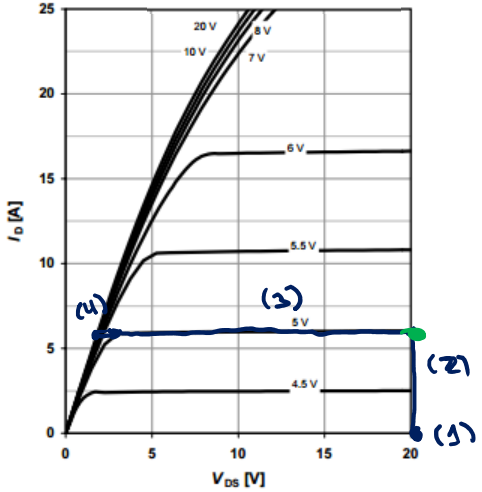
Note: Not clamped Voltage

≈ zero Pov

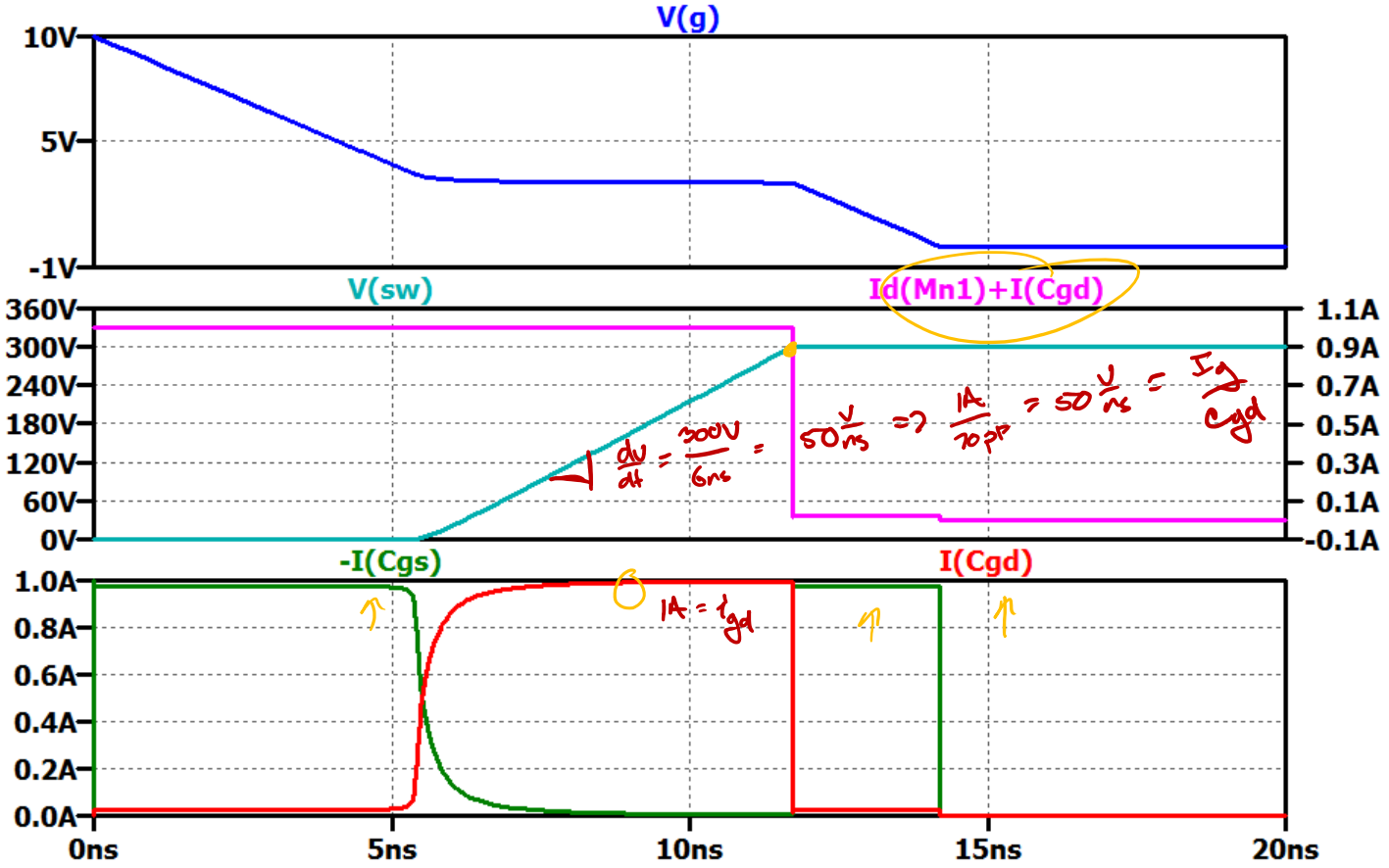
full Pov

$P_{ov} = \frac{1}{2} I_L V_{DC} \frac{t_{ov}}{T_s}$

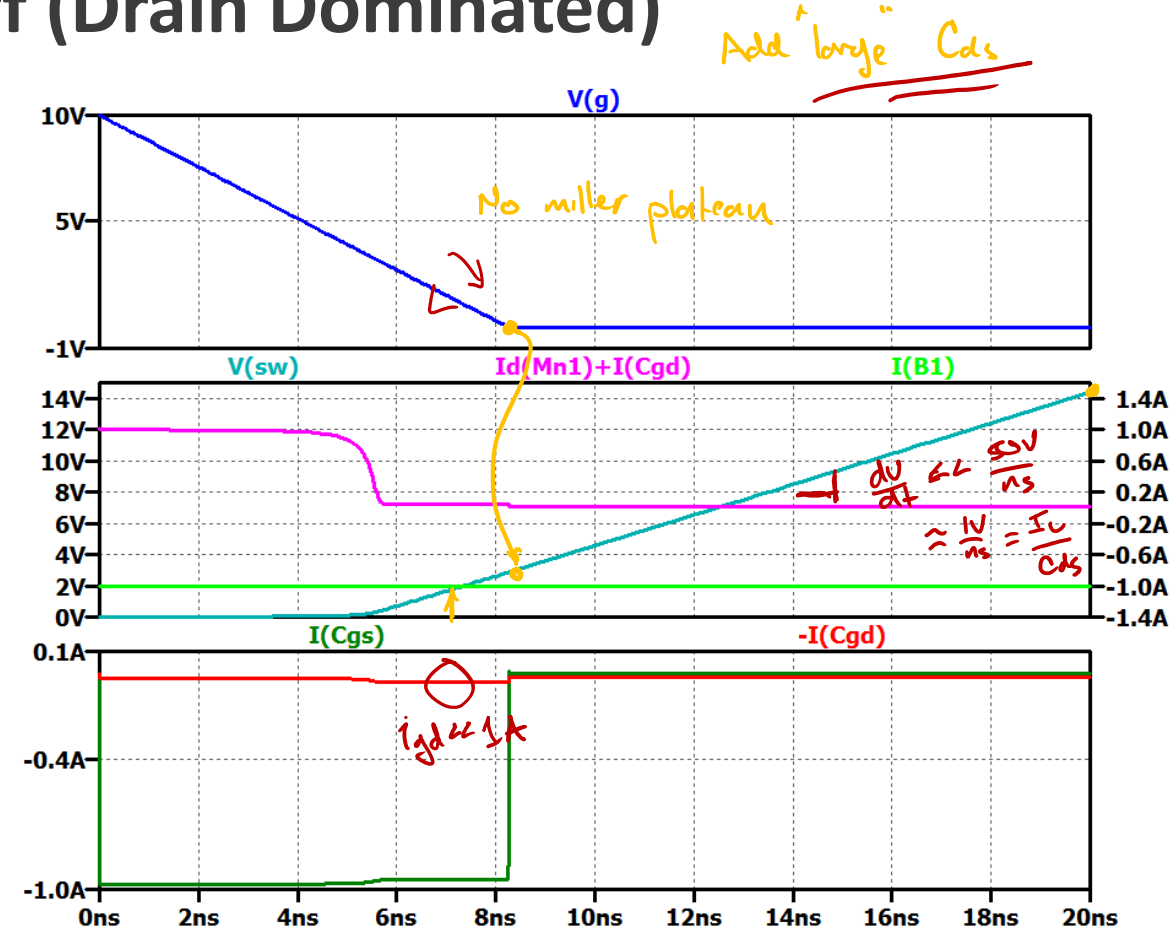




Turn-off


V(g)
10V
5V
-1V
V(sw)
Id(Mn1)+I(Cgd)
360V
300V
240V
180V
120V
60V
0V
1.1A
0.9A
0.7A
0.5A
0.3A
0.1A
-0.1A
-I(Cgs)
I(Cgd)
1.0A
0.8A
0.6A
0.4A
0.2A
0.0A
0ns
5ns
10ns
15ns
20ns

Turn-Off (Drain Dominated)



Gate- vs. Drain-Limited Switching

Drain-limited turn-off

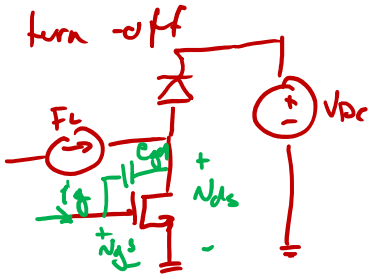
Ideal: FET shuts off before V_{ds} rises significantly

$$\frac{dV_{dc}}{dt} = \frac{I_L}{C_{oss}}$$

$$\frac{I_g}{C_{gd}} \gg \frac{I_L}{C_{oss}}$$

for ≈ zero P_{OV} loss during turn-off

Gate-limited turn-off



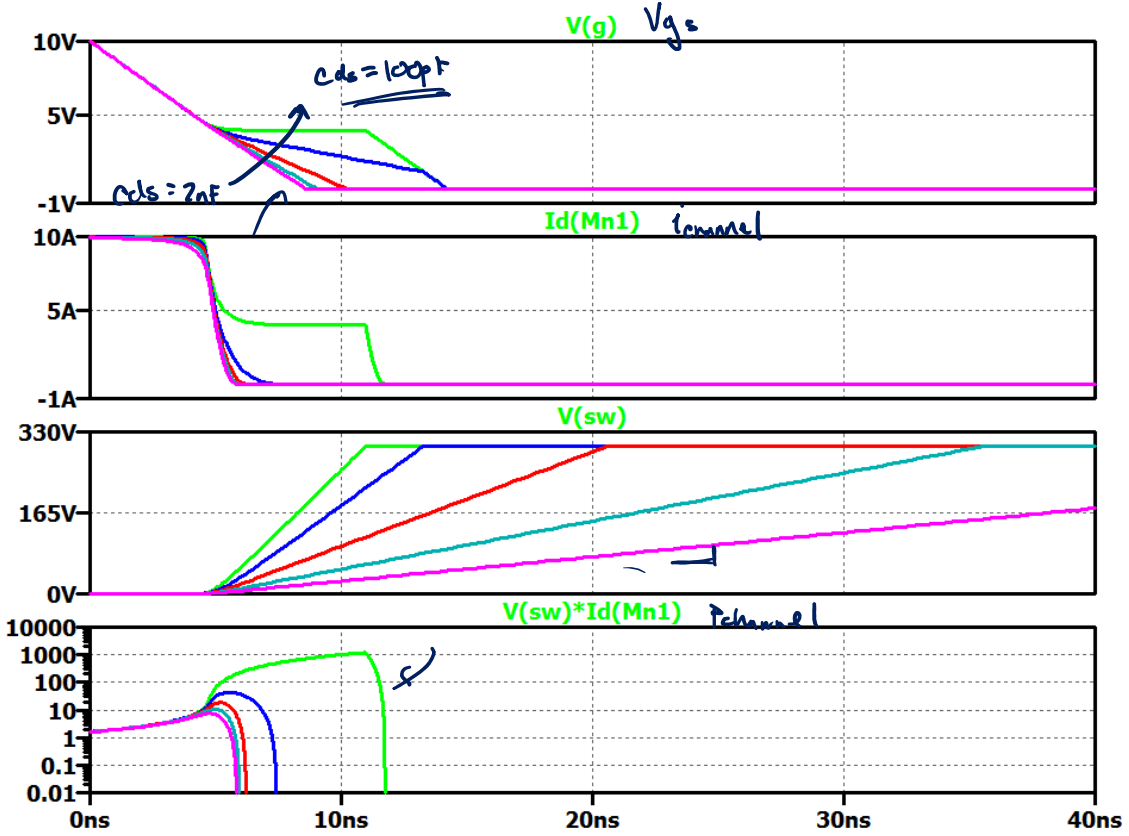
$V_{ds} = V_{gs} + V_{dg}$

If clamped miller plateau

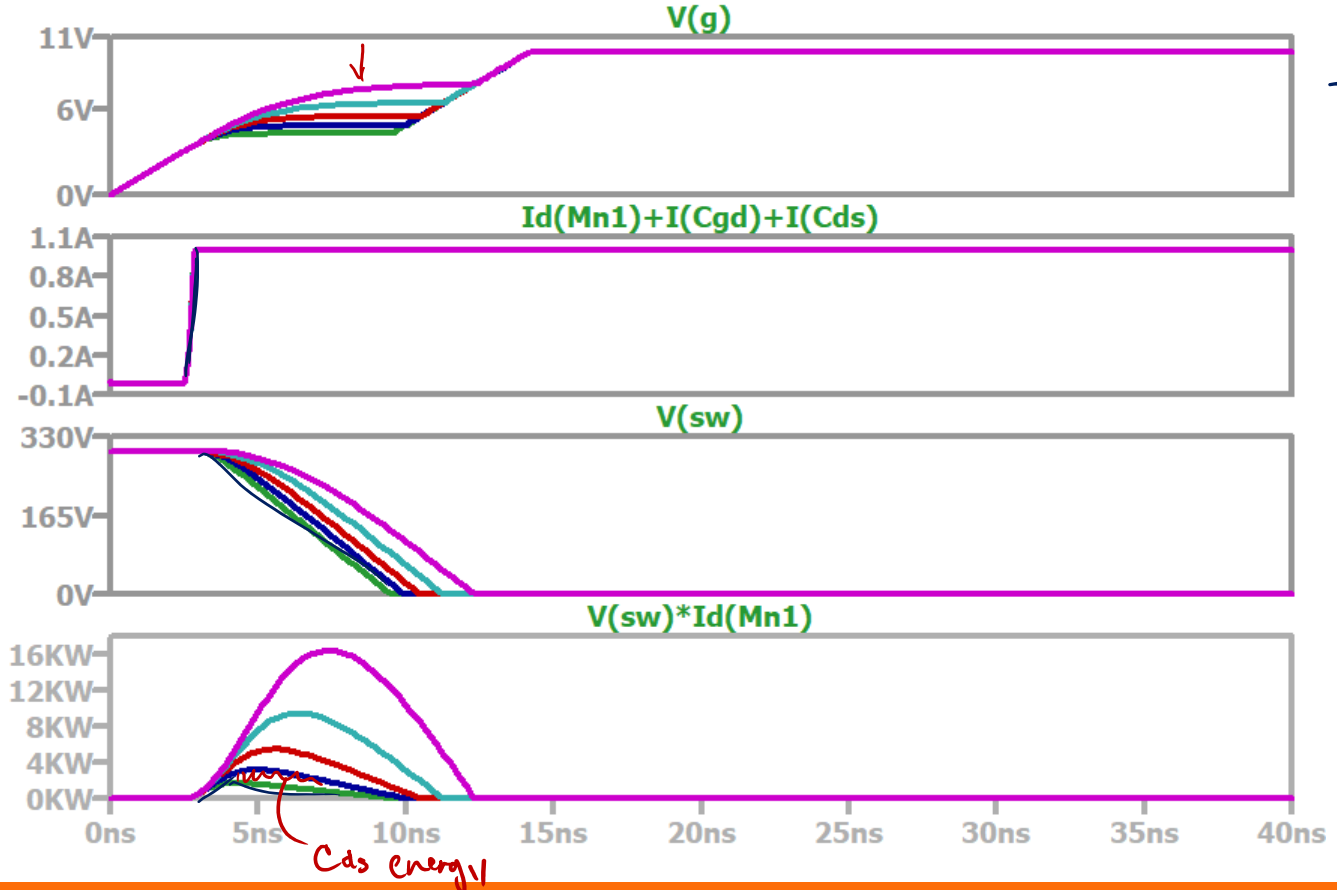
$$\frac{dV_{ds}}{dt} = \frac{dV_{gs}}{dt}^{\nearrow 0} + \frac{dV_{dg}}{dt}$$

$$\frac{dV_{ds}}{dt} = \frac{I_g}{C_{gd}}$$

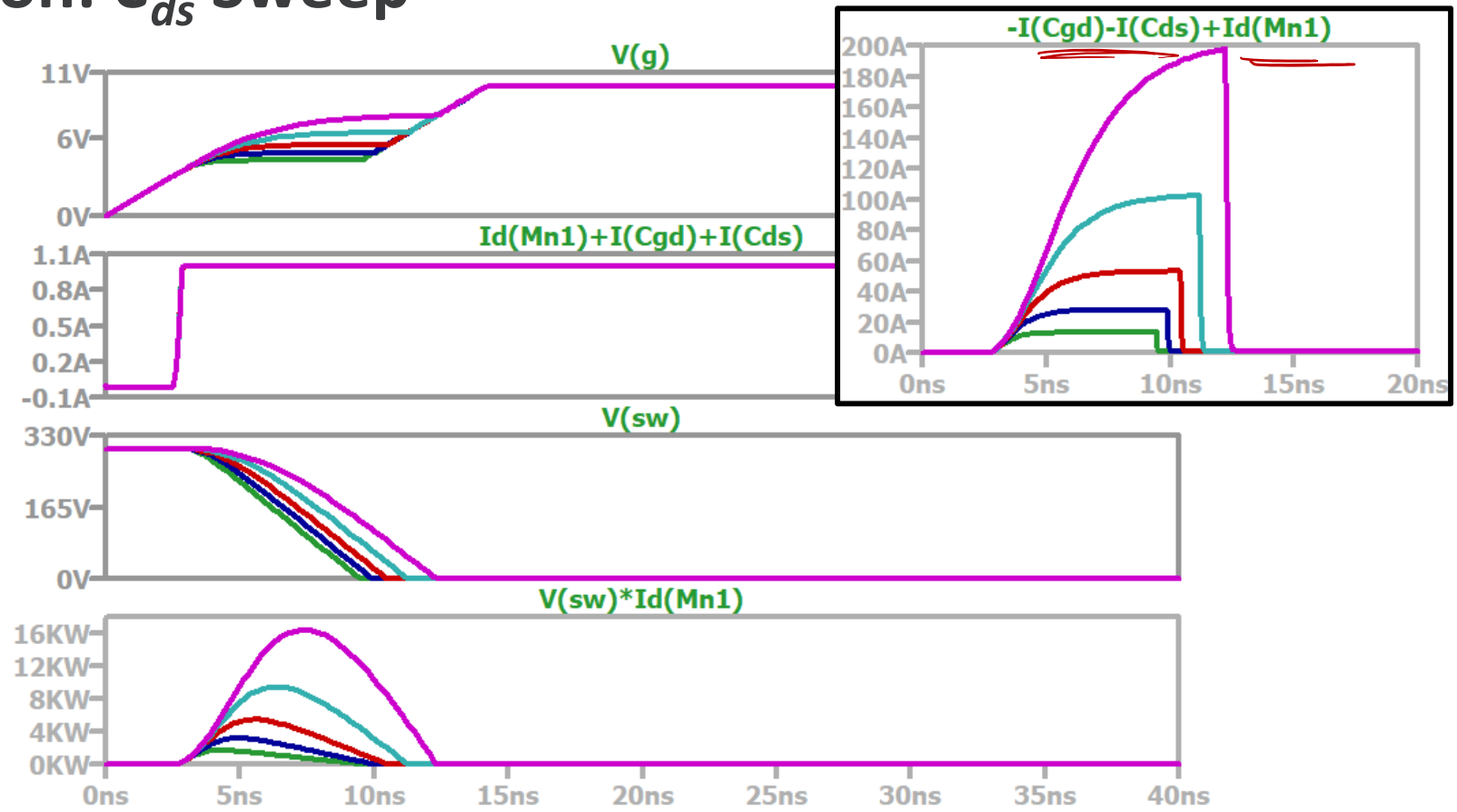
Simulation Results: C_{ds} Sweep



Turn-on: C_{ds} Sweep



Turn-on: C_{ds} Sweep



Limitations on Switching Speed

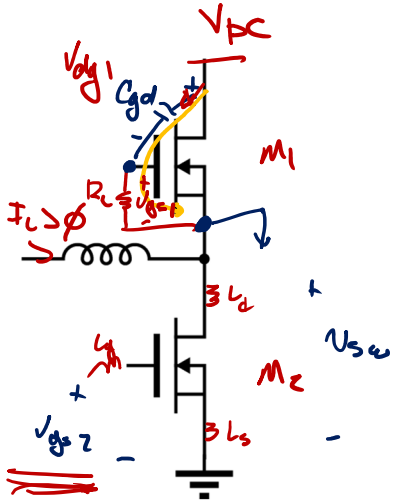
From Pov analysis @ both turn-on & turn-off want maximum I_g & sw speed

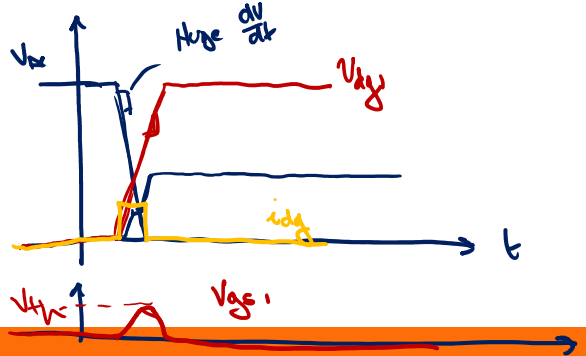
Limits:

(1) $\frac{V_{gg(max)}}{R_g}$ → Max possible GD current

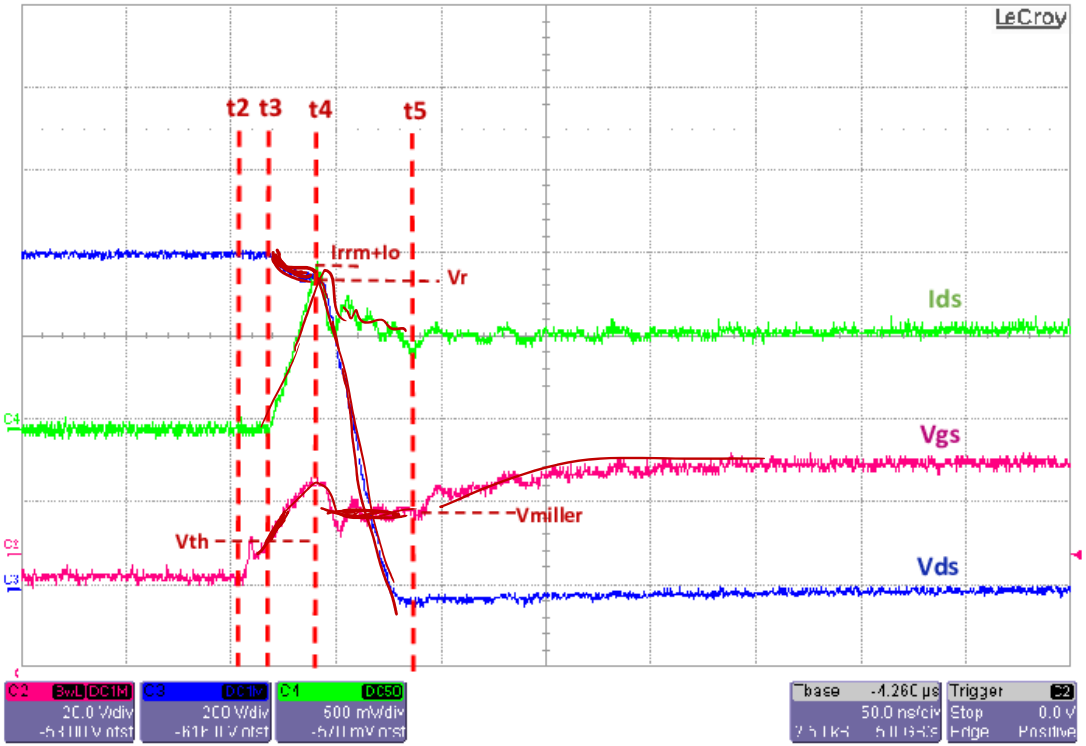
(2) Overshoot / ringing / EMI

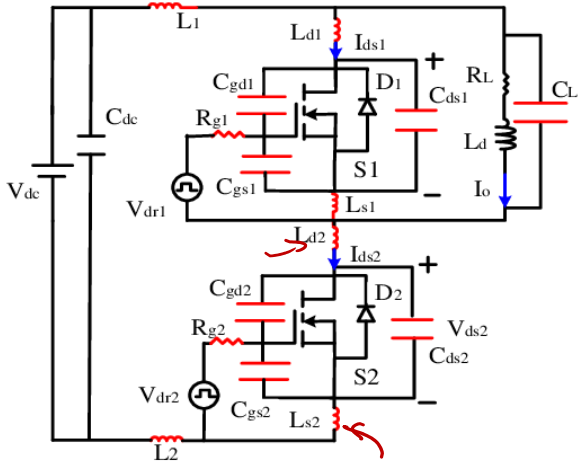
(3) Cross-talk





Switching Waveforms





S. Eskandari et al. (2018). "Accurate Analytical Switching Loss Model for High Voltage SiC MOSFETs Includes Parasitics and Body Diode Reverse Recovery Effects."

Switching Losses in a Half Bridge