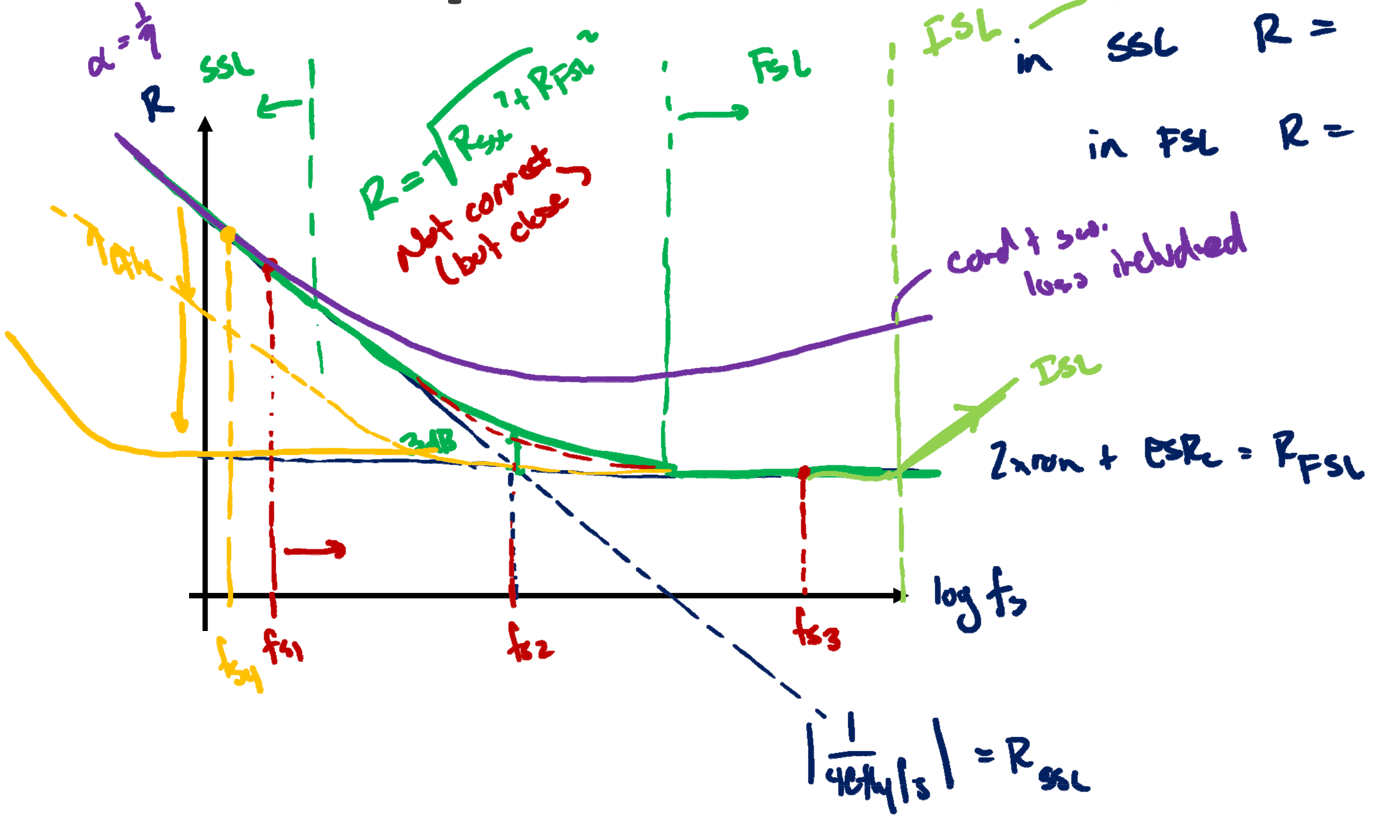
SC Output Resistance



Inductive Switching Limit

in SSL $R = \frac{1}{4C_{fly} f_s}$

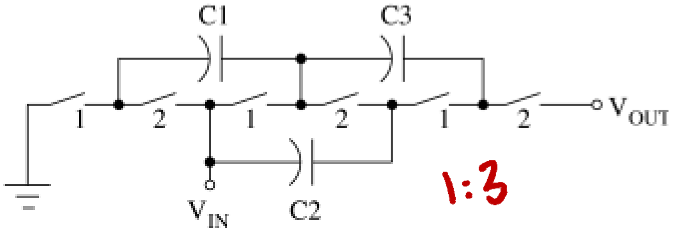
in FSL $R = 2 \times r_{on} + ESR_c + \ldots$

Modeled in this is "charge sharing" losses
- → converter conduction losses
- → switching losses not included
  - No overlap loss (per previous analysis) No clamped inductive switching
  - Coss losses of all FETs

$R = \frac{1}{4C_{fly} f_s}$

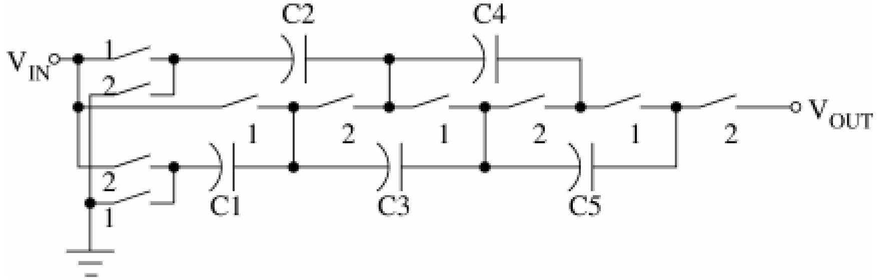
$RC_{fly} = \tau = \frac{T_s}{4} = \frac{t_c}{2}$

SC Converter Topologies (step-up)

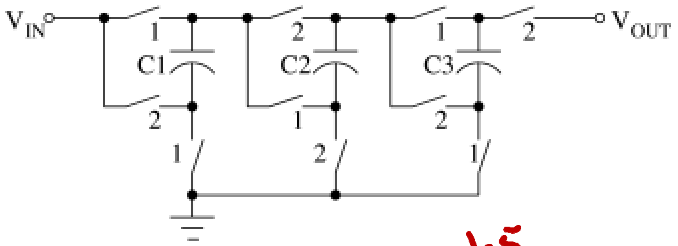


1:3

a) Ladder

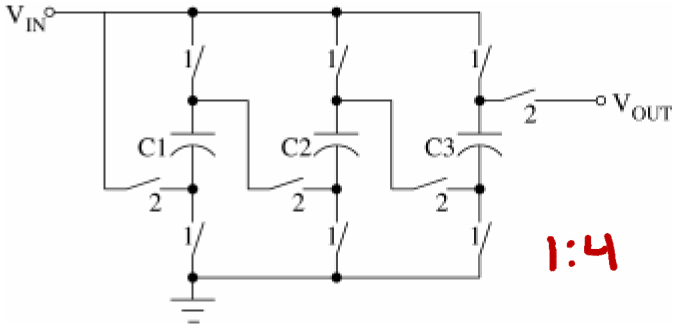


b) Dickson Charge Pump



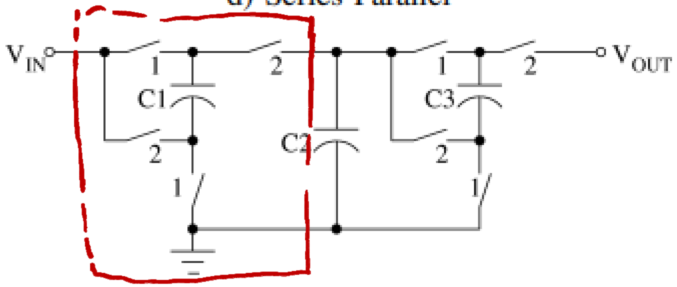
1:5

c) Fibonacci



1:4

d) Series-Parallel



1:2

e) Doubler

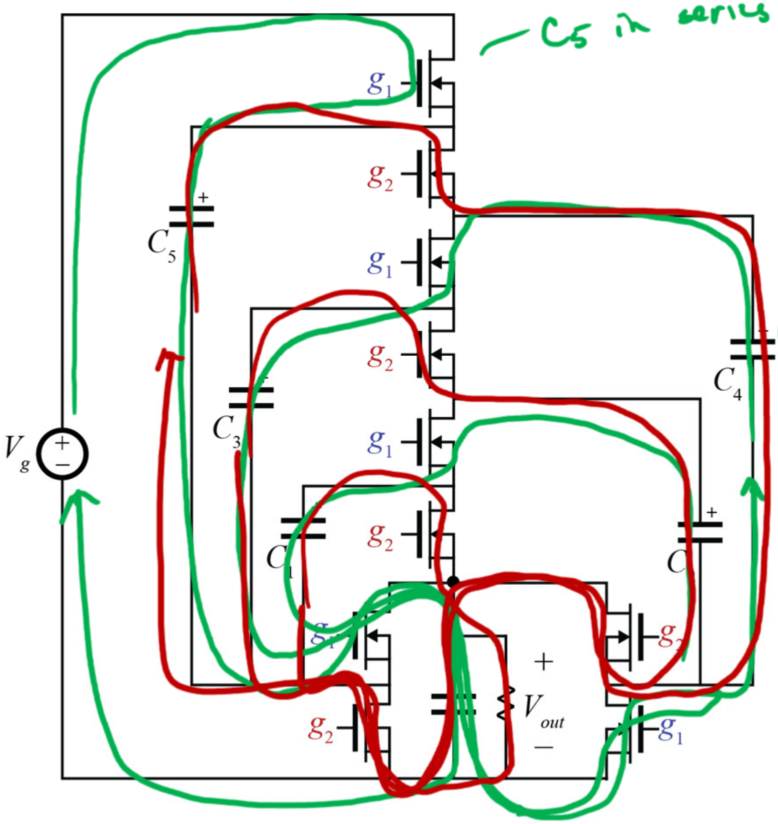
1:4 overall

M Seeman and S. Sanders, “Analysis and Optimization of Switched-Capacitor DC-DC Converters”

Dickson Converter (step-down)

in Ⓘ

in Ⓘⓘ



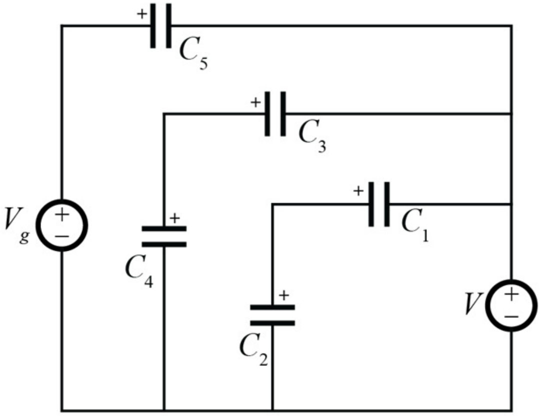
— C5 in series between Vg & Vout

C4. & C3 anti-in series w/ output

C2 & C1 anti-in series w/ Vout

Dickson Subintervals

I



$V_g = 6V$

$V_{c4} = 4V$

$V_{c2} = V_{c1} + V = 2V$

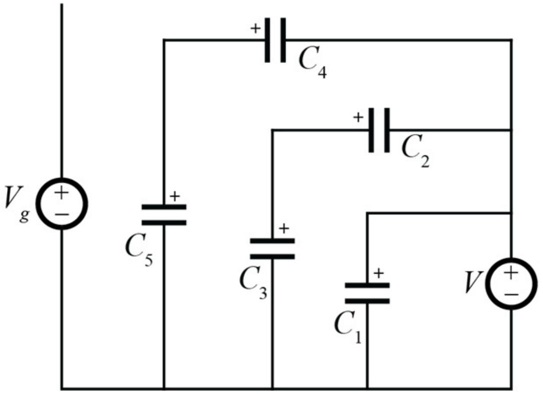
<u>Ideal Analysis</u>:

lossless, let all caps have DC voltage

this is a 6:1 Dickson converter

what is the output resistance?

II

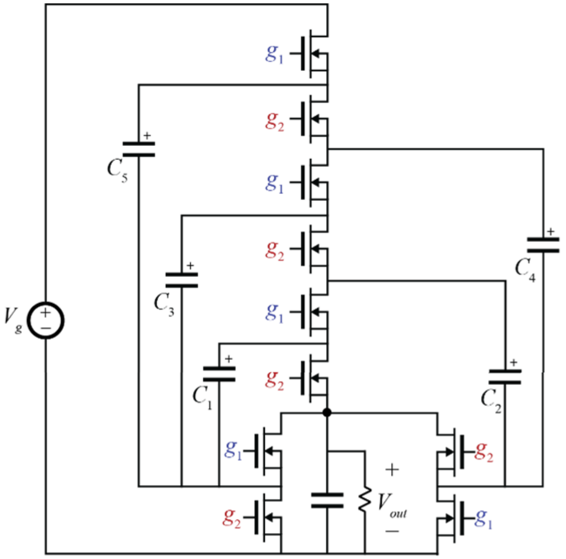


$V_{c5} = 5V$

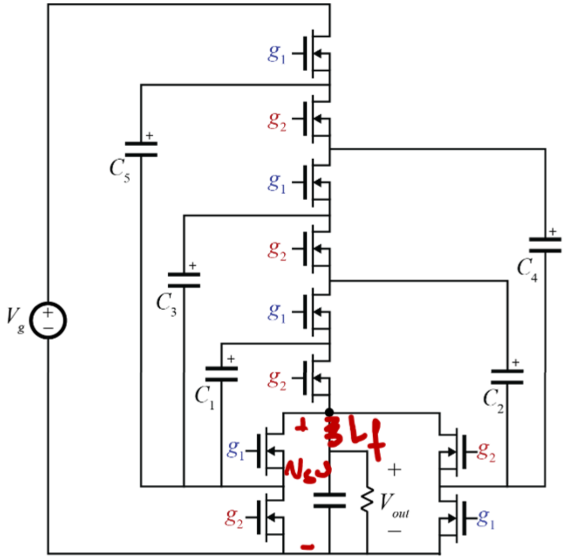
$V_{c3} = 3V$

$V_{c1} = V$

Dickson Converter Variants

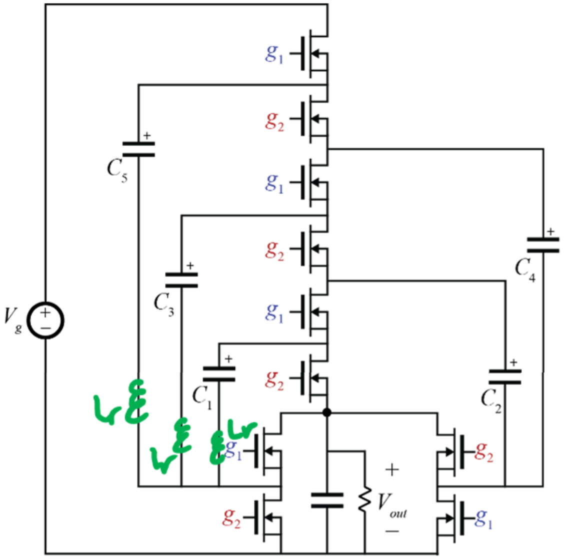


Standard Dickson Converter



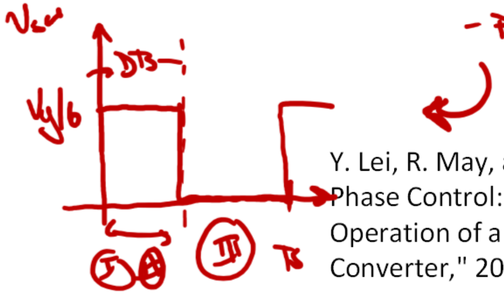
Hybrid Dickson Converter

- Current sink
  - reduces some charge sharing loss
- Can add regulation
  - PWM like a buck w/ $1/6$th V_g



Switched Tank converter

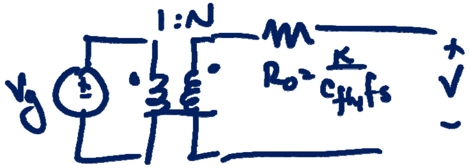
- still unregulated 6:1
- resonant charging of all caps
- reduced switching losses



Y. Lei, R. May, and R. Pilawa-Podgurski, "Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched- Capacitor Converter," 2016

Y. Li, X. Lyu, D. Cao, S. Jiang and C. Nan, "A 98.55% Efficiency Switched-Tank Converter for Data Center Application," 2018.

Charge Vector Analysis: Notation



Goal: Find N & k for any switched cap converter

- Apply Cap-Q balance to all caps in the circuit

q_x^I = Charge flowing through capacitor x in subinterval I ($q_{c_1}^{II}$ = charge through c_1 in $\textcircled{II}$)

$a_x^I = \frac{q_x^I}{q_{out}}$ → q_x^I normalized by q_{out}, the total charge delivered to the output in all subintervals

$q_{out} = q_{out}^I + q_{out}^{II} + \dots$

$$\bar{a}^I = [\underset{\text{input}}{a_{in}^I} \quad \underbrace{a_{c_1}^I \quad a_{c_2}^I \dots a_{cN}^I}_{\text{for converter w/ N flying caps}} \quad \underset{\text{output}}{a_{out}^I}]$$

$$\bar{v}^I = [V_g \quad v_{c1}^I \quad v_{c2}^I \dots v_{cN}^I \quad V]$$

V_x^I = Voltage on C_x at the <u>end</u> of subinterval I

M. Makowski and D. Maksimovic, “Performance Limits of Switched-Capacitor DC-DC Converters,” 1995
M Seeman and S. Sanders, “Analysis and Optimization of Switched-Capacitor DC-DC Converters,” 2008

Charge Vector Analysis: Rules

- KVL & KCL equations apply
- Cap-Q balance, for all caps $\int_0^{T_s} i_{cx}\,dt = Q_{cx} = 0$ in steady state

In a 2-subinterval converter

$$q_{cx}^{I} + q_{cx}^{II} = 0 \rightarrow q_{cx}^{I} = -q_{cx}^{II}$$

same for a_{cx}