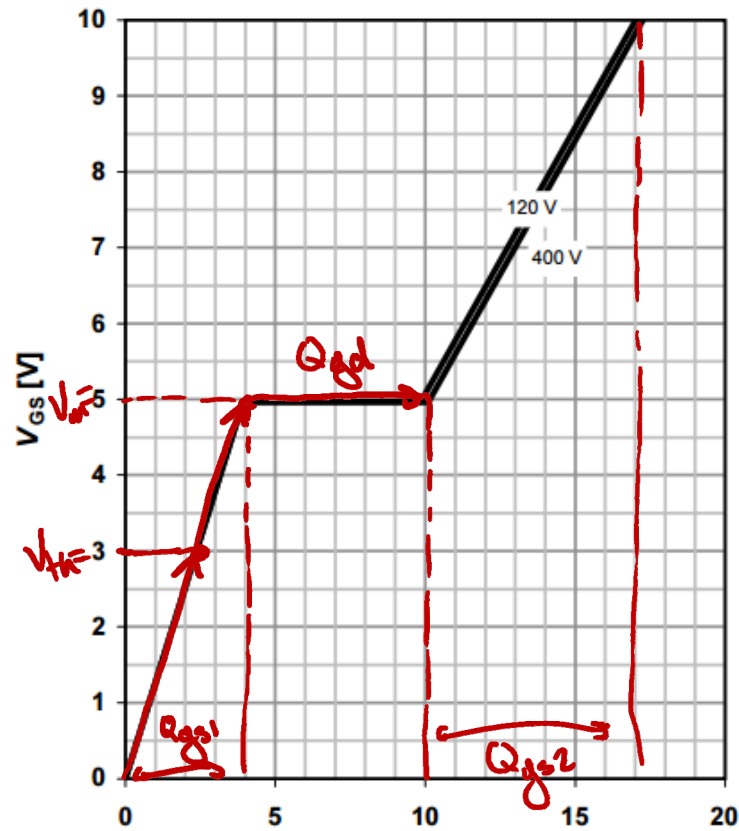


Gate Charge

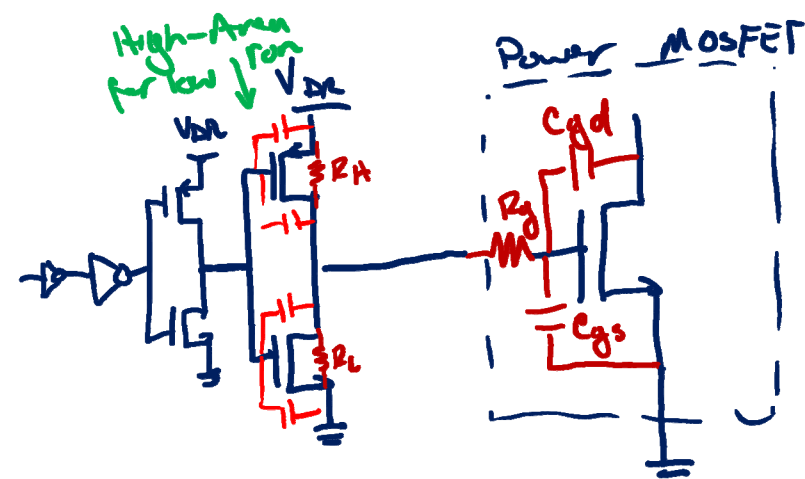
9 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 5.2$ A pulsed

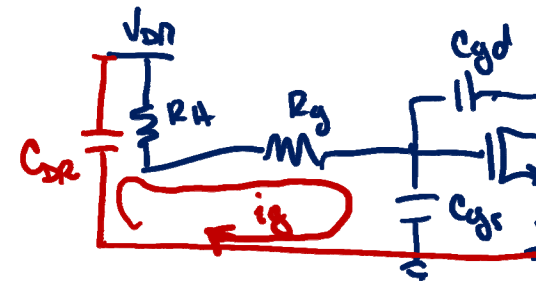
parameter: V_{DD}



$$Q_g = Q_{gate} [nC] = \int_0^t i_{gdt} dt$$



Turn-ON



$$E_{DR,ON} = \int_{on} V_{DS} \cdot i_{gdt} dt$$

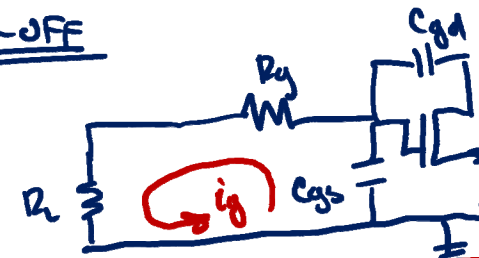
$$= V_{DS} \int i_{gdt} dt$$

$$= V_{DS} Q_g$$

$$\approx \frac{1}{2} C_{gs} V_{DS}^2 \text{ still}$$

all of the energy lost

Turn-OFF



$$P_g = Q_g V_{DS} f_s \rightarrow \text{From GD supply}$$

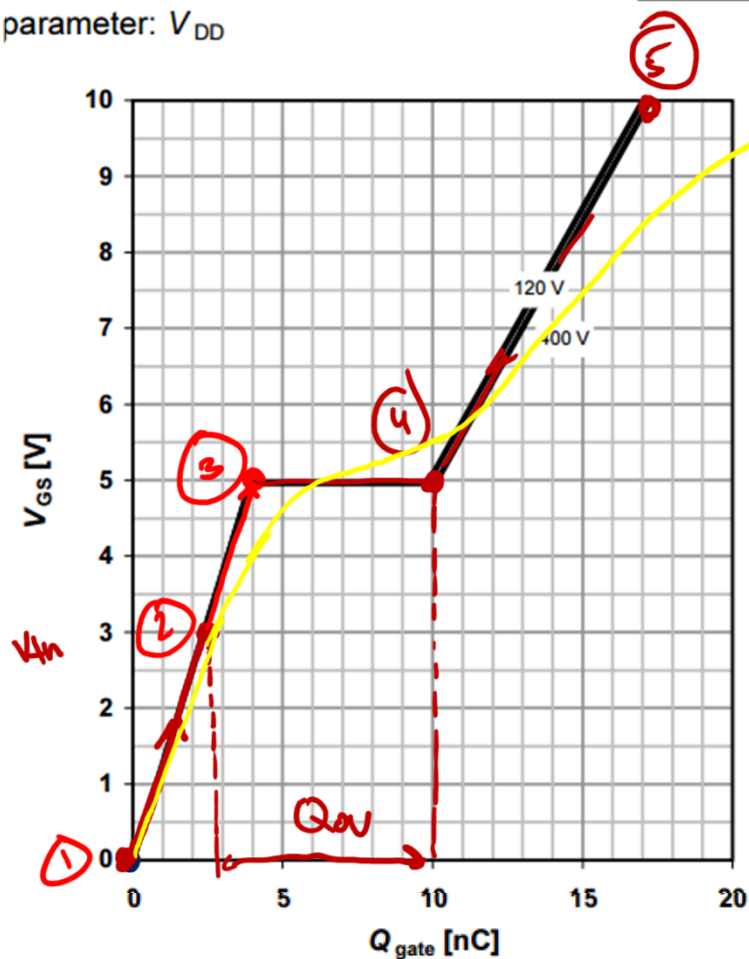
Overlap Time

9 Typ. gate charge

$V_{GS}=f(Q_{gate}); I_D=5.2\text{ A pulsed}$

parameter: V_{DD}

Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=0.34\text{ mA}$	2.5	<u>3</u>	3.5
Gate resistance	R_G	$f=1\text{ MHz, open drain}$	-	1.8	- Ω



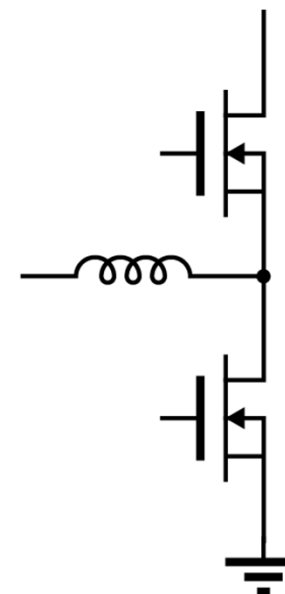
Assume gate driver supplies
a constant current I_g

$$Q_g = \int_0^t i_g(t) dt = I_g t$$

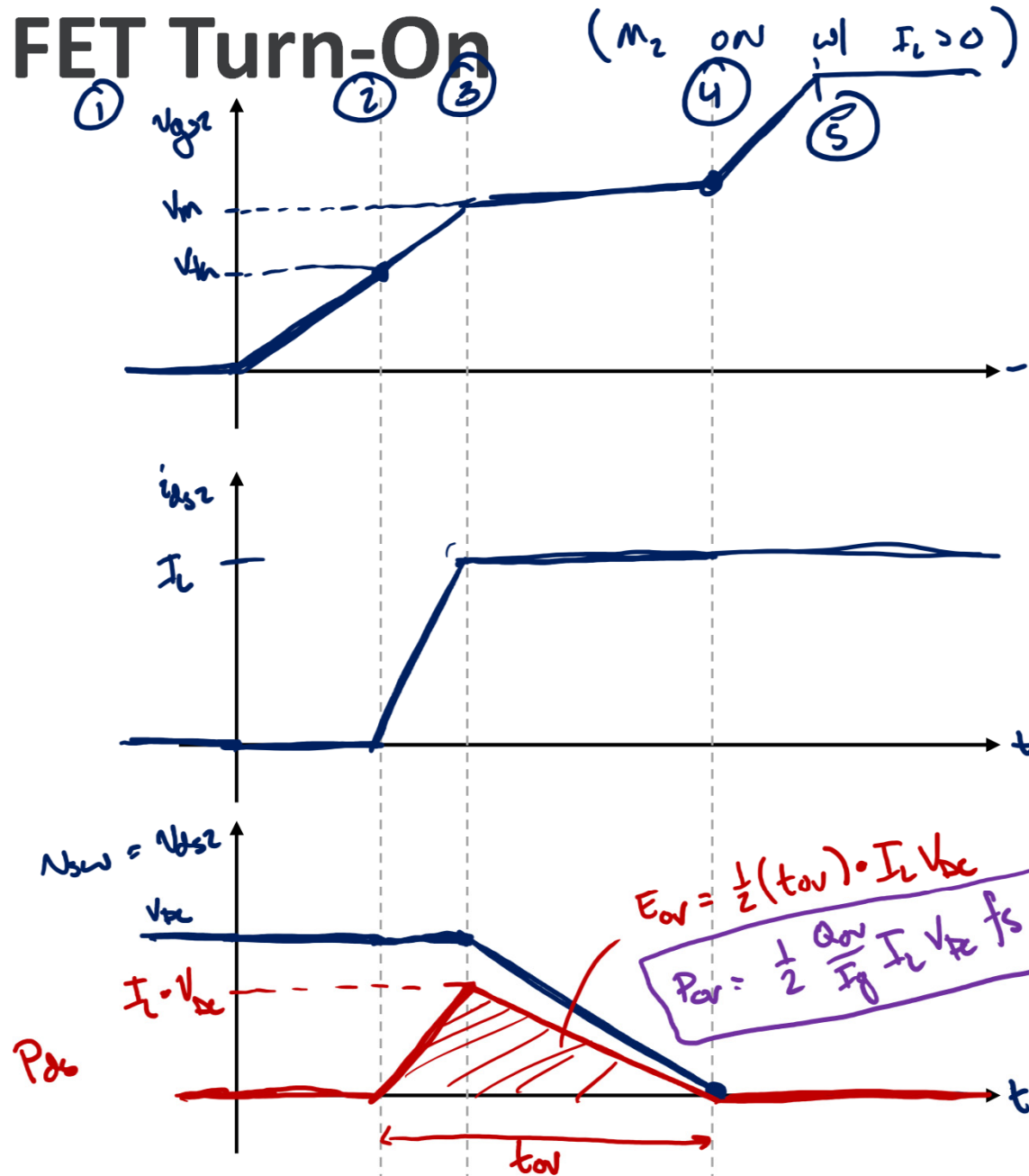
$$t_{ov} = \frac{Q_{ov}}{I_g}$$

for most of t_{ov}

$$I_g \approx \frac{V_{DD} - V_{th}}{R_g + R_{th}}$$



FET Turn-On



① Device in cutoff
Gate drive begins supplying I_g

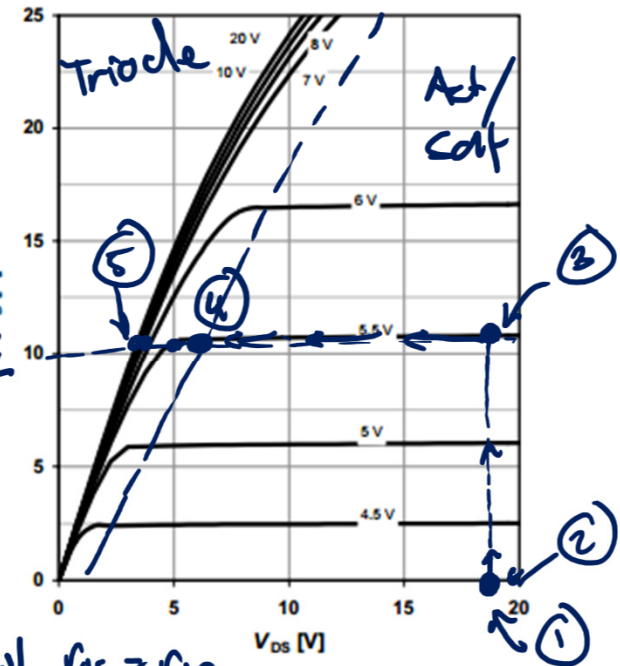
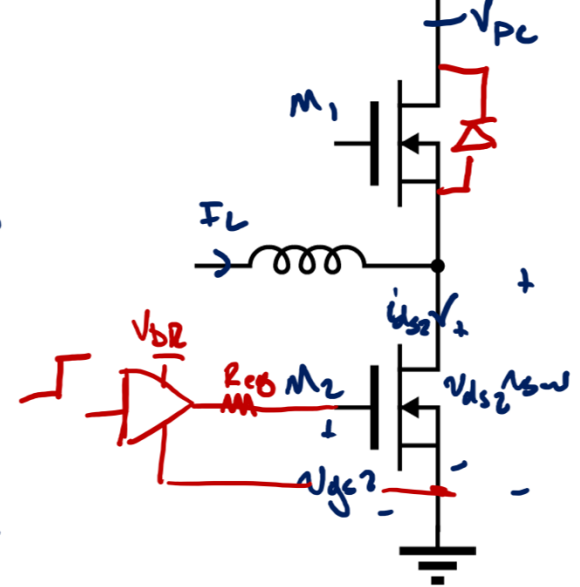
② $V_{gs} \rightarrow V_{th}$
Device comes out of cutoff into Act/sat

③ $V_{gs} = V_{th} = V_{th} + g_m I_L$

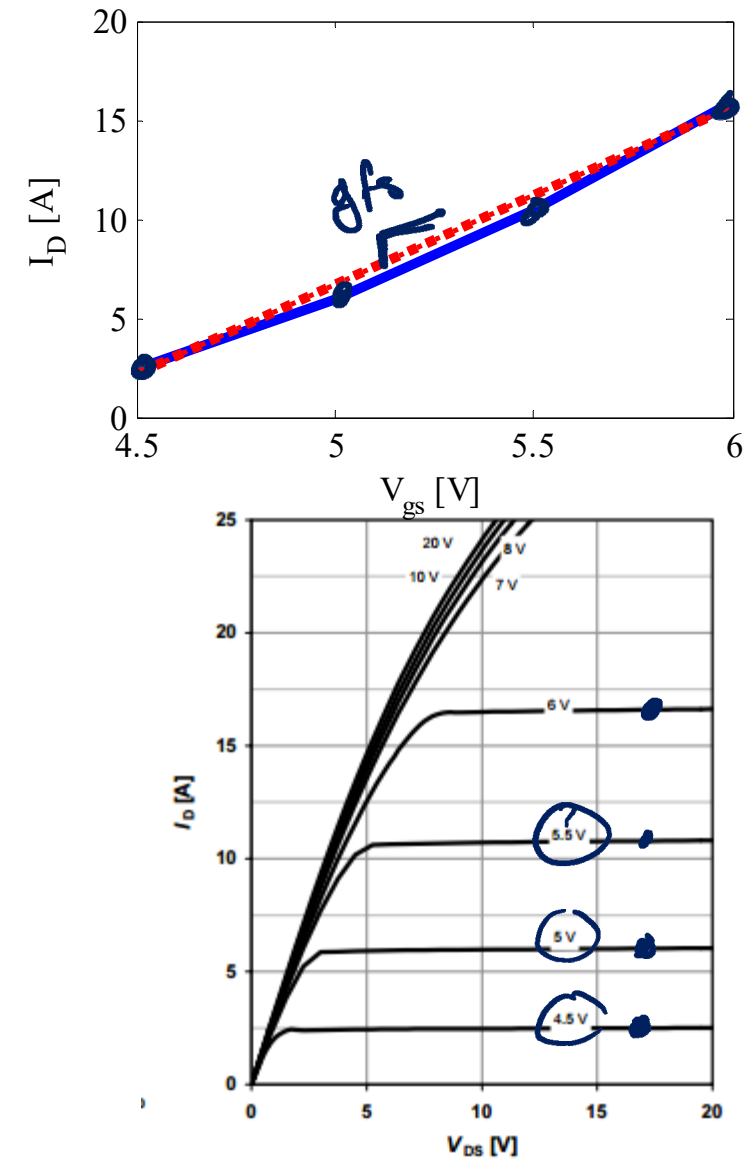
Diode off
 V_{ds} drops & $\frac{dV_{gs}}{dt}$ takes all I_g into C_{gd}

④ Device enters triode

⑤ Device on w/ $V_{as} = V_{an}$



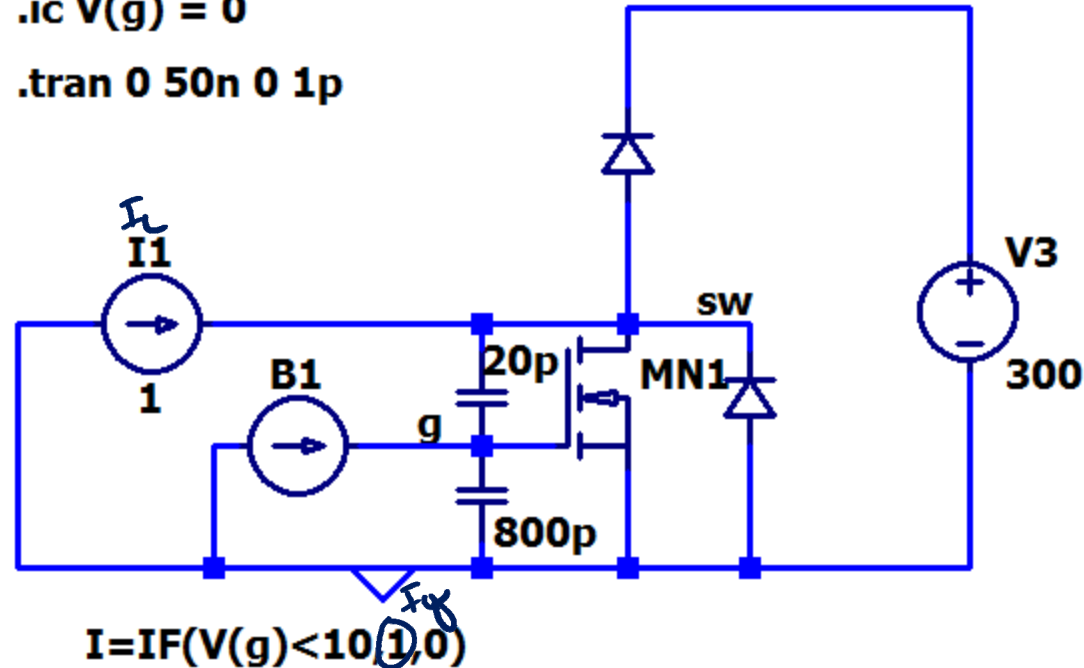
Device Transconductance



Example Simulation

.ic V(g) = 0

.tran 0 50n 0 1p

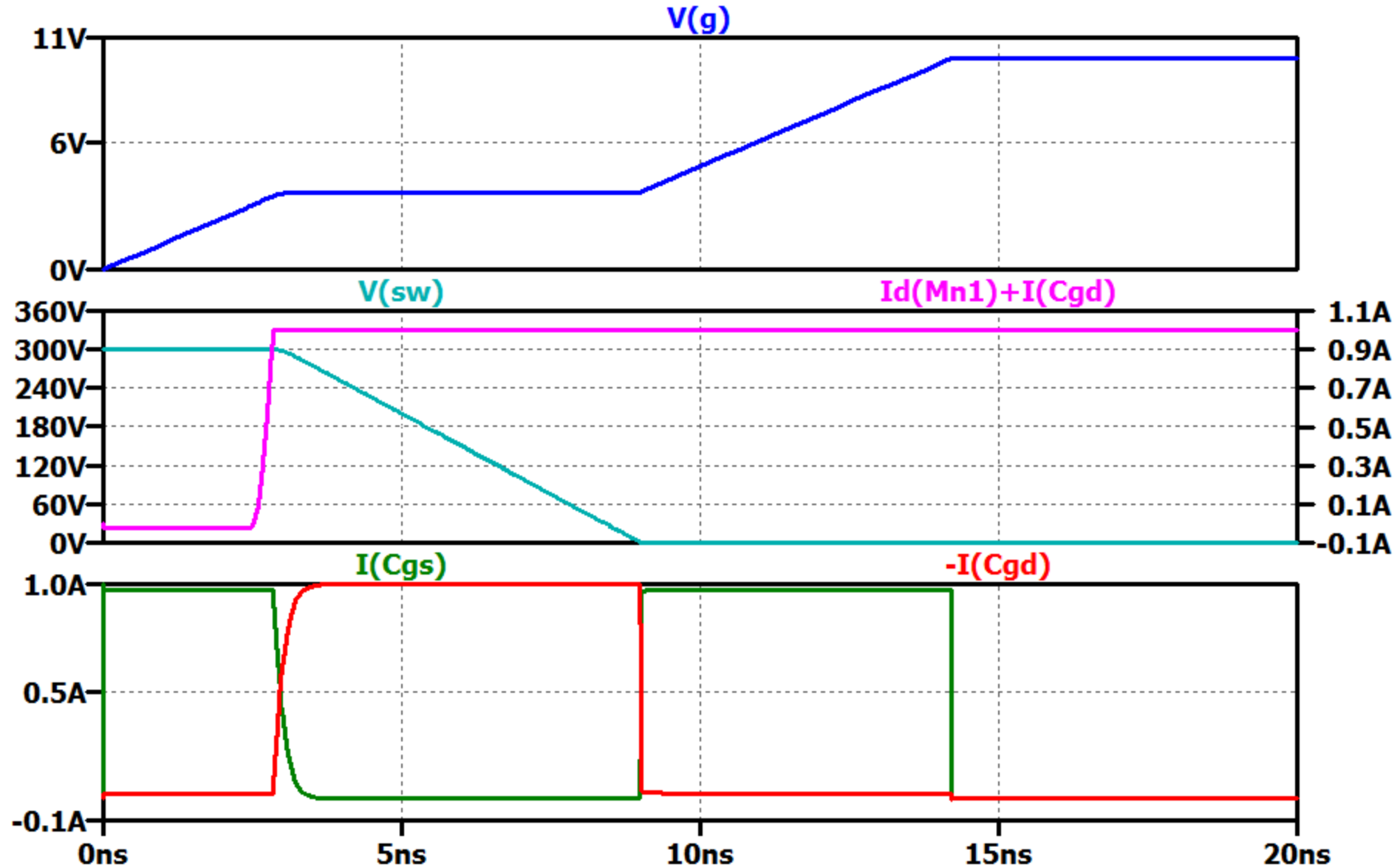


$I = IF(V(g) < 10, 1, 0)$

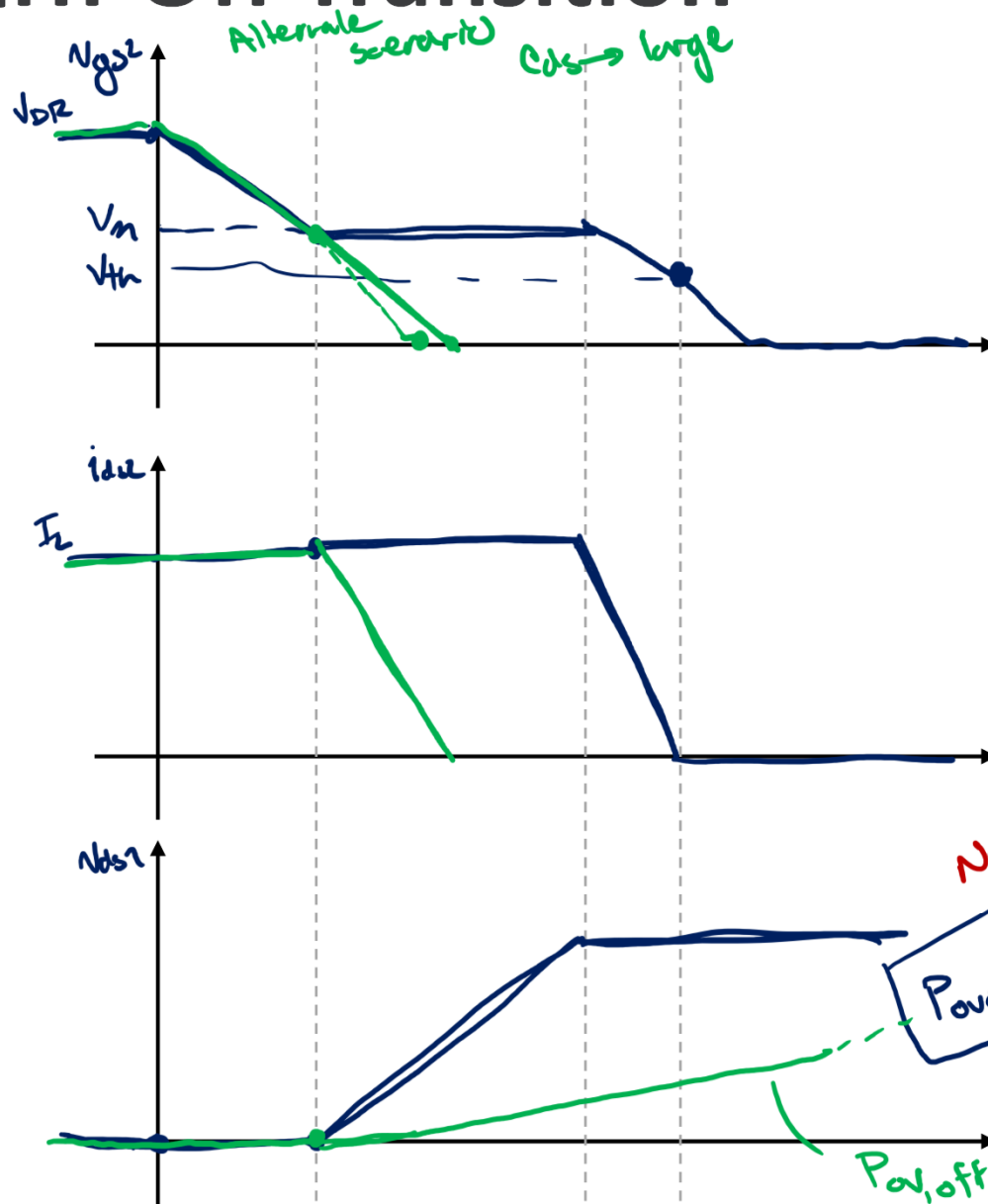
.model myD D(n=.01)

.model testFET VDMOS(Rg=.1 Rd=0 Rs=0 Vto=3 Kp=9 Cgdmax=0p
+ Cgdmin=0p Cgs=0p Cjo=1.5f Is=26p Rb=0m Vds=600 Ron=385m Qg=0n)

Simulation Waveforms – Turn On



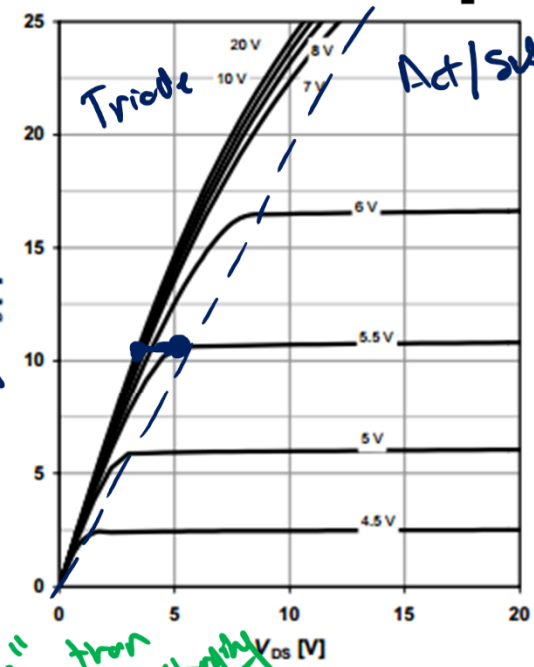
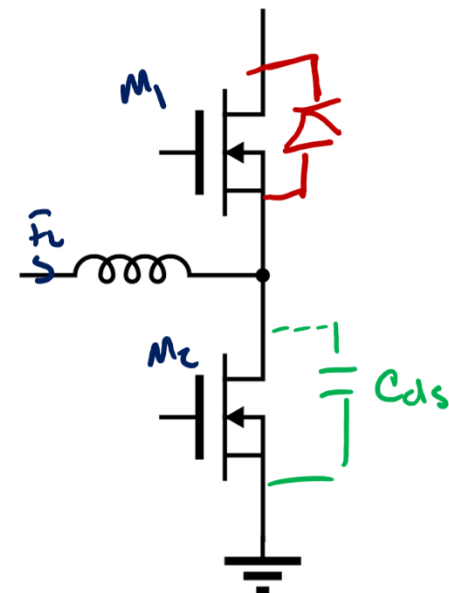
Turn-Off Transition $(M_2, \bar{r}_L > 0)$



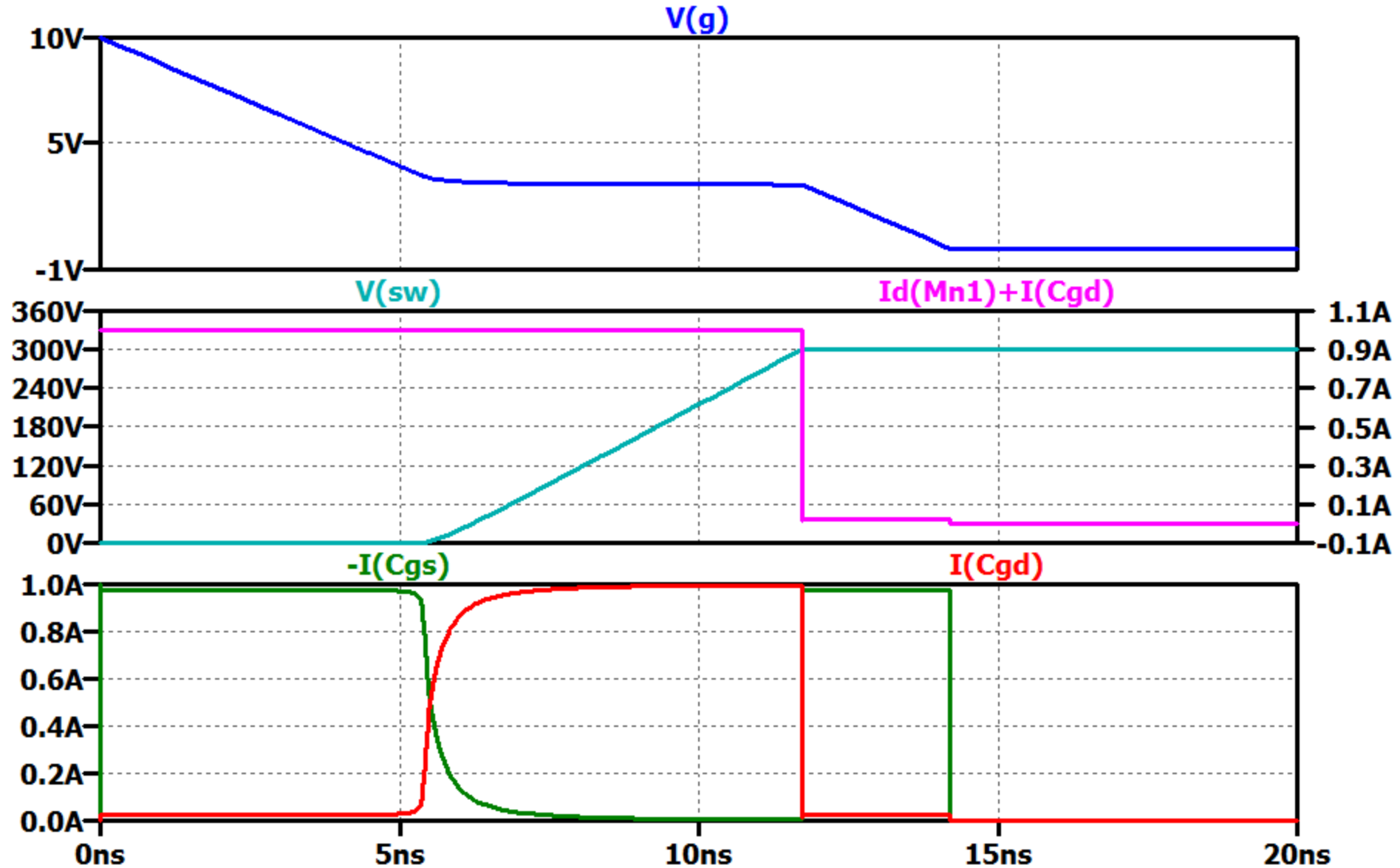
Not necessary

$$P_{avg, off} = \frac{1}{2} \frac{Q_{sw}}{T_g} V_{th} I_{L, fs}$$

$P_{avg, off} \ll \frac{1}{2} \frac{Q_{sw}}{T_g} V_{th} I_{L, fs}$
if gate driver "faster" than C_{ds} charging



Turn-Off



Turn-Off (Drain Dominated)

