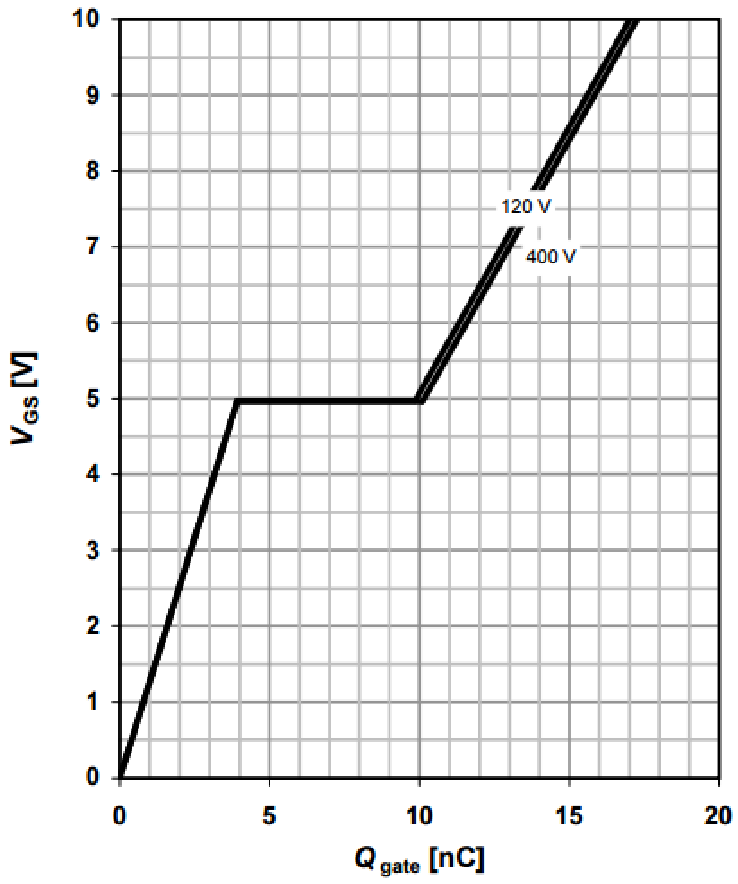
Overlap Time

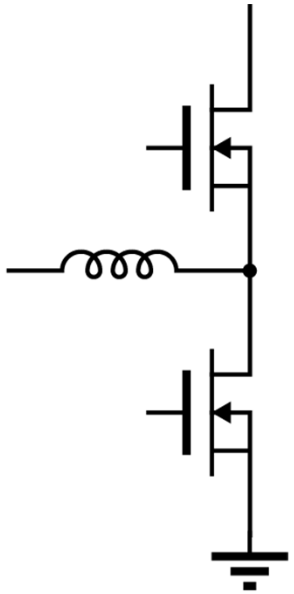
9 Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=5.2 A pulsed

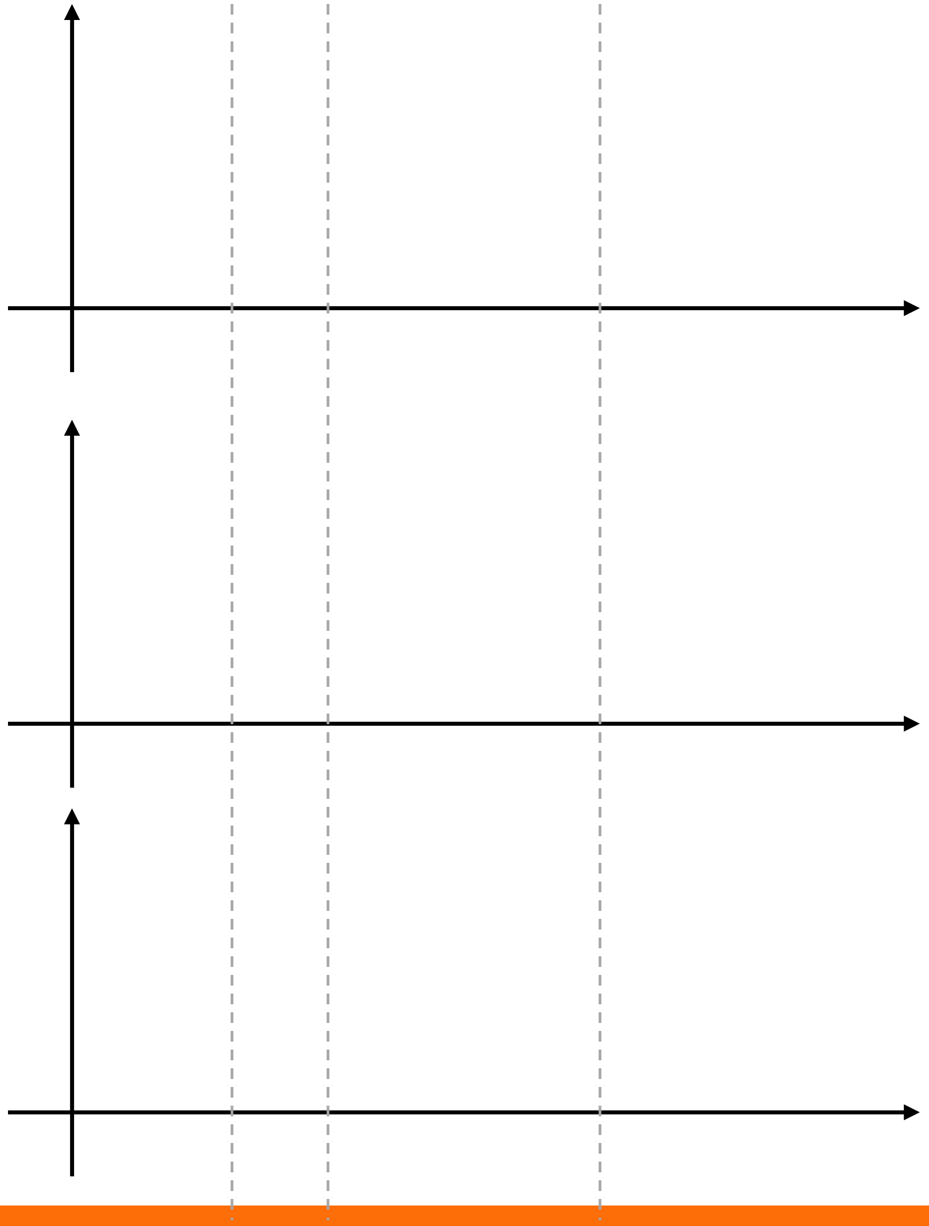
parameter: V_{DD}

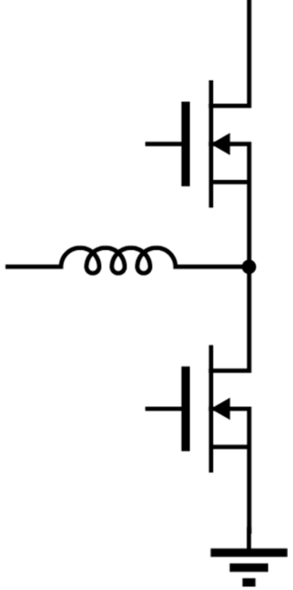


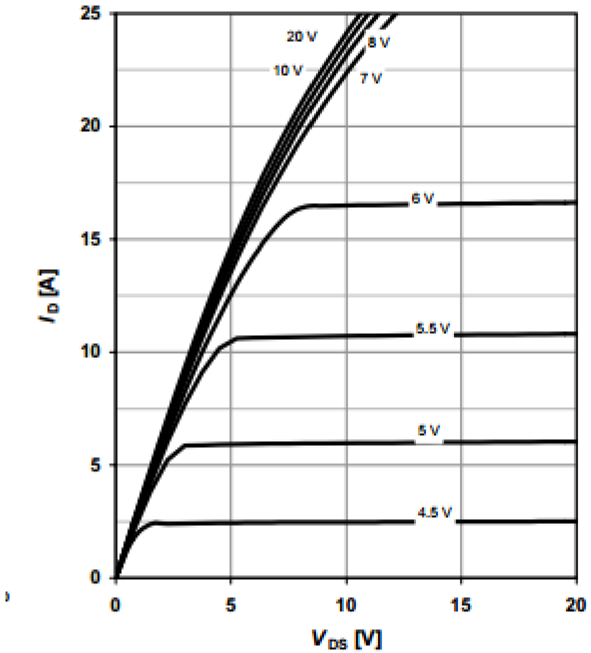
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.34 mA	2.5	3	3.5	
Gate resistance	R_G	f=1 MHz, open drain	-	1.8	-	Ω



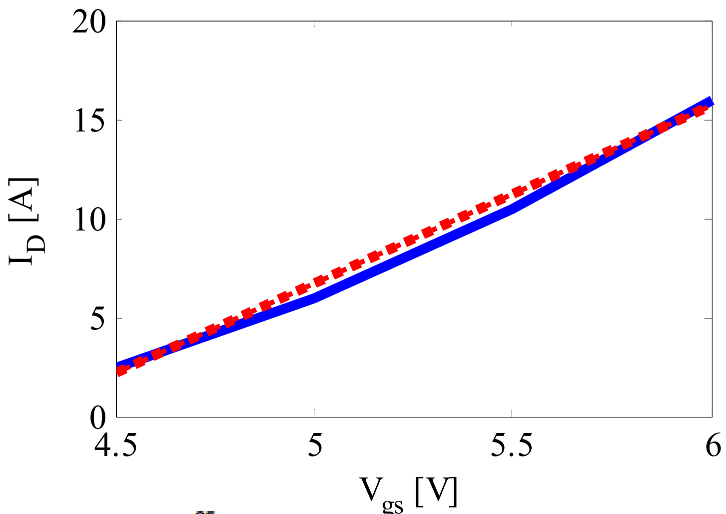
FET Turn-On

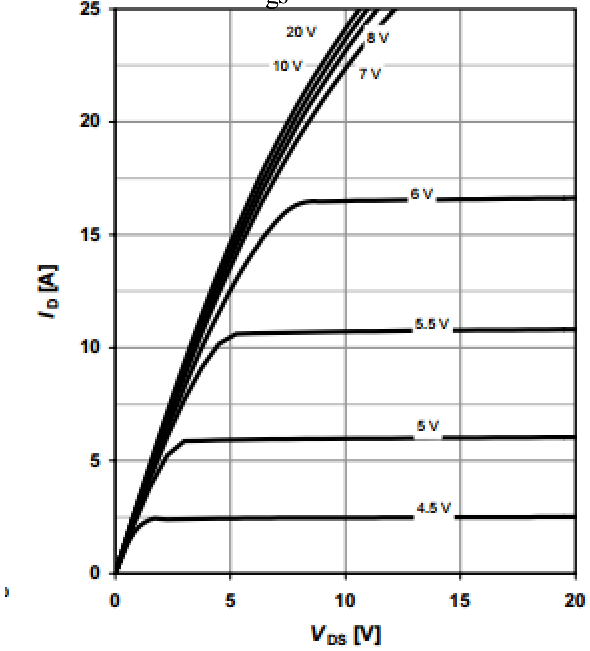






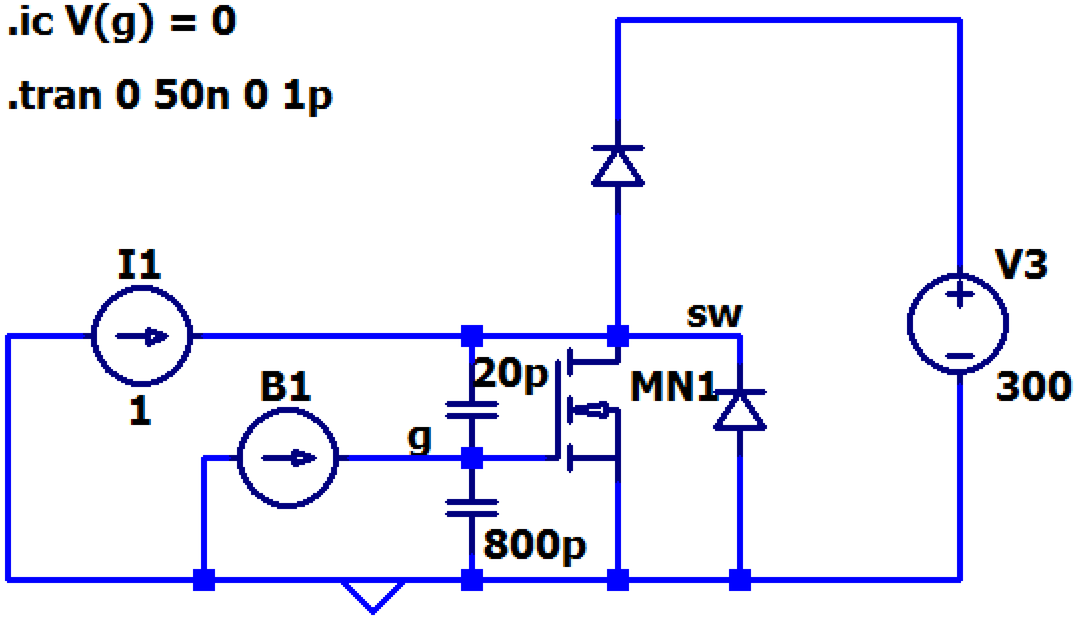
Device Transconductance





Example Simulation

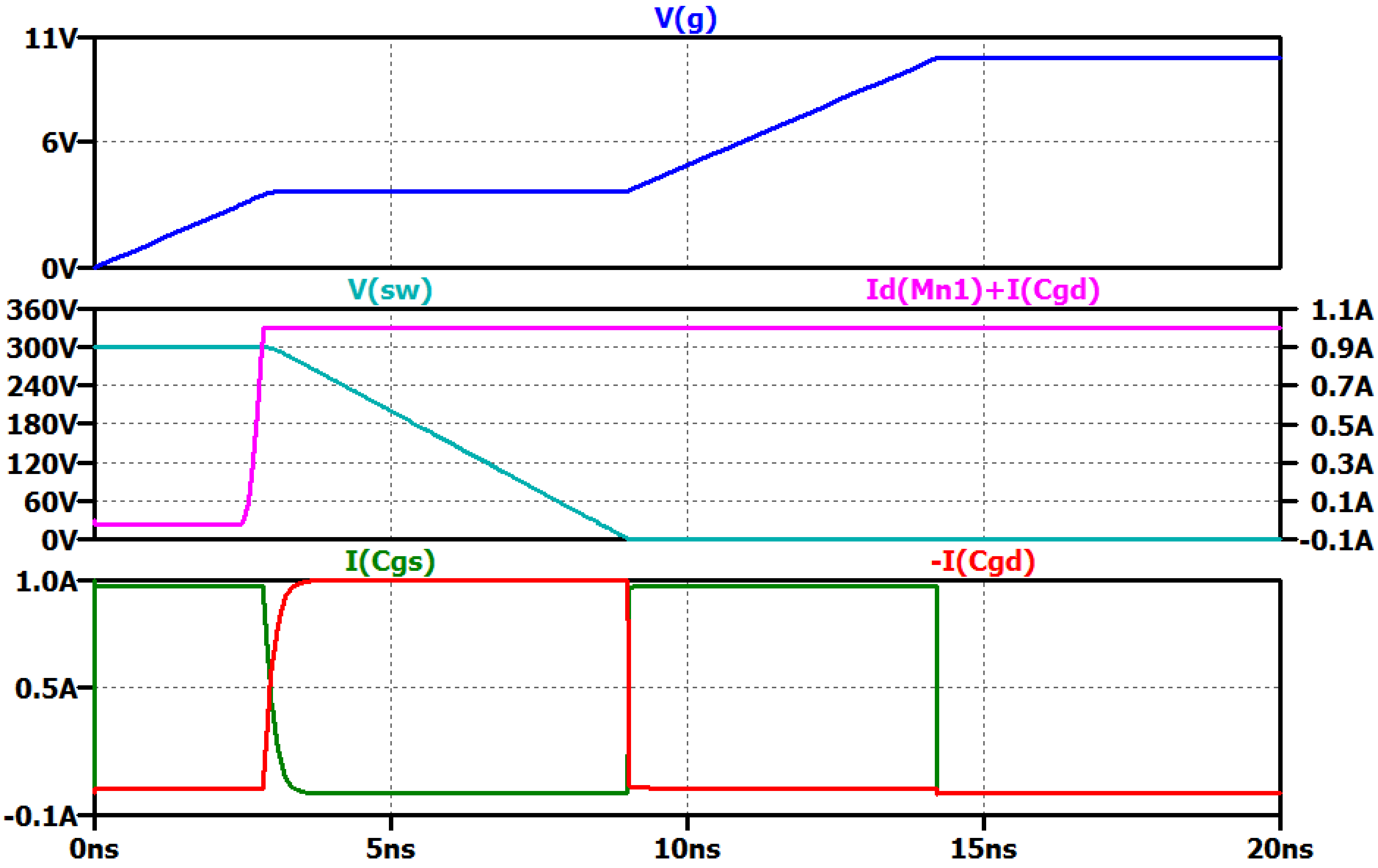
```
.ic V(g) = 0
.tran 0 50n 0 1p
```



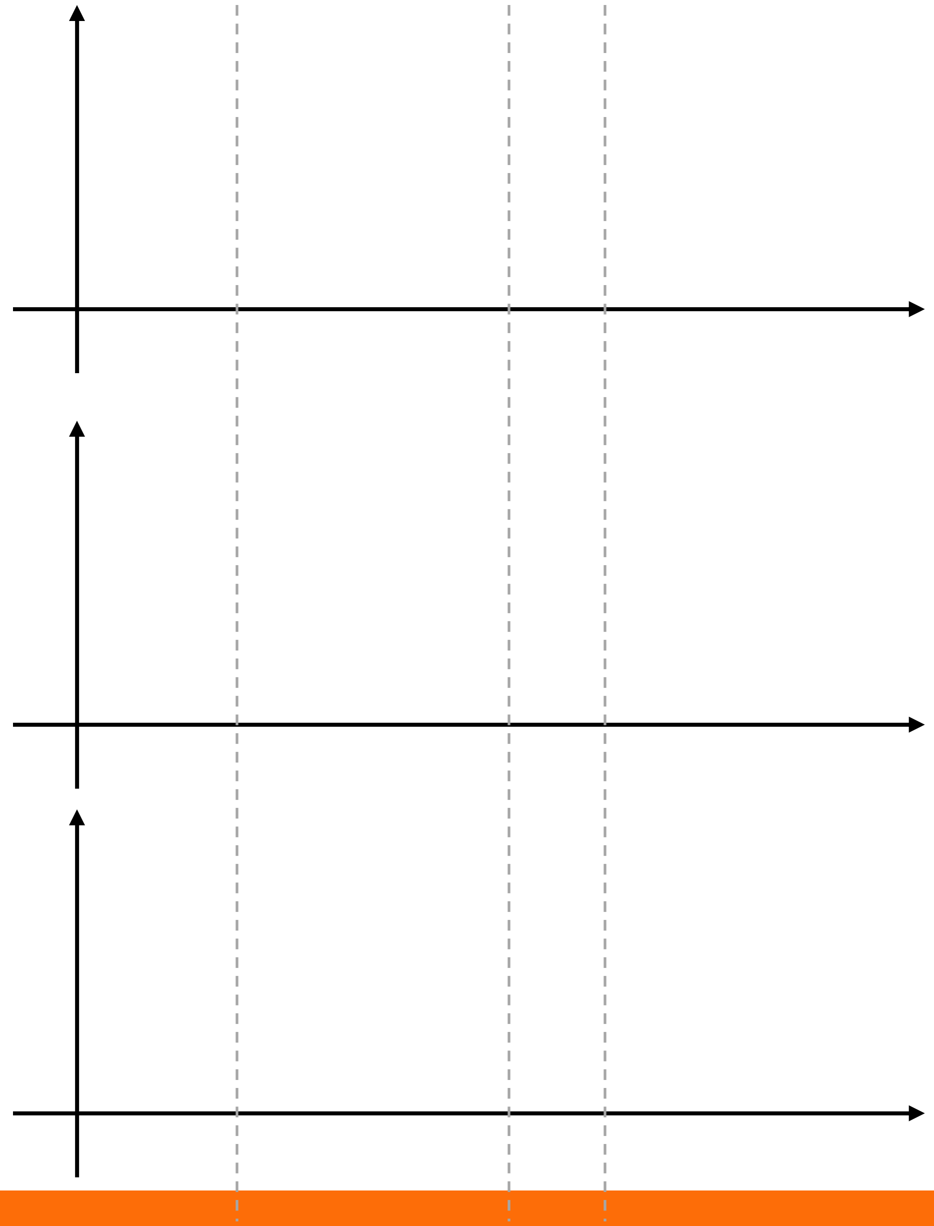
```
I=IF(V(g)<10,1,0)
```

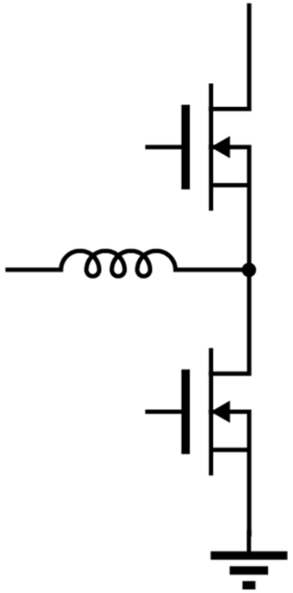
```
.model myD D(n=.01)
.model testFET VDMOS(Rg=.1 Rd=0 Rs=0 Vto=3 Kp=9 Cgdmax=0p
+ Cgdmin=0p Cgs=0p Cjo=1.5f Is=26p Rb=0m  Vds=600 Ron=385m Qg=0n)
```

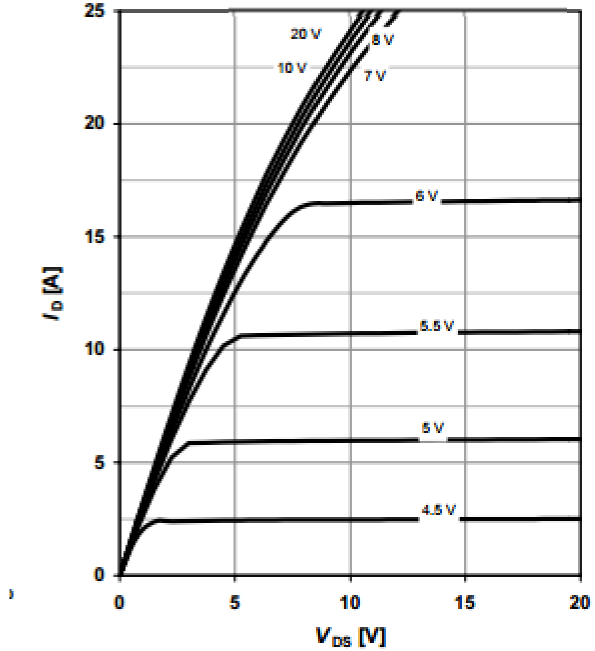
Simulation Waveforms – Turn On



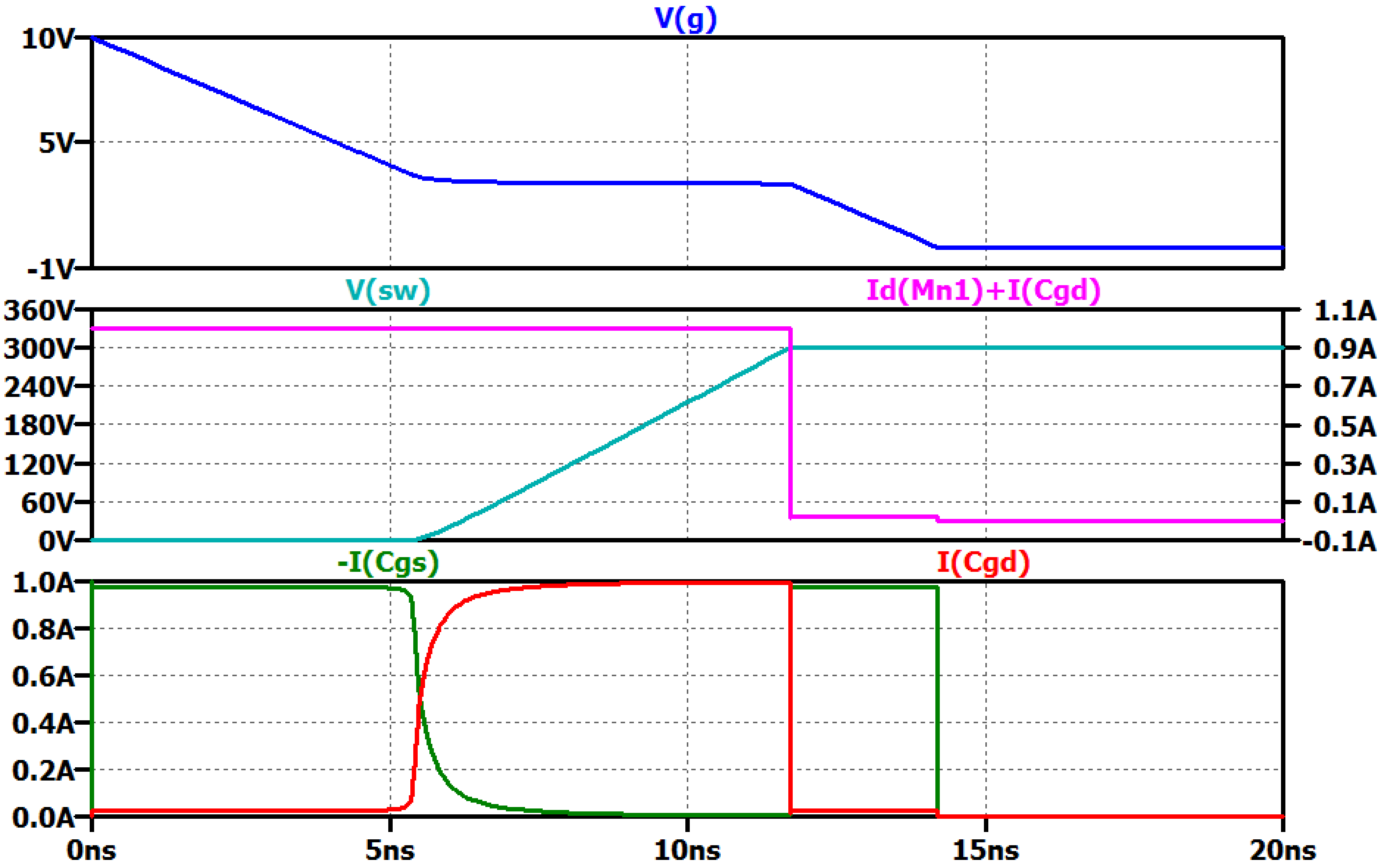
Turn-Off Transition



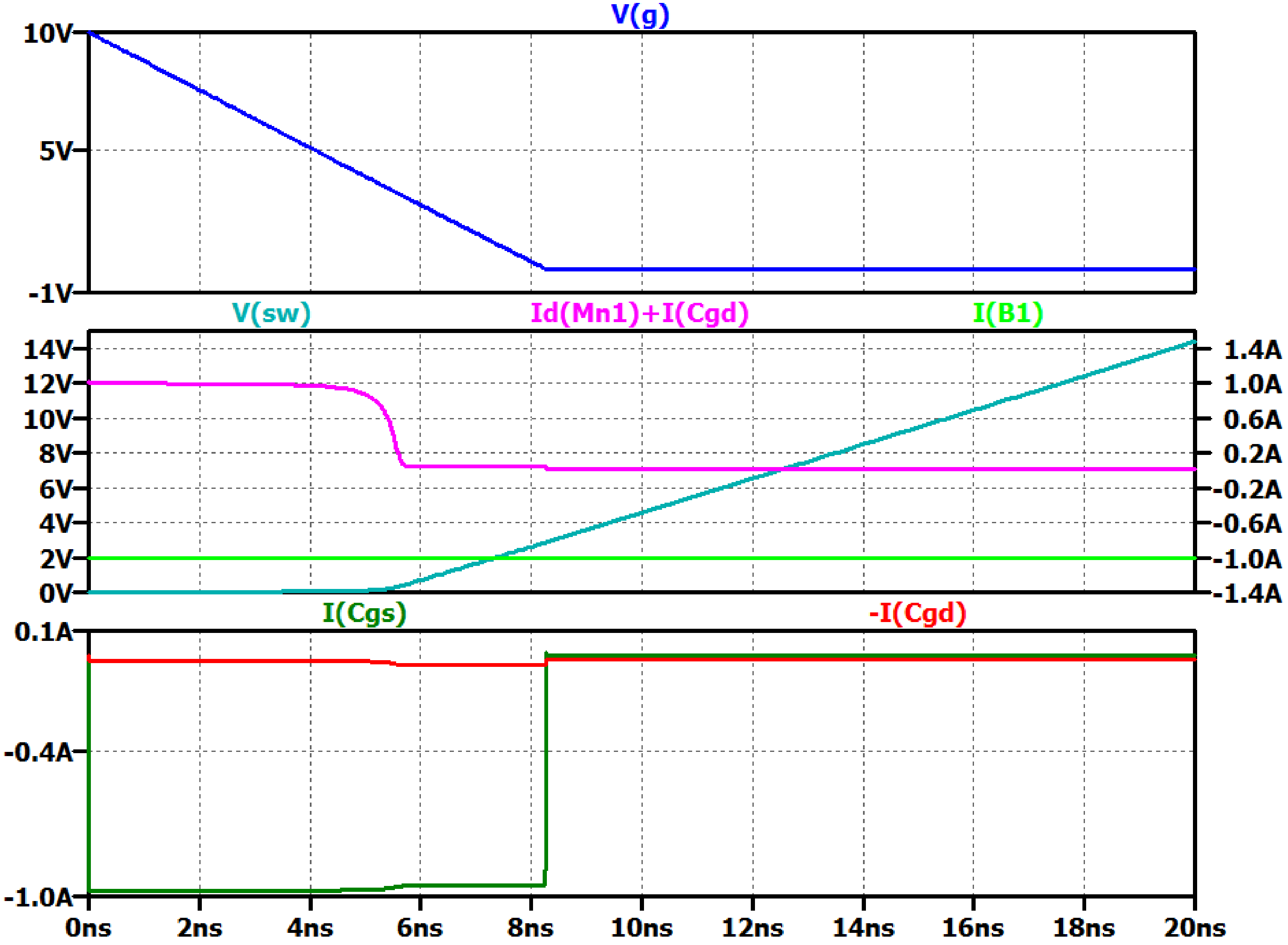




Turn-Off


V(g)
10V
5V
-1V
V(sw)
Id(Mn1)+I(Cgd)
360V
300V
240V
180V
120V
60V
0V
1.1A
0.9A
0.7A
0.5A
0.3A
0.1A
-0.1A
-I(Cgs)
I(Cgd)
1.0A
0.8A
0.6A
0.4A
0.2A
0.0A
0ns
5ns
10ns
15ns
20ns

Turn-Off (Drain Dominated)



Gate- vs. Drain-Limited Switching