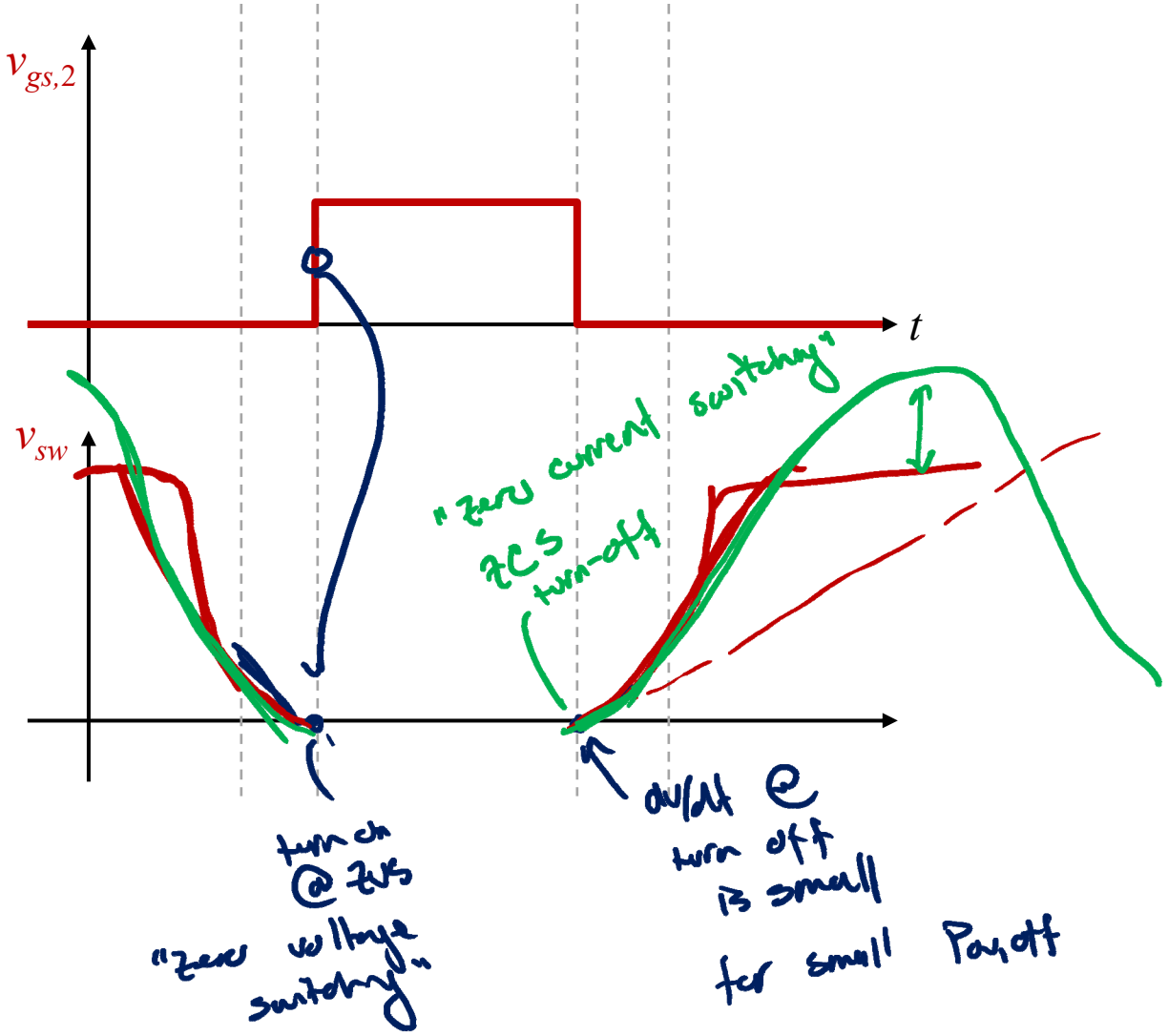
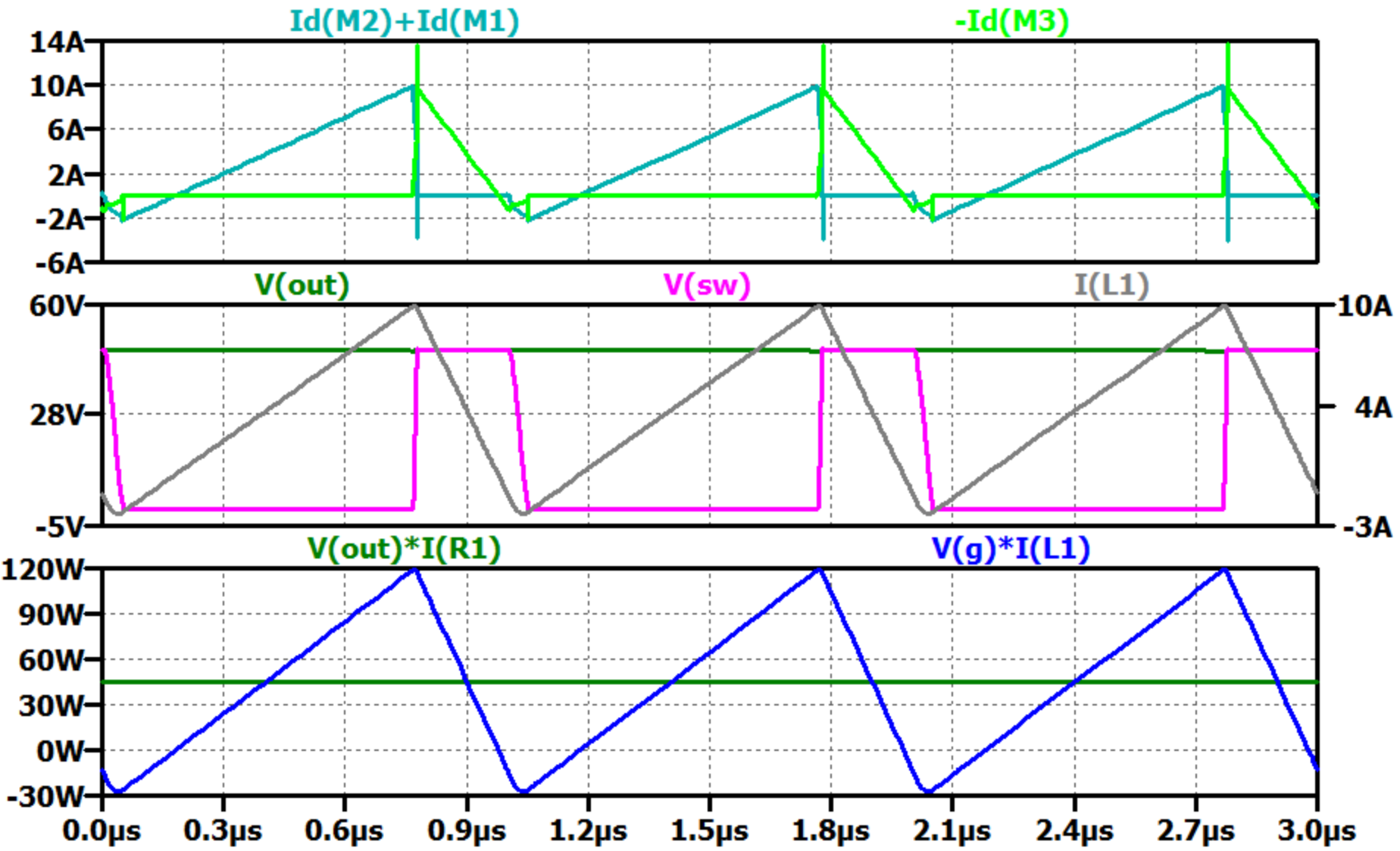
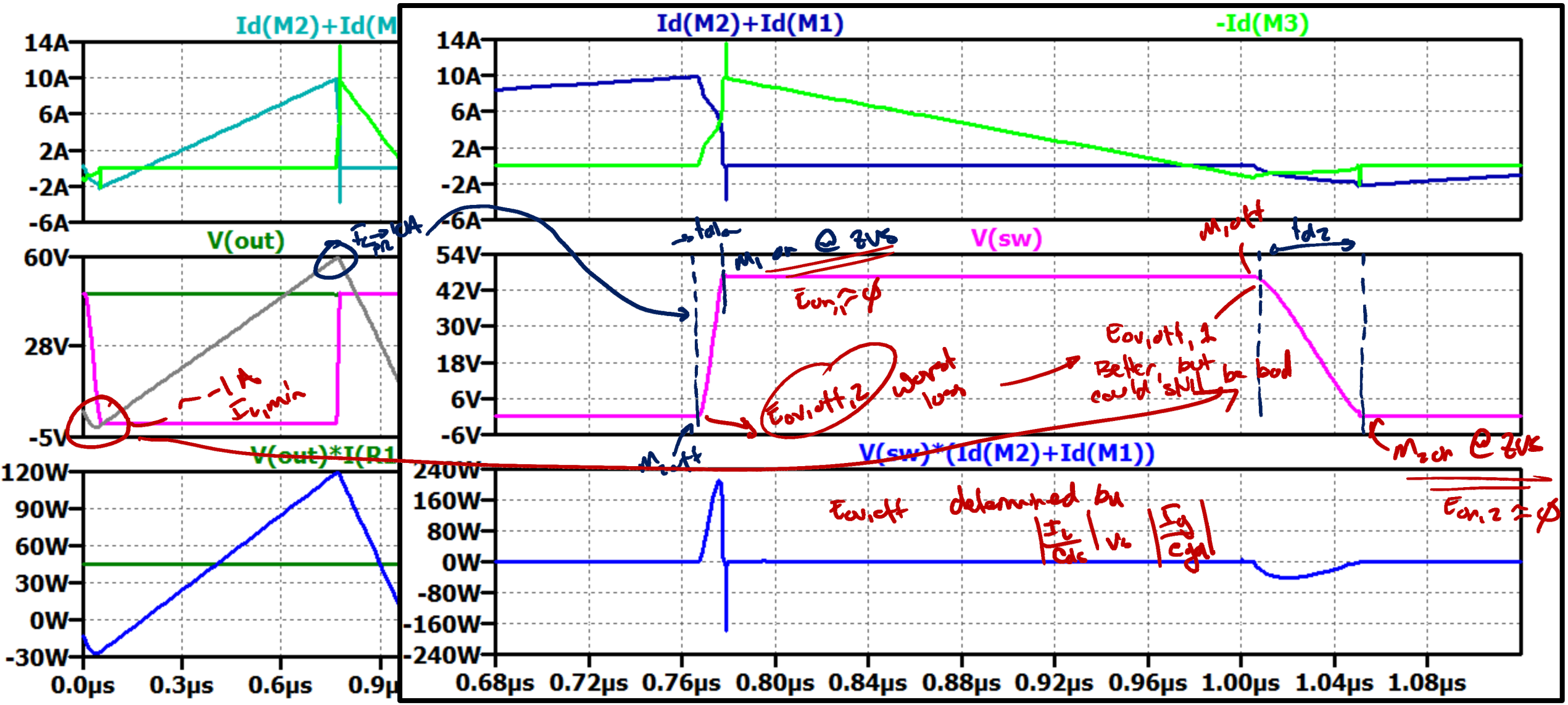
Ideal Switching Waveforms



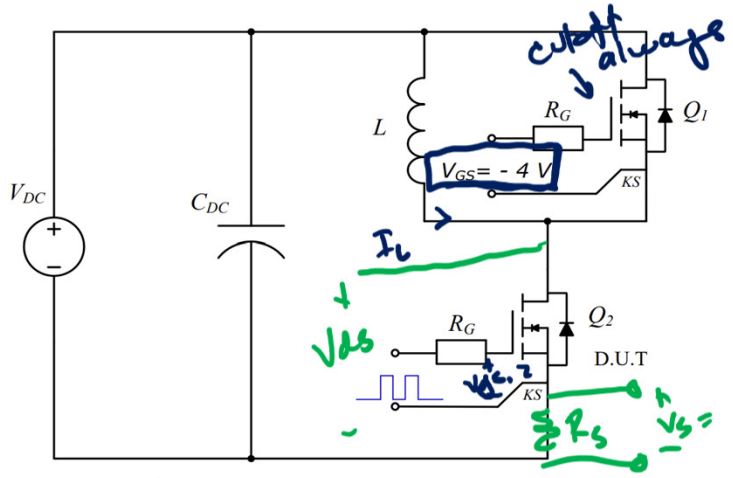
Synchronous Simulation (L3)

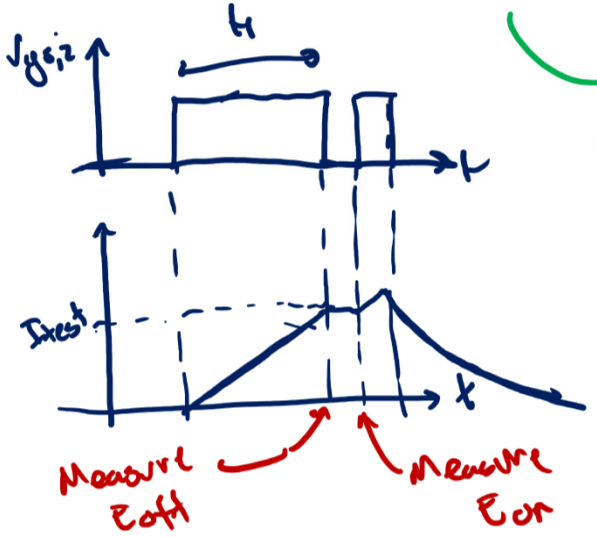


Synchronous Simulation (L3)



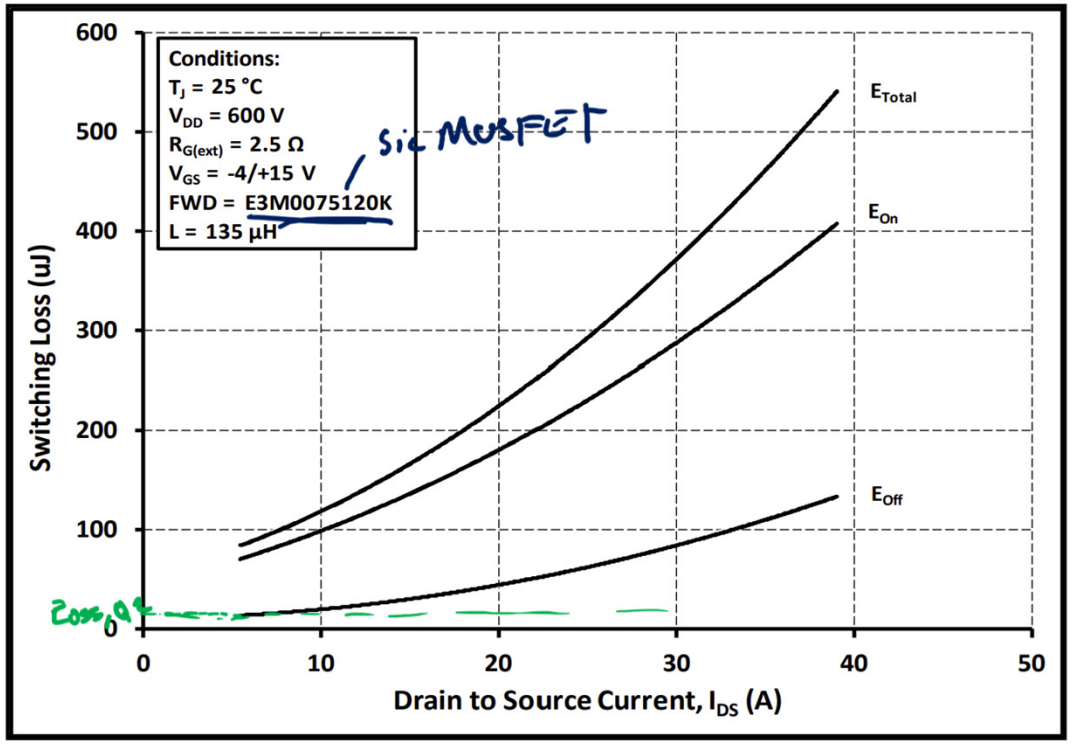
Double-Pulse Test





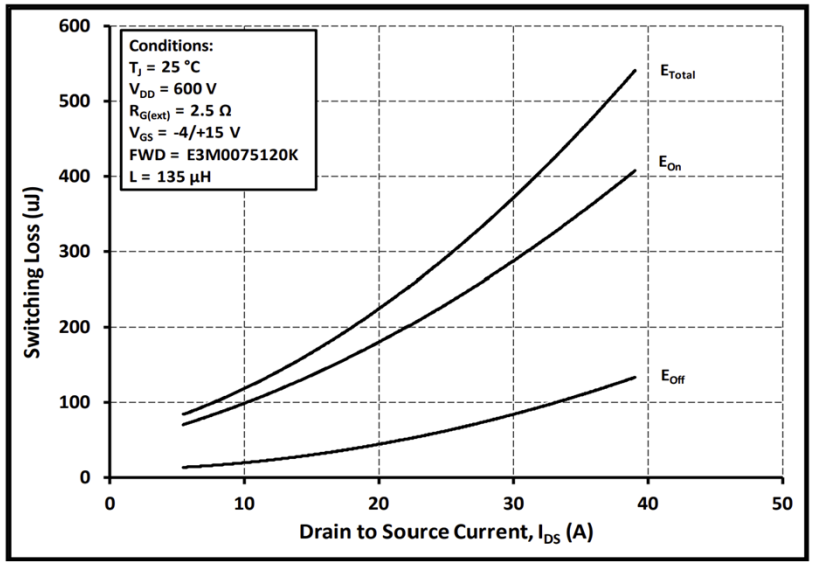
Both measurements wide BW, low noise, low parasitic, low skew

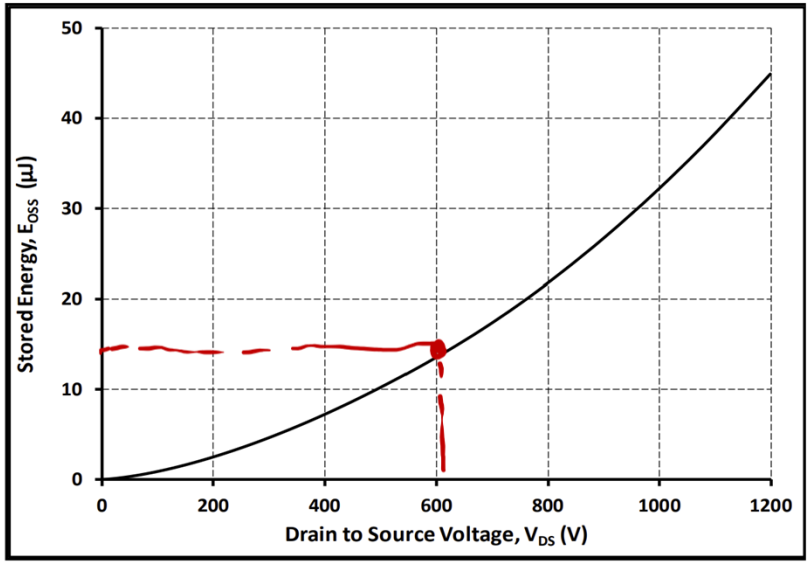
$$E_{off} = \int_{off} V_{ds} i_{ds}$$

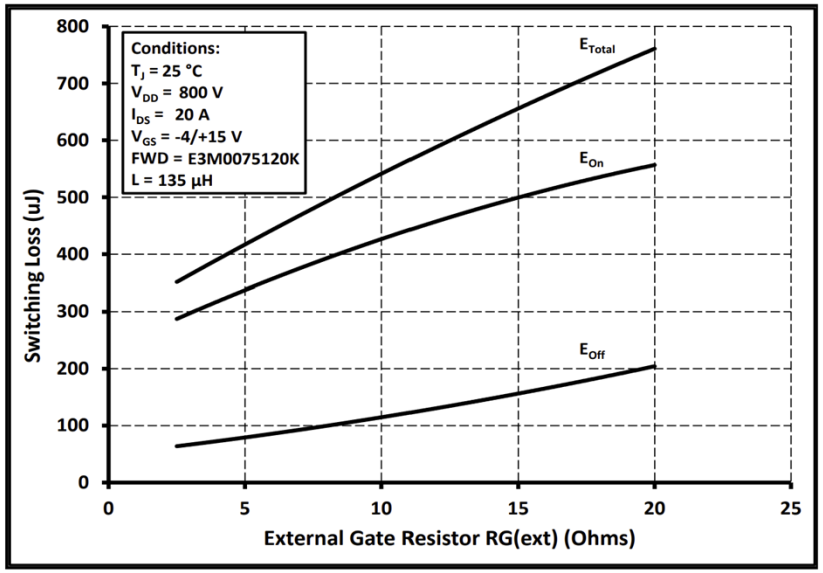


$E_{off} = E_{ov,off} + E_{oss,Q2}$

All measurements highly dependent on layout, gate drive implementation, devices, switching scheme, etc.

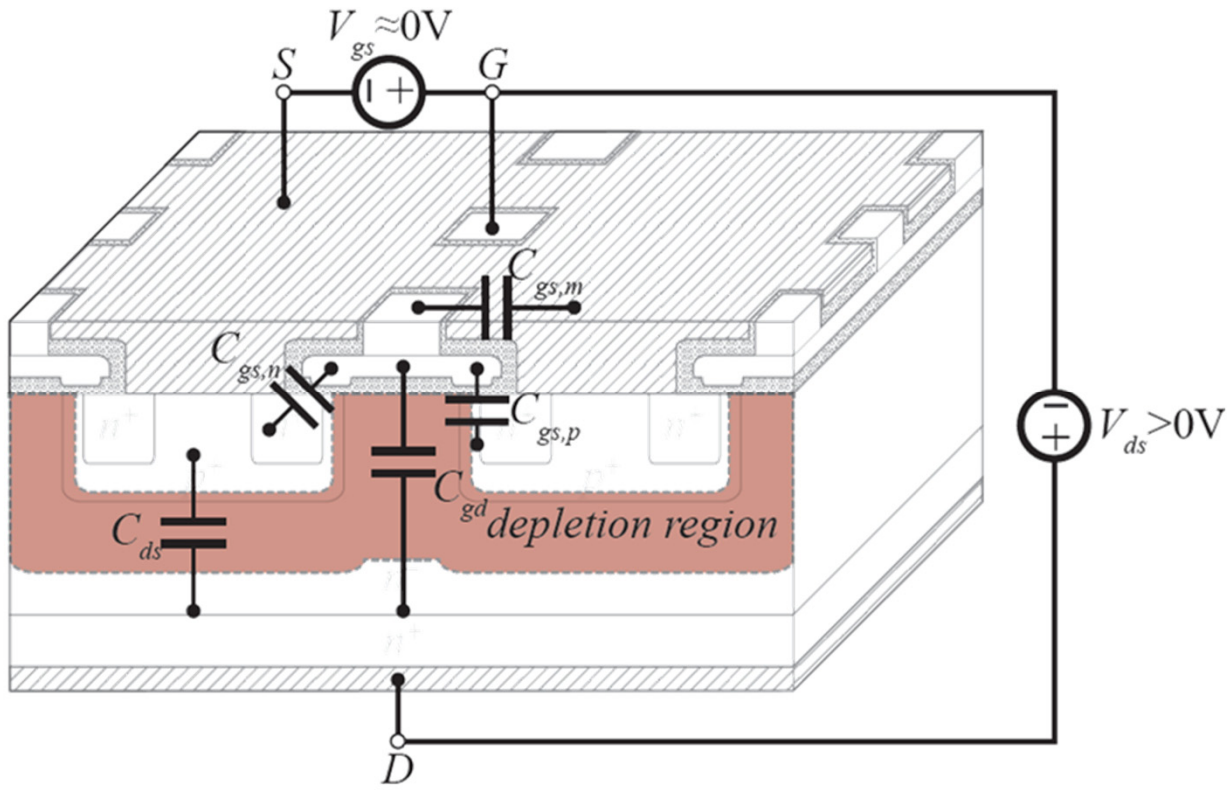

Conditions:
T_J = 25 °C
V_{DD} = 600 V
$R_{G(ext)}$ = 2.5 Ω
V_{GS} = -4/+15 V
FWD = E3M0075120K
L = 135 µH
E_{Total}
E_{On}
E_{Off}
Switching Loss (uJ)
Drain to Source Current, I_{DS} (A)
0
100
200
300
400
500
600
0
10
20
30
40
50


Stored Energy, E_{OSS} (µJ)
Drain to Source Voltage, V_{DS} (V)
0
10
20
30
40
50
0
200
400
600
800
1000
1200

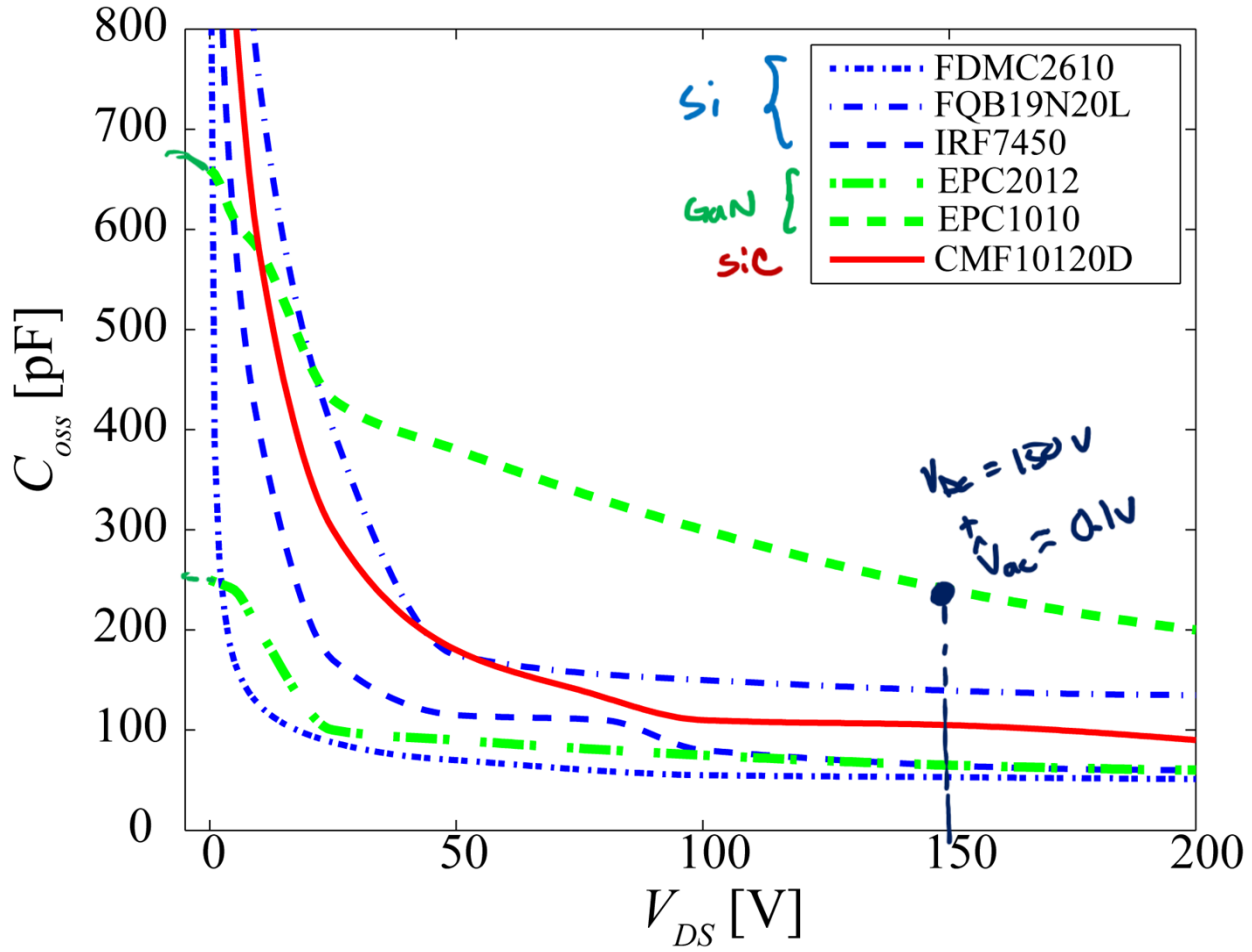

Conditions:
T_J = 25 °C
V_{DD} = 800 V
I_{DS} = 20 A
V_{GS} = -4/+15 V
FWD = E3M0075120K
L = 135 µH
E_{Total}
E_{On}
E_{Off}
Switching Loss (uJ)
External Gate Resistor RG(ext) (Ohms)
0
100
200
300
400
500
600
700
800
0
5
10
15
20
25

Capacitive switching loss

ANALYSIS OF NONLINEAR CAPACITANCES


$V_{gs} \approx 0V$
S
G
$C_{gs,m}$
$C_{gs,n}$
$C_{gs,p}$
C_{gd}
depletion region
C_{ds}
$V_{ds} > 0V$
D

Example Device C_{oss}



Coss is a small-signal measurement

$$\hat{i}_c = C_{oss}(V_{DC}) \frac{d\hat{v}_{ds}}{dt}$$

$$\Delta q_c = C_{oss}(V_{DC}) \Delta V_{DC}$$

$$Q \neq C_{oss}(V_{DC}) V_{DC}$$

we care, exclusively, about large-signal behaviors.

Analytical model used in e.g. Spice

$$C_{ds} = \frac{C_{jo}}{\left(1 + \frac{V_{ds}}{V_{jo}}\right)^m}, \text{ commonly } m = \frac{1}{2}$$

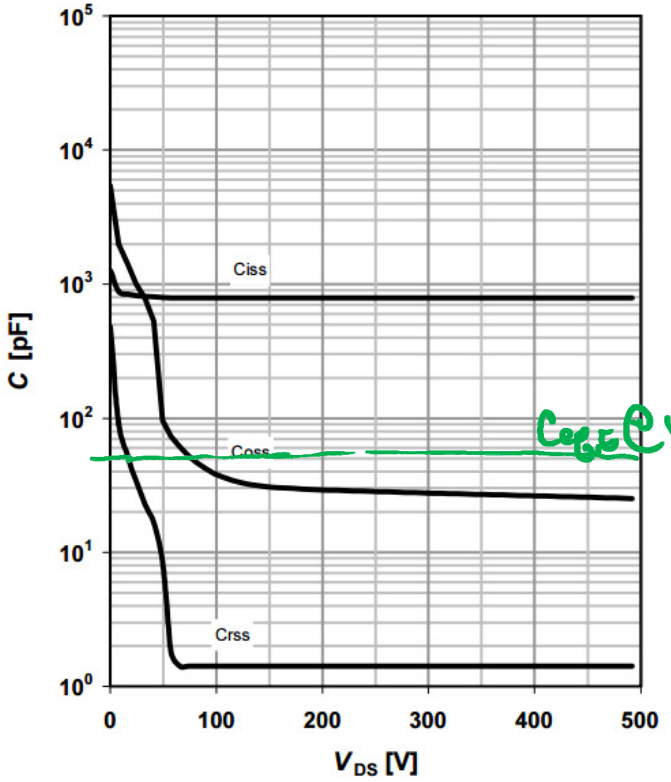
↓

not a good fit for a variety of power FETs

Datasheet Reported Capacitance

13 Typ. capacitances

$C = f(V_{DS})$; V_{GS}=0 V; f=1 MHz



14 Typ. Coss stored energy

$E_{oss} = f(V_{DS})$