ECE692

Comparison of Switched Capacitor Step-Down Converters

In this problem, you will compare five different converters for application as a 48-to-6 V step-down application. The five topologies and their modulation schemes are shown on the following page. Each topology, with the depicted modulation scheme, operates as an unregulated converter with a native conversion ratio near 8:1.

To ensure a uniform comparison, the following parameters are held constant across all devices in all topologies.

C_{ds}	r_{on}	C_x	C_o	C_x ESR	L	L ESR	f_s	I_{load}	V_g
710 pF	4 mΩ	2 µF	10 µF	4 mΩ	500 nH	4 mΩ	1 MHz	5 A	48 V

C_x is any capacitor shown in the schematics on the following page other than the output capacitance C_o. All Cx capacitors and all inductors have equivalent series resistances (ESRs) which should be included in the circuit model. All MOSFETs should be modeled with the above r_{on} and C_{ds} (not shown in schematics). Modulation waveforms are as shown, and all switching occurs with zero dead time.

The input source V_g can be modeled with a 1 mΩ series resistance.

Two of the topologies, the Hybrid Dickson Converter and Dual Inductor Hybrid have a variable modulation duty cycle D. In both, you should find the value for D which results in the highest efficiency of the converter. No additional approximations should be applied in your calculations.

Use PLECS to generate state space descriptions of each topology. Additional information on PLECS is available on the materials page of the course website.

a) Develop a single MATLAB function which can solve steady-state and return the efficiency and average output voltage for any of the topologies,

```
[eff, Vout] = your_function(ModelPath, ti, swVec)
```

Where `ModelPath` is the path to the PLECs model of the circuit, `ti` is a vector of k subinterval durations (in seconds) and `swVec` is a k-by-n_{sw} binary vector of switching states for each MOSFET.

b) For each of the Hybrid Dickson Converter and Dual Inductor Hybrid Converter, find the Duty Cycle D which maximizes efficiency.

c) For each of the five topologies, plot and submit waveforms of all capacitor voltages (excluding C_{ds}) and inductor currents over one period.

d) Submit a table of efficiencies and output voltages for each topology. Which topology has the highest efficiency? What additional characteristics of these topologies should be considered if implementing in a real application?

Dickson	Inductively Loaded Dickson	Hybrid Dickson	Dual Inductor	Dual Inductor Hybrid