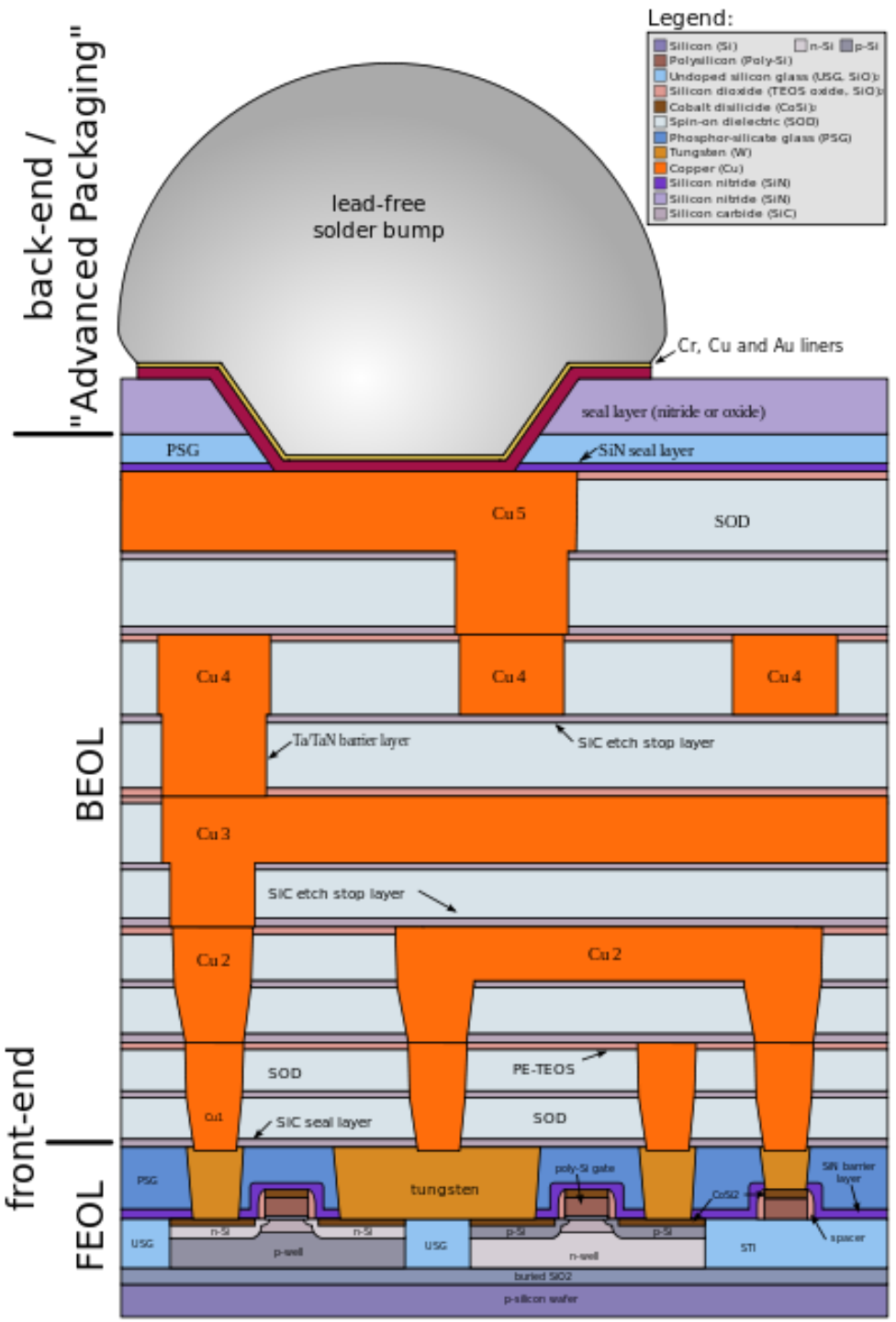
Schematic profile of “modern” IC

BEOL (metalization layer)
& FEOL (devices)

Isolation between devices:

Undoped Silicate Glass (USG)
shallow trench isolation (STI)

https://en.wikipedia.org/wiki/Back_end_of_line



Schematic profile of legacy IC

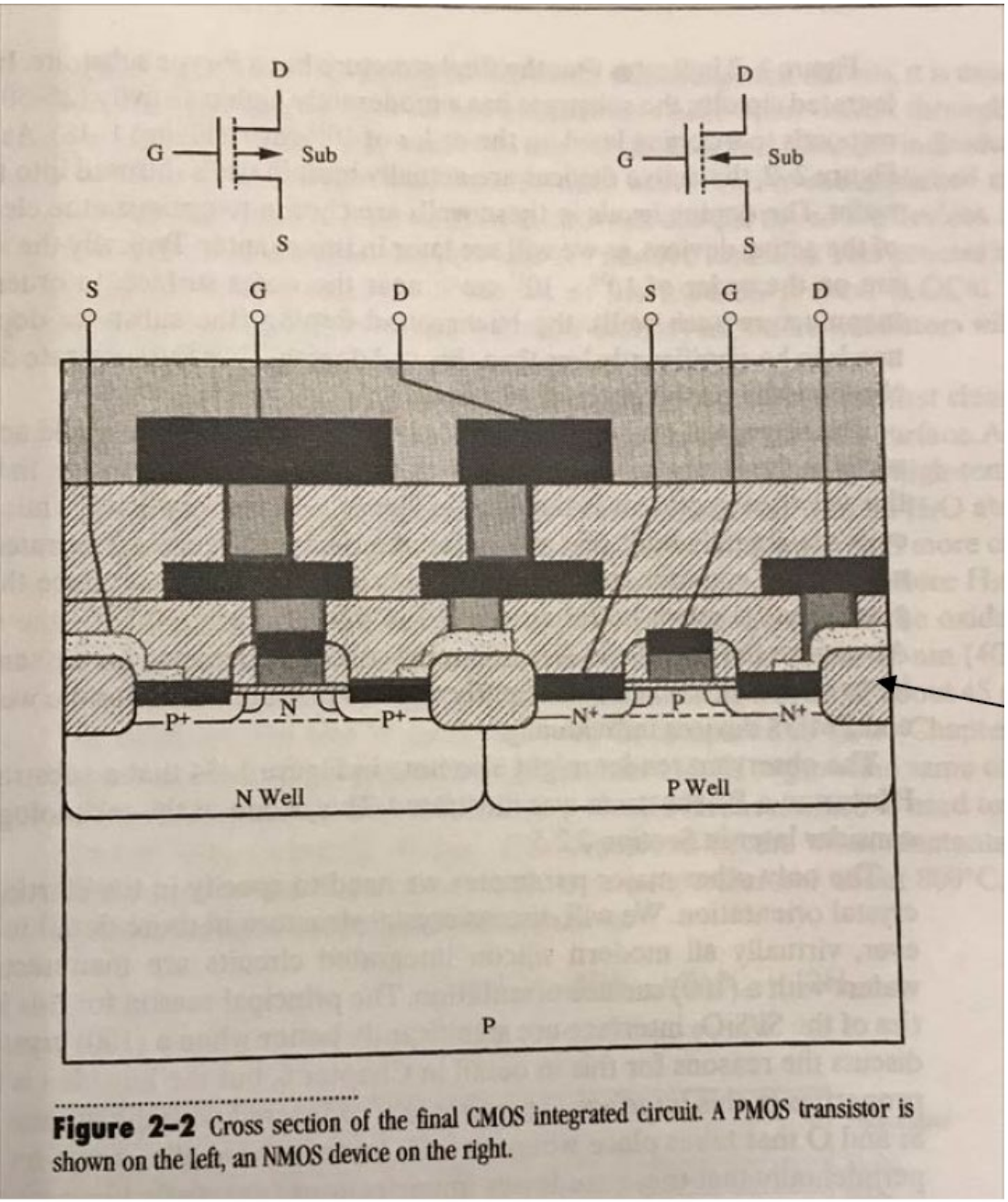


Figure 2–2 Cross section of the final CMOS integrated circuit. A PMOS transistor is shown on the left, an NMOS device on the right.

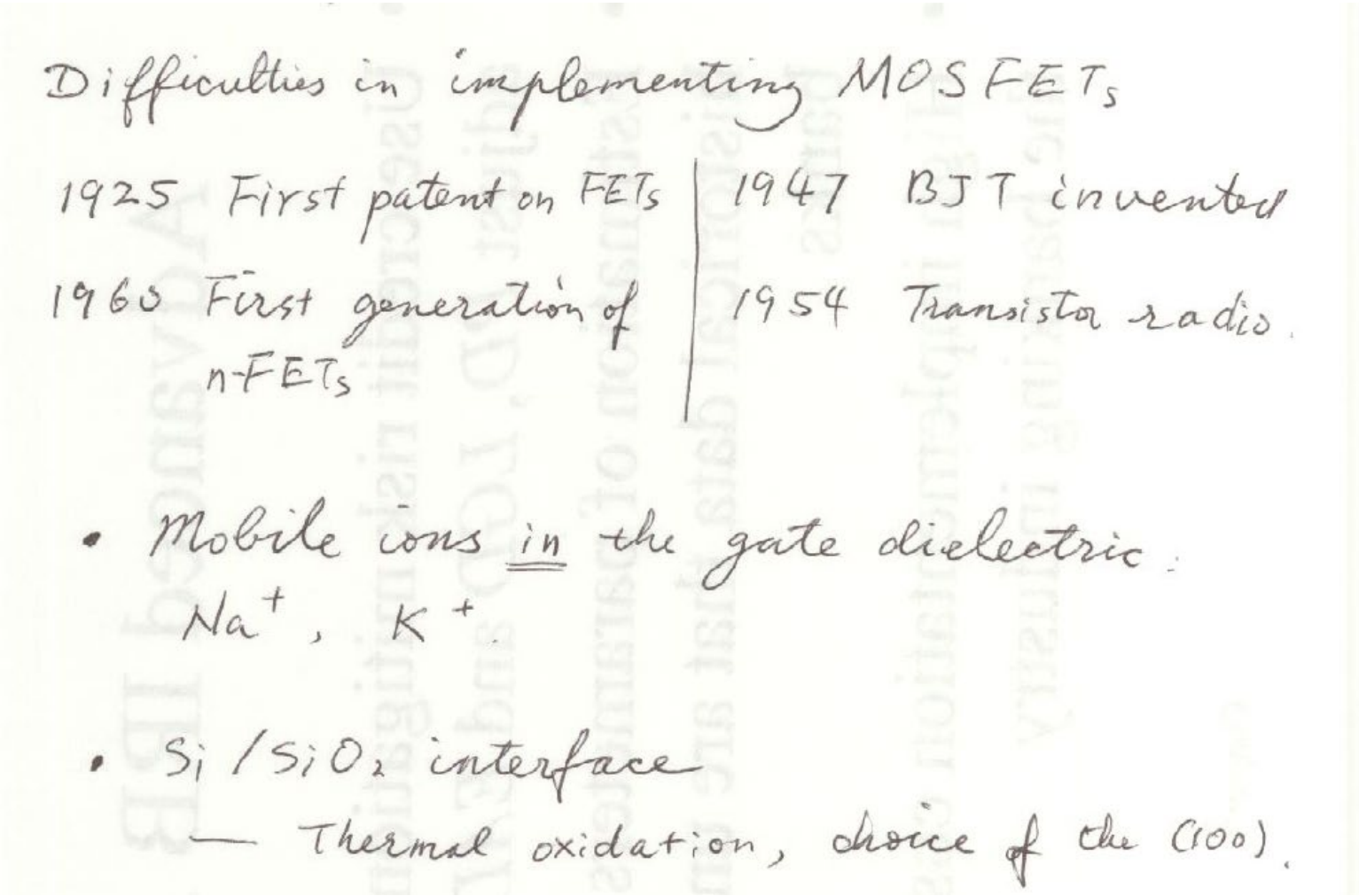
Field oxide or LOCOS (local oxidation of Si)

This figure and many others in this lecture note are adapted from Plummer, Deal, & Griffin, *Silicon VLSI Technology*

Processing

Watch video Silicon Run I: https://ut.kanopy.com/video/silicon-run-i (log in with your UTK NetID)

Reference book: Plummer, Deal, & Griffin, *Silicon VLSI Technology.*
A bit old, but good for understanding basic principles. References on more advanced processes will be listed.



Contaminations:

- Mobile ions: Na^+, K^+.
  source: us!
- Particles: Plenty in air!
  We emit!
- Metals: Fe, Cu, Au, etc.
  why are they bad? What about Cu interconnects?
- Organic residues (photoresist residue)

Deep-level impurities

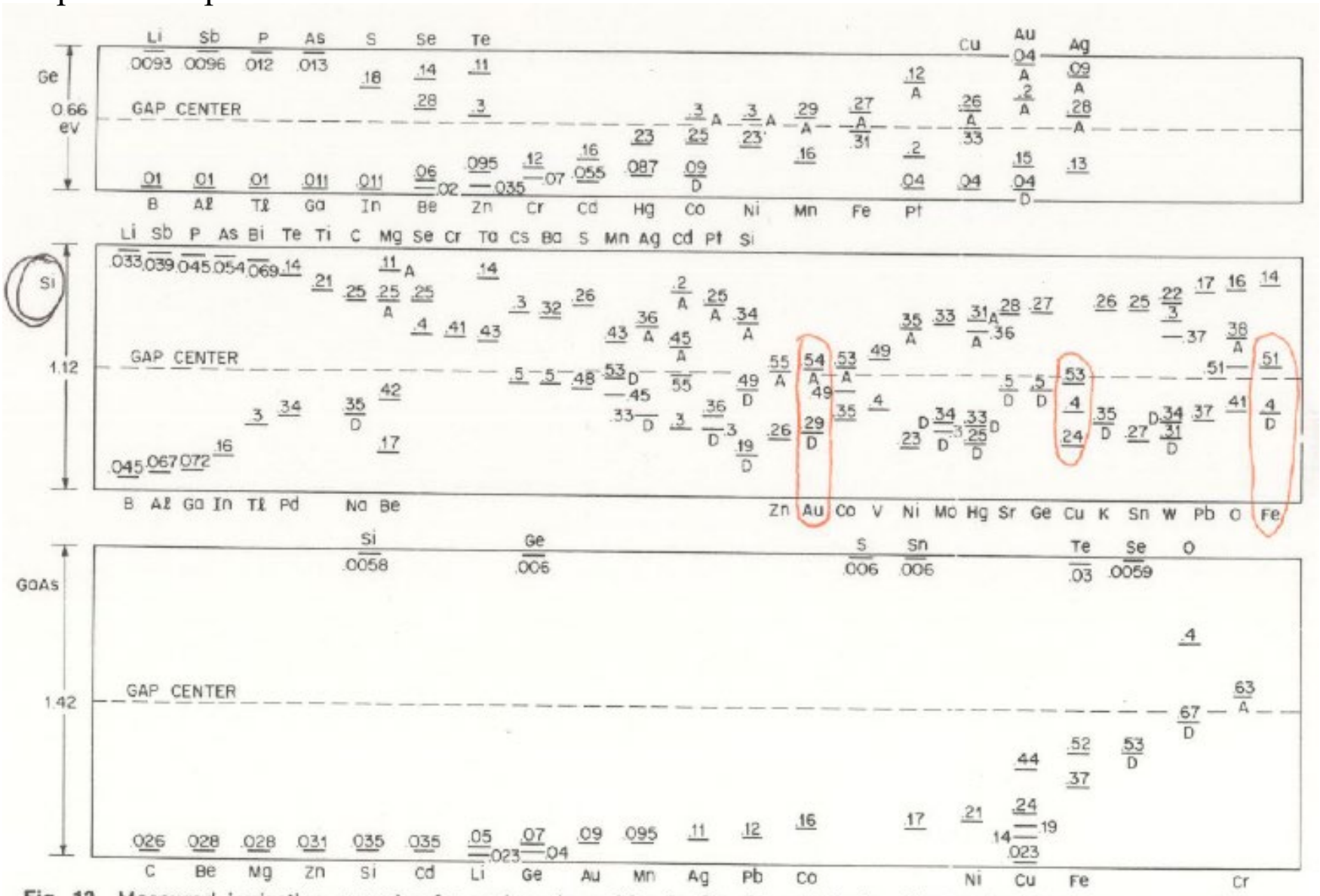


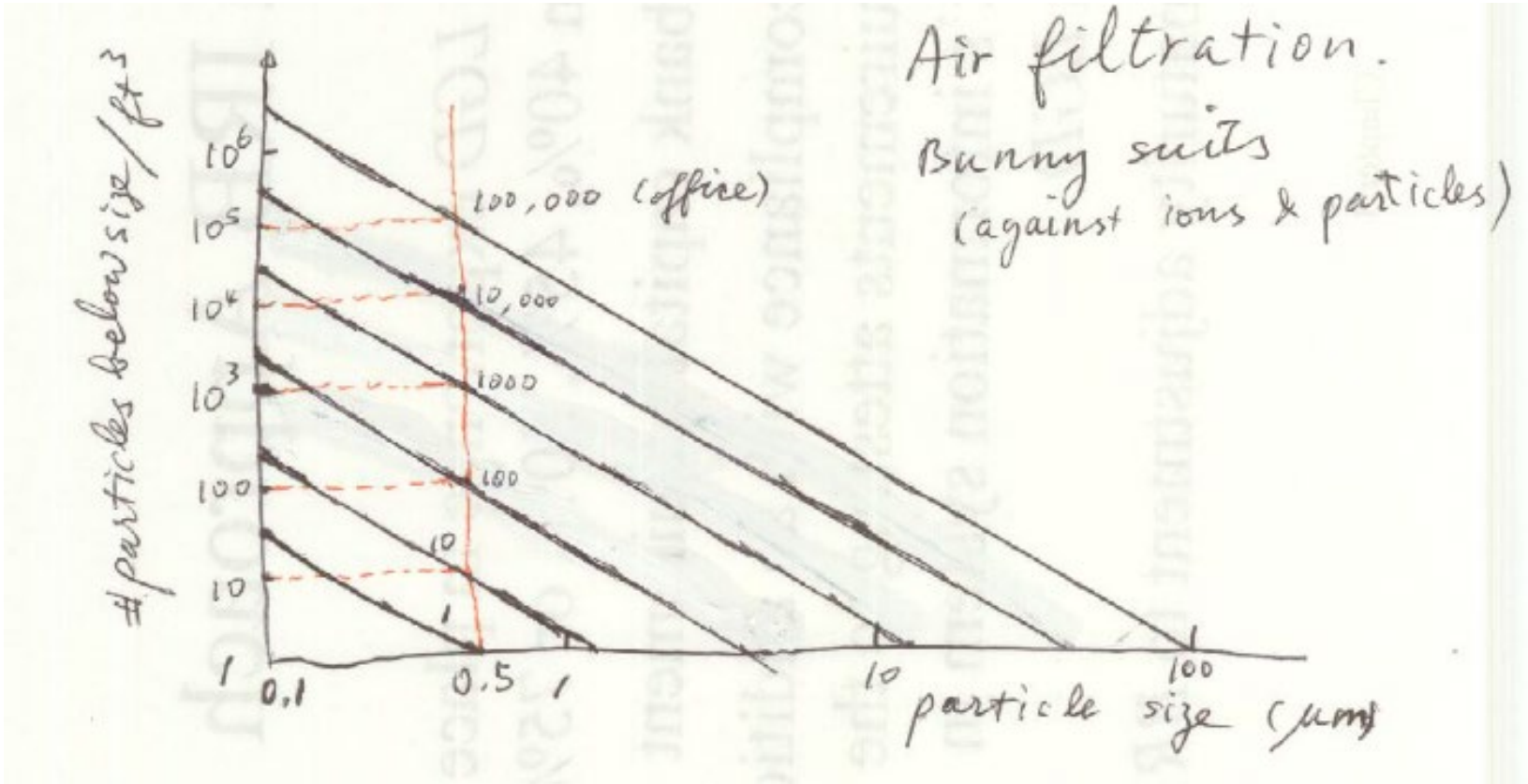
Fig. 13 Measured ionization energies for various impurities in Ge, Si, and GaAs. The levels below the gap centers are measured from the top of the valence band and are acceptor levels unless indicated by D for donor level. The levels above the gap centers are measured from the bottom of the conduction-band level and are donor levels unless indicated by A for acceptor level. The bandgaps at 300 K are 0.66, 1.12, and 1.42 eV for Ge, Si, and GaAs, respectively. (After Conwell, Ref. 27; Sze and Irvin, Ref. 28; Milnes, Ref. 24.)

From Sze

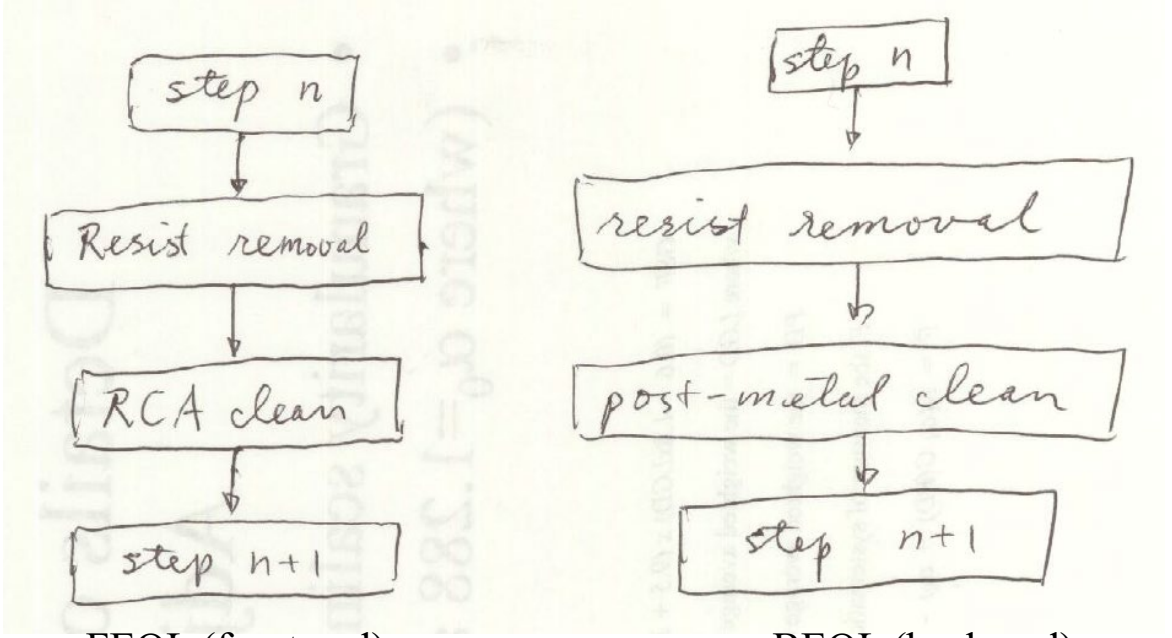
3 tiers of defense against contamination

1. Clean factory
2. Wafer cleaning
3. Gettering

Classes of cleanrooms



Wafer cleaning



FEOL (front end)

BEOL (back end)

RCA clean

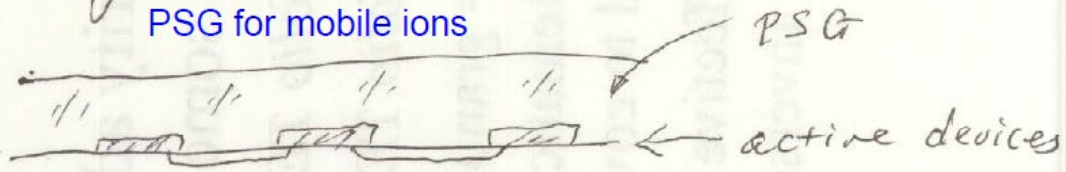
a series of cleaning steps involving acids & H_2O_2, NH_4OH, including the famous SC-1 & SC-2.

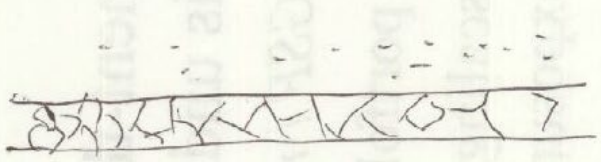
- oxidizes organics
- complexes metals
- Etches SiO_2 but simultaneously oxidizes Si, → remove surface particles

Post-metal clean:
Not as effective, but requirement relaxed.

○ Gettering

PSG for mobile ions





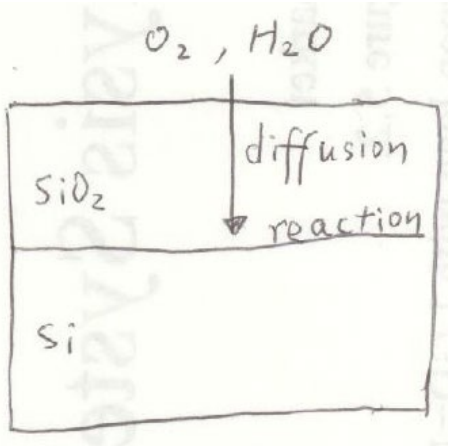
Si with defects (far away from active devices) for transition metals

- PSG (phosphosilicate glass, $SiO_2 : P_2O_5$)
  complexes mobile ions (K^+, Na^+).
  Mobile ions are, of course, mobile!
- Metal atoms diffuse faster than intentional dopants (B, P, As, etc)
- Trapped by defects.

The choice of the (100) surface

- The (100) surface has the lowest Si atom density; the (111) has the highest
  [Therefore (100) oxidizes the slowest.]
- The Si(100)/SiO_2 interface has the lowest surface state density (defects associated w/ dangling bonds).
- Historically, (111) was used for bipolar technologies, due to relative ease of growth.

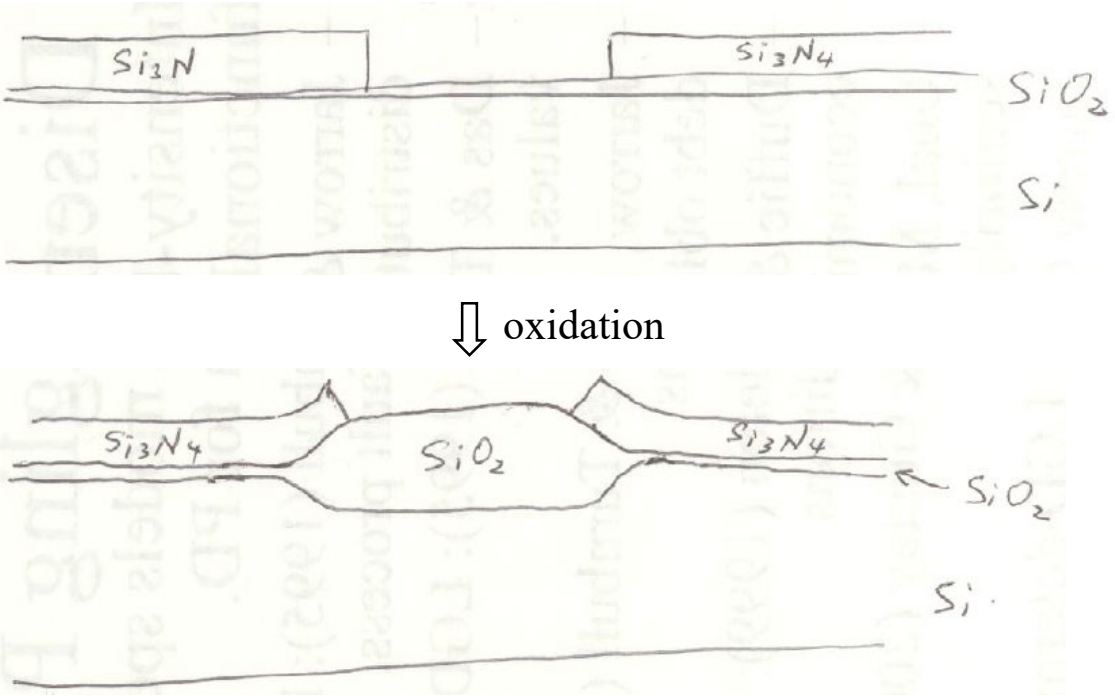
Si oxidation: the big picture

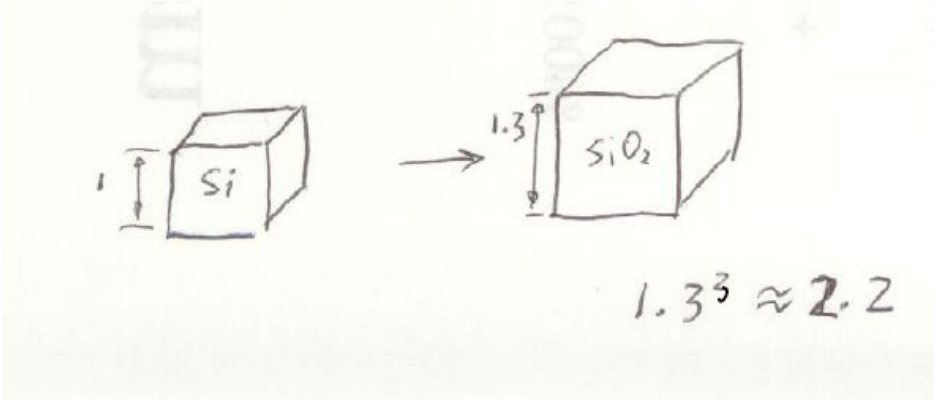


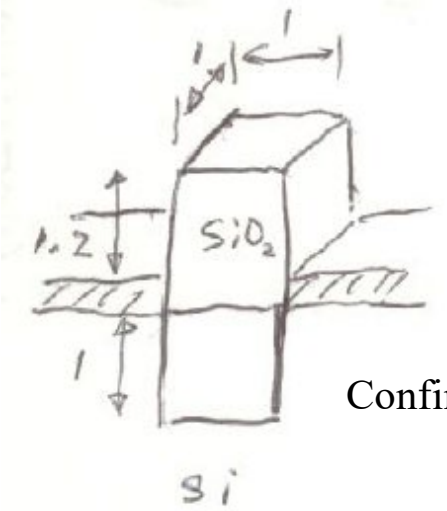
$Si + O_2 \rightarrow SiO_2$

$Si + 2H_2O \rightarrow SiO_2 + 2H_2$

Example: LOCOS (local oxidation of Si) for field oxide

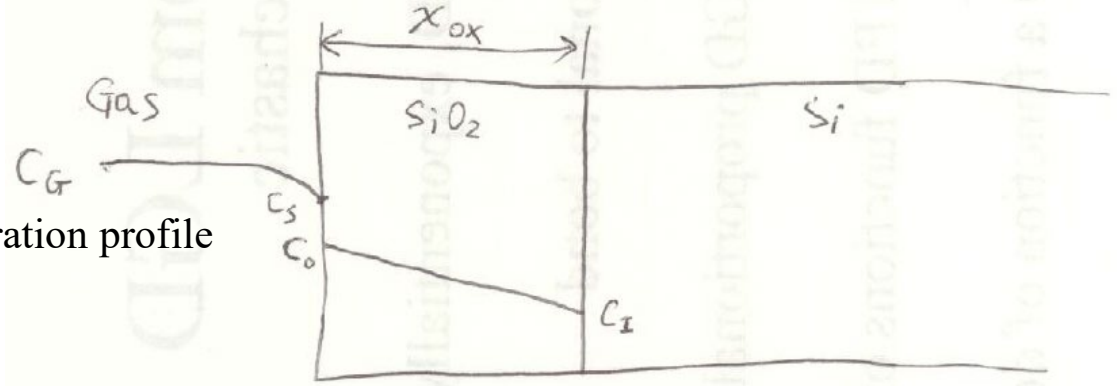






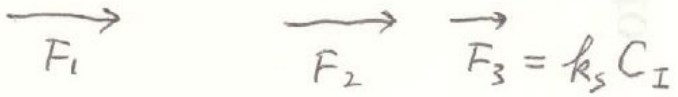
Confined growth

Oxidation Kinetics



Concentration profile

Flows



$$F_1 = F_2 = F_3 \quad \Rightarrow \quad x_{ox} = \frac{A}{2}\left[\sqrt{1 + \frac{t+\tau}{A^2/4B}} - 1\right]$$

t : time

τ : If $x_{ox}(0) \equiv x_i \neq 0$, τ is the time to generate x_i under the same conditions (as if the process started τ earlier)

$$\tau = \frac{x_i^2 + A x_i}{B}$$

- What are the dimensions (units) of A & B?

$$x_{ox} = \frac{A}{2}\left[\sqrt{1 + \frac{t+\tau}{A^2/4B}} - 1\right]$$

For small $t+\tau$ (i.e. initial stage,

$\frac{t+\tau}{A^2/4B} \ll 1$):

$x_{ox} \cong \frac{B}{A}(t+\tau)$. — linear

For large $t+\tau$,

$x_{ox} = \sqrt{B(t+\tau)}$ — parabolic

Example: $\tau = 0$

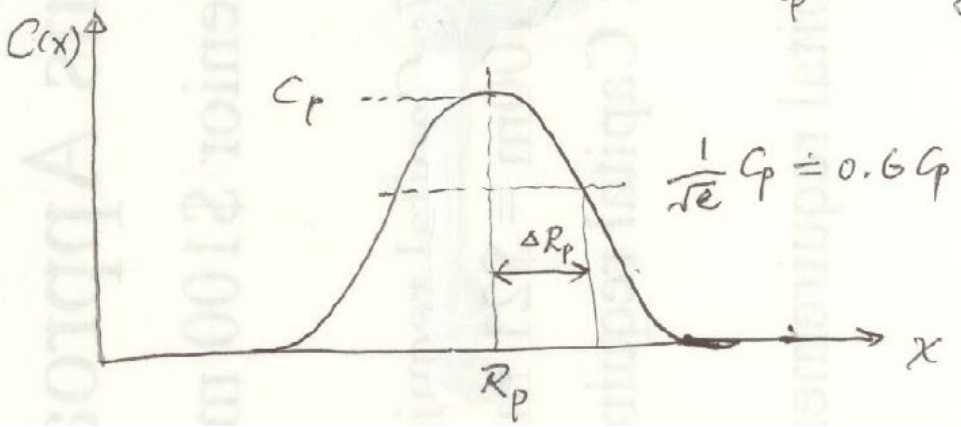
Introduce dopants to Si: ion implantation & dopant diffusion

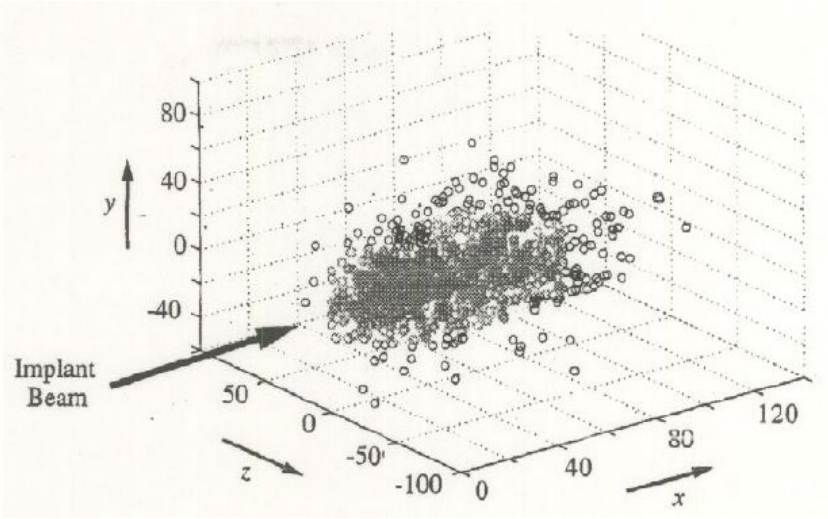
Ion implantation: precise control of dose and energy.

But, where the ion ends up is random

$$C(x) = C_p\, e^{-\frac{(x-R_p)^2}{2\Delta R_p^2}}$$

R_p: range



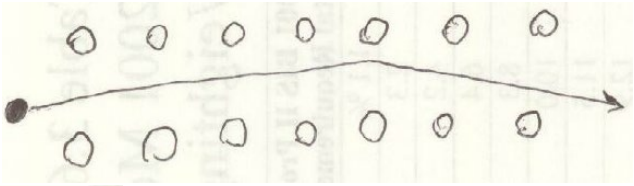


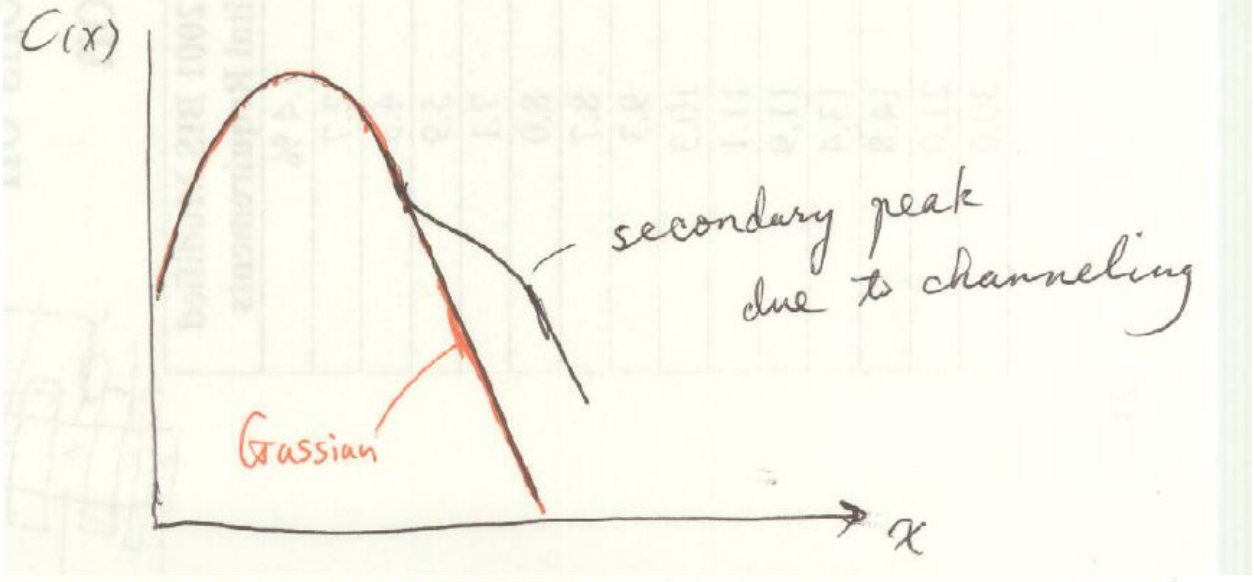
Total dose

$$Q = \int_{-\infty}^{+\infty} C(x)\,dx = \sqrt{2\pi}\,\Delta R_p\, C_p$$

Channeling

At low incident angles an ion can channel through between crystalline planes

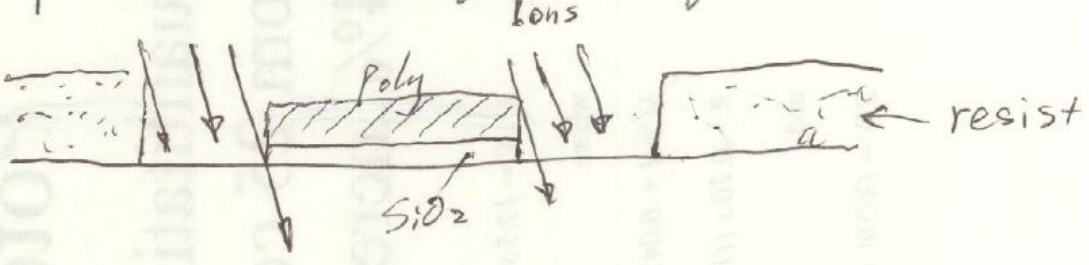




To avoid channeling:

- Use a thin SiO_2 "screening" layer
- Implant at an angle (e.g. 7°)

⇒ S/D asymmetry of FETs



As implanted, dopants are not electrically active yet. Activation: by annealing, dopants occupy substitutional sites.

The diffusion step repairs damages caused by implantation, activates dopants, and re-distributes dopants.

Description of diffusion

A gradient in concentration causes a flow — diffusion

The flow: $F = -D\frac{\partial C}{\partial x}$ (C: concentration; D: diffusivity)

$$\frac{\partial C}{\partial t} = -\frac{\partial F}{\partial x} \Rightarrow \boxed{\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2}}$$

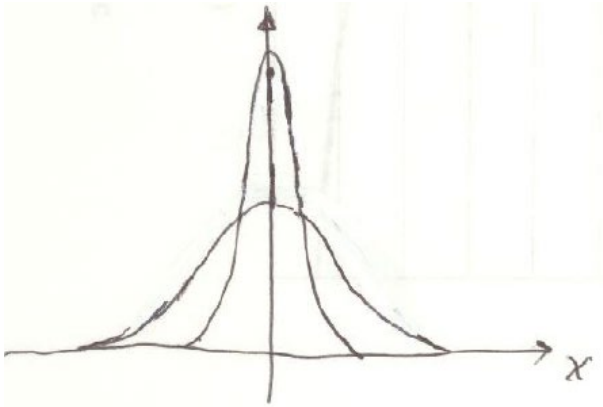
If D is a constant

Example: $C(x, 0) = Q\delta(x)$

Q: total dose

Solution: $C(x, t) = \frac{Q}{2\sqrt{\pi D t}} e^{-\frac{x^2}{4Dt}}$

Gaussian

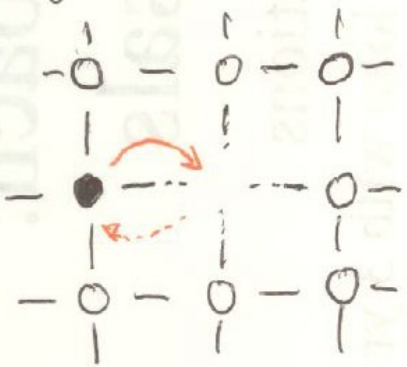


Slope varies w/ *x*, thus flows unequal.
Where do dopants go?

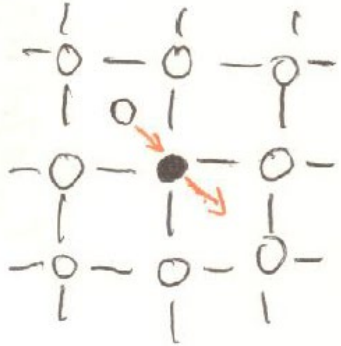
Start w/ Gaussian, always Gaussian.

Recall that the implanted profile is Gaussian to the 1st order.

In the solid state dopants don't diffuse by themselves → assisted by point defects.



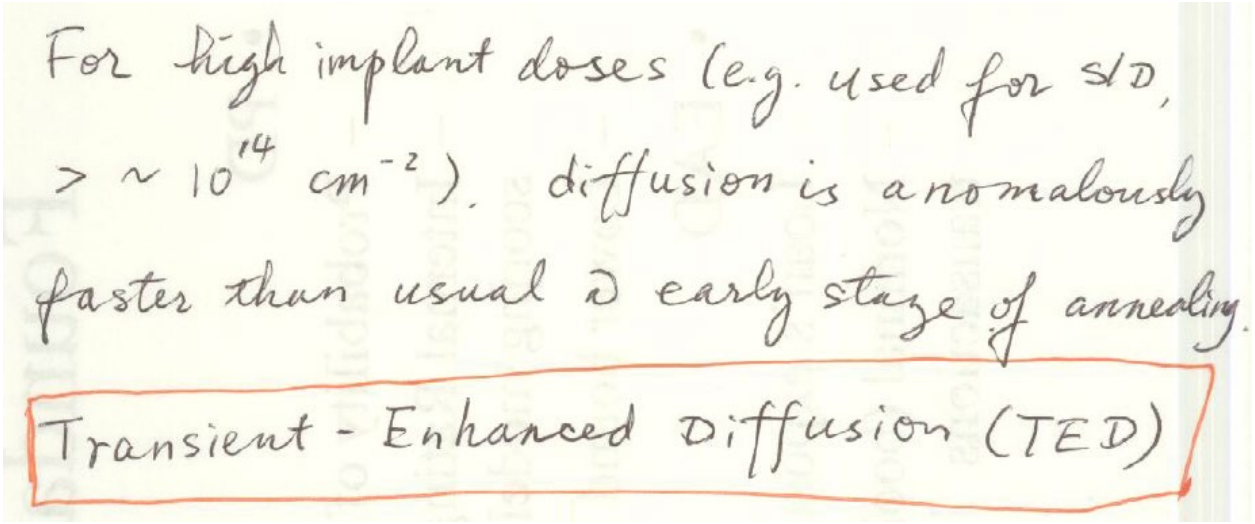
vacancy assisted



interstitial assisted.

⇒ Anomalous diffusion behaviors

Anomalous diffusion behaviors



Diffusion happens not only during intentional diffusion steps, but also whenever temperature is high (> 400 °C).

Implication?

Oxidation alters defect density and thus diffusion rates.

BEOL: Low-T deposition of interlayer dielectrics and metals

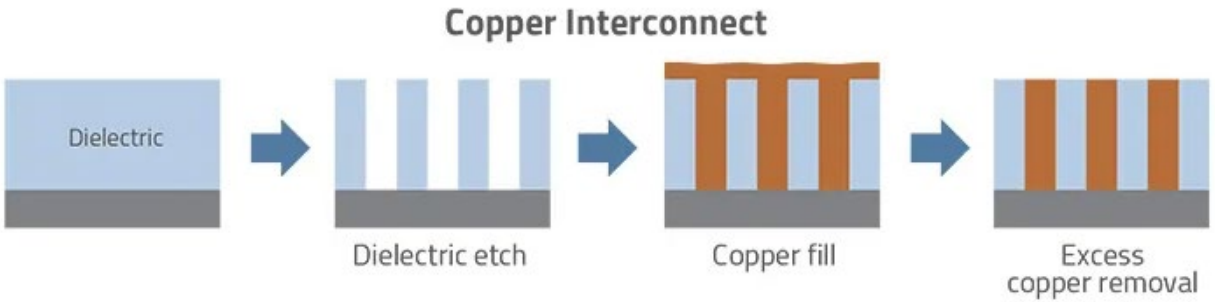
Desired properties: low dielectric constant (low k) for interlayer dielectrics;
low resistivity for interconnect metals.

Processes for their deposition limited to low temperature (< ~400 °C)
to prevent dopant diffusion in Si.

Opportunities for heterogeneous integration

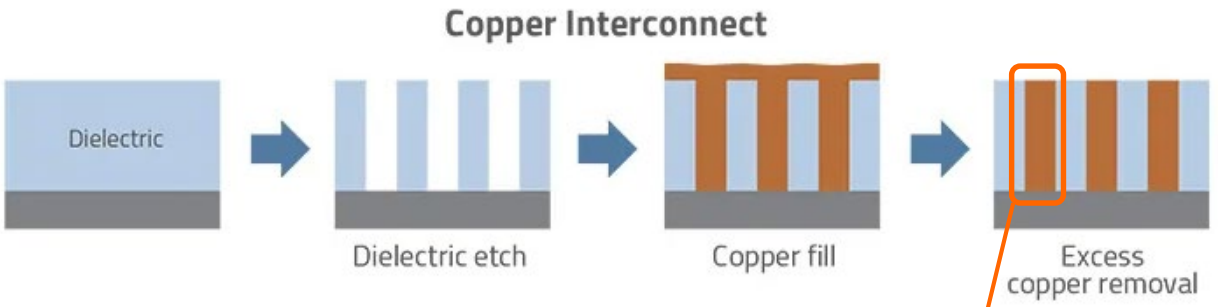
Modern and emerging interconnects

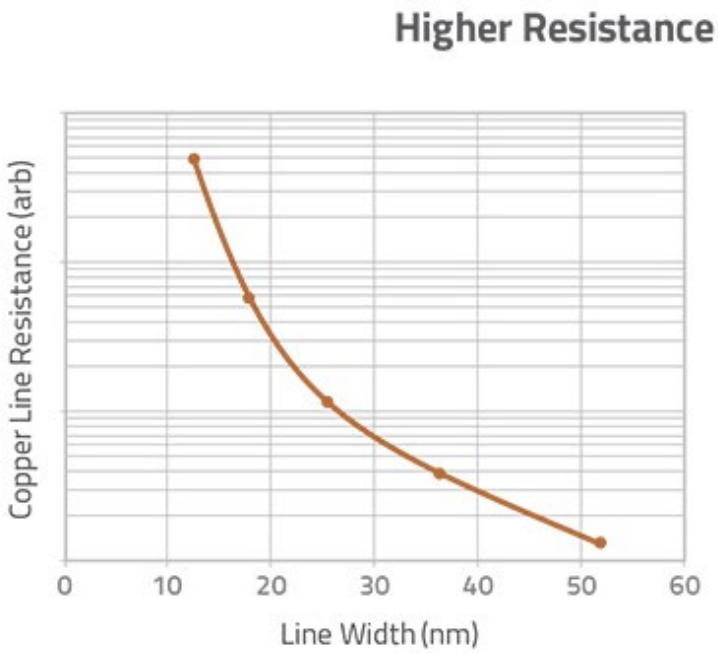
Planarity, conductivity, diffusion barriers

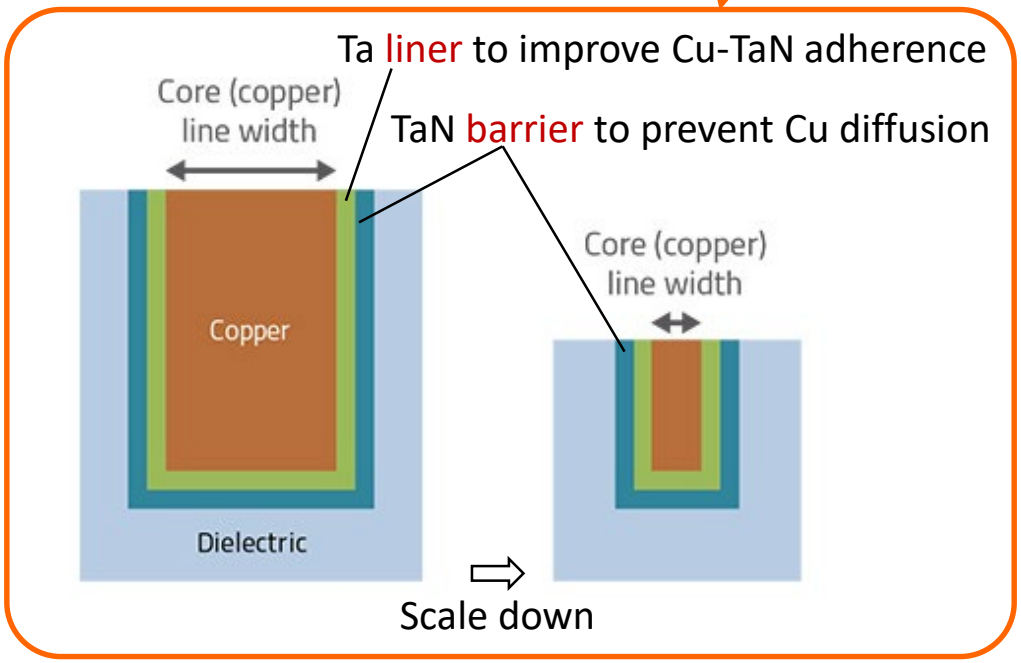


See *All About Interconnects*, https://semiengineering.com/all-about-interconnects/

Damascene process for Cu interconnects: Trench-filling deposition followed by polishing, for planarity







Challenge to further scaling: Finite minimum barrier/liner total thickness limits Cu wire width; Cu resistivity (not just resistance!) increases as wire width decreases.

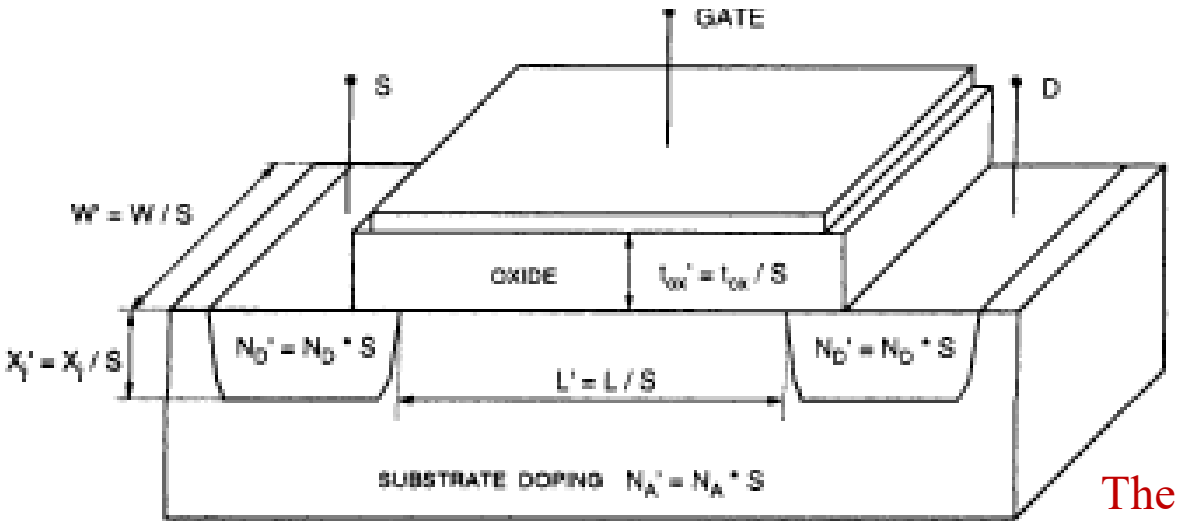
For more details about Cu interconnects and TaN/Ta barrier/liner, see Nitta et al, (2003) Copper BEOL Interconnects for Silicon CMOS Logic Technology; https://doi.org/10.1007/978-1-4615-0461-0_2

CMOS Scaling

Two motivations to scale down

- Faster transistors, both digital and analog
- To pack more functionality per area.
  - Lower the cost!

Full Scaling (Constant-Field Scaling) (which makes (some) physical sense)



Scale all dimensions and voltages by the same factor, so the field does not change, and the device physics will be about the same. Makes sense at the first glance.

The scaling factor S (also denoted α)

Table 3.2 Full scaling of MOSFET dimensions, potentials, and doping densities

Quantity	Before scaling	After scaling
Channel length	L	$L' = L/S$ ($S > 1$)
Channel width	W	$W' = W/S$
Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox}/S$
Junction depth	x_j	$x_j' = x_j/S$
Power supply voltage	V_{DD}	$V_{DD}' = V_{DD}/S$
Threshold voltage	V_{T0}	$V_{T0}' = V_{T0}/S$
Doping densities	N_A	$N_A' = S \cdot N_A$
	N_D	$N_D' = S \cdot N_D$

Will talk about these later

(A/cm)

Constant filed ➔ constant current density

$W' = W/S$ } ⇨ $I_D' = I_D/S$ (S > 1)

$P = I_D \cdot V_{DS}$ (holds for every instant)

$P' = I_D' \cdot V_{DS}' = \frac{1}{S^2} \cdot I_D \cdot V_{DS} = \frac{P}{S^2}$

Device resistance $R = V/I$. $R' = C$

Load capacitance $C = C_{ox}WL$. $C' = C/S$ Why?

Switch delay time $\tau \sim RC$. $\tau' = \tau/S$

$f_T \propto (V_G - V_{th})/L^2$ or $f_T \propto v_{sat}/L$ How's f_T doing?

Table 3.3 Effects of full scaling upon key device characteristics

Quantity	Before scaling	After scaling
Oxide capacitance	C_{ox}	$C'_{ox} = S \cdot C_{ox}$
Drain current	I_D	$I'_D = I_D/S$
Power dissipation	P	$P' = P/S^2$
Power density	$P/Area$	$P'/Area' = P/Area$

Constant-Voltage Scaling (to make some economic sense by being compatible)

Table 3.4 Constant-voltage scaling of MOSFET dimensions, potentials, and doping densities

Quantity	Before scaling	After scaling
Dimensions	W, L, t_{ox}, x_j	reduced by S ($W' = W/S, \ldots$)
Voltages	V_{DD}, V_T	remain unchanged
Doping densities	N_A, N_D	increased by S^2 ($N'_A = S^2 \cdot N_A, \ldots$)

($S > 1$)

Table 3.5 Effects of constant-voltage scaling upon key device characteristics

Quantity	Before scaling	After scaling
Oxide capacitance	C_{ox}	$C'_{ox} = S \cdot C_{ox}$
Drain current	I_D	$I'_D = S \cdot I_D$
Power dissipation	P	$P' = S \cdot P$
Power density	$P/Area$	$P'/Area' = S^3 \cdot (P/Area)$

Switch delay time $1/S^2$

Constant filed ➔ constant current density (A/cm)

$$W' = W/S \Rightarrow I_D' = I_D/S$$

Let's check this out:

e's per area

Areal carrier charge density in channel $qn = \frac{\varepsilon_{ox}(V_{GS}-V_{th})}{t_{ox}} \Rightarrow n' = n$

if we scale V_{th} by the same factor S, i.e., $V'_{th} = V_{th}/S$

$$\Rightarrow J_s' = J_s$$

$$J_s = \mu qnE_{lateral}$$

A/cm $\qquad \frac{\cancel{\text{cm}^2}}{\text{Vs}} \frac{\text{C}}{\cancel{\text{cm}^2}} \frac{\cancel{\text{V}}}{\text{cm}} = \text{A/cm}$

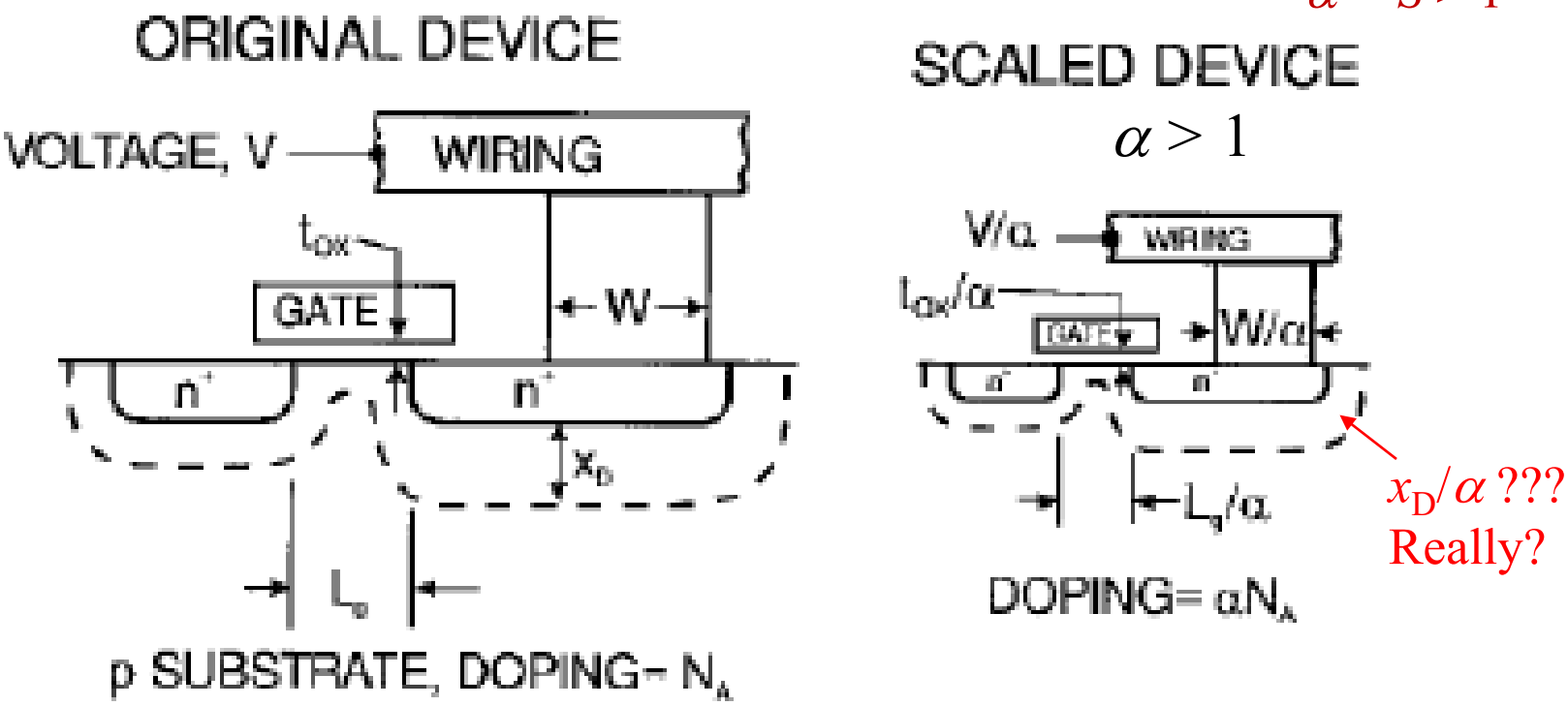
$$I_D = J_s W \Rightarrow I_D' = I_D/S$$

The rationale for constant-field scaling (the "physical sense" it makes):
Device behavior does not change if we scale all dimensions by the same factor while maintaining same electric field.

The rationale for constant-field scaling (the "physical sense" it makes):
Device behavior does not change if we scale all dimensions by the same factor while maintaining same electric field.

Simple constant-field scaling: $V \rightarrow V/\alpha$, $I \rightarrow \alpha I$

$\alpha = S > 1$



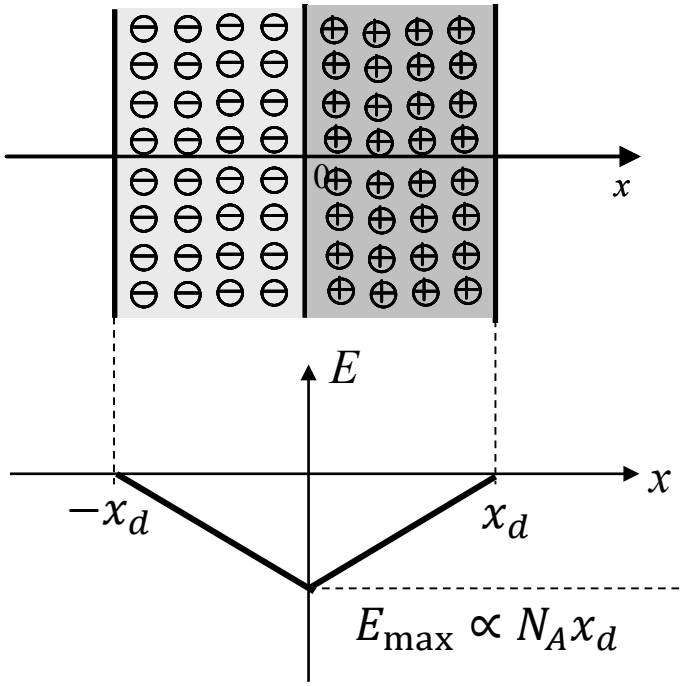
$$x_d \propto \sqrt{\ln(N_D N_A / n_i^2)} / \sqrt{N_A} \quad \Rightarrow \quad x_d' = x_d/\sqrt{\alpha}$$

Consider a simple pn junction within the depletion approximation
(keep in mind the S/D junctions & the depletion under the channel)

Think graphically about *E*, potential, and the band diagram

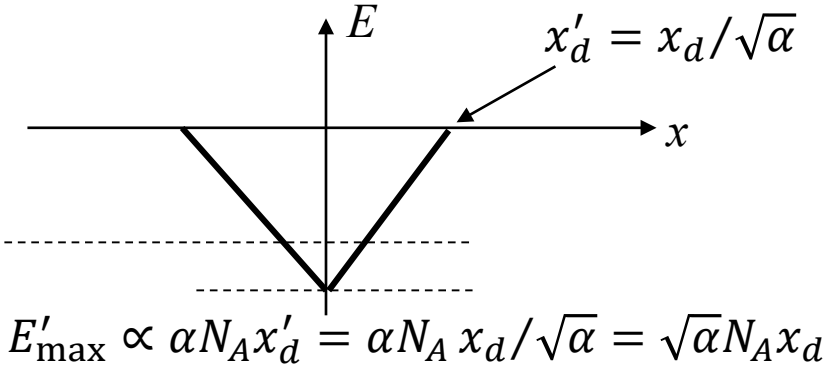
Original

For simplicity, $N_D = N_A$ (or $N_D >> N_A$)



Scaled

$\alpha N_A \quad \alpha N_D$



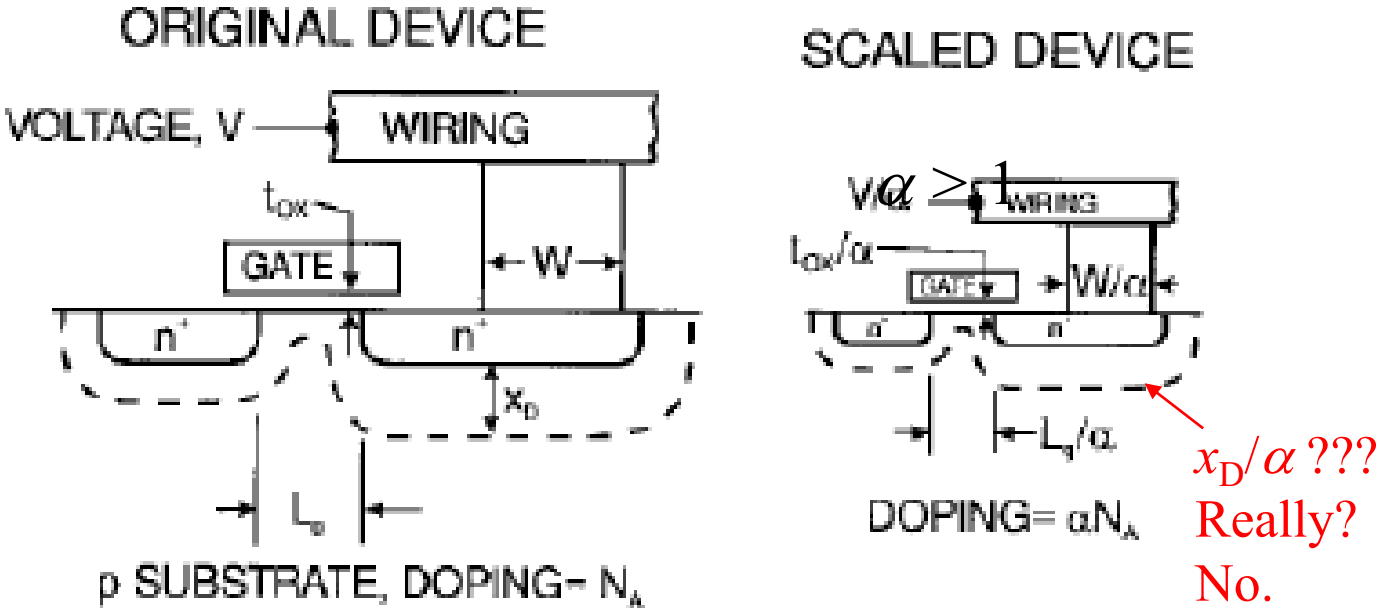
The integral of the field is the built-in potential: $\phi_i \propto E_{\max} x_d \implies \phi'_i = \phi_i$

This looks good - built-in voltage not changed by full (constant-field scaling).
But, there is a problem…

The rationale for constant-field scaling (the "physical sense" it makes):
Device behavior does not change if we scale all dimensions by the same factor while maintaining same electric field.

Simple constant-field scaling: $V \rightarrow V/\alpha$, $I \rightarrow \alpha I$ $\qquad \alpha = S > 1$

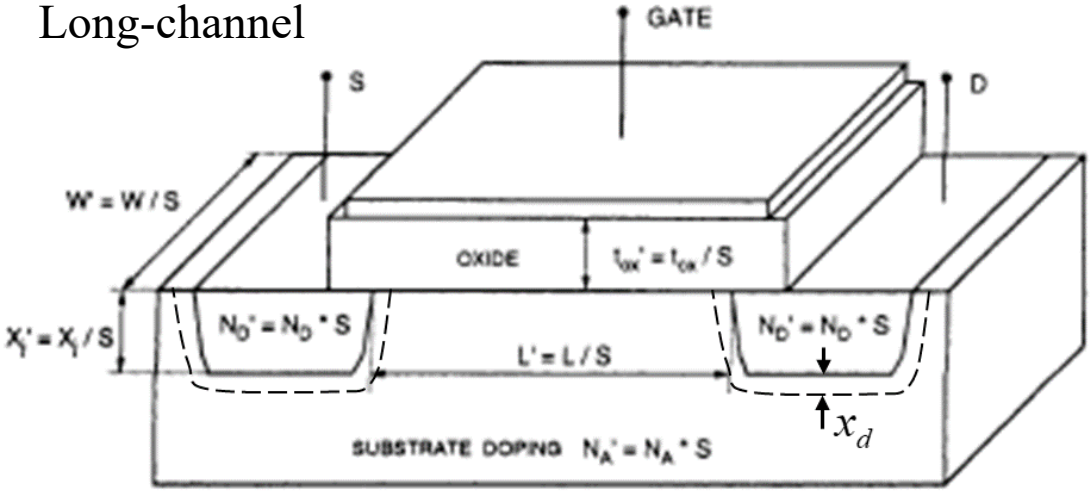
Short-channel



x_D/α ??? Really? No.

$x'_d = x_d/\sqrt{\alpha}$

Long-channel

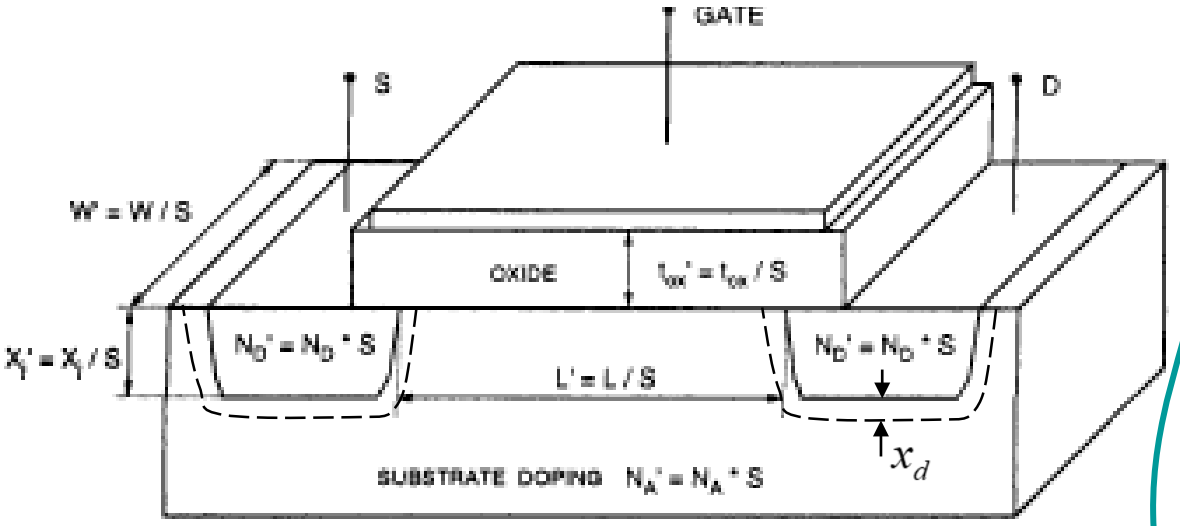


x_d scales not as much as other dimensions.

Not an issue in the good, old days, when MOSFETs were large.

But a problem for small devices, say, $2x_d > L$ (above).

Full Scaling (Constant-Field Scaling) (which makes (some) physical sense)



$$x_d' = x_d/\sqrt{S}$$

Another issue: we need to scale V_{th} by factor S

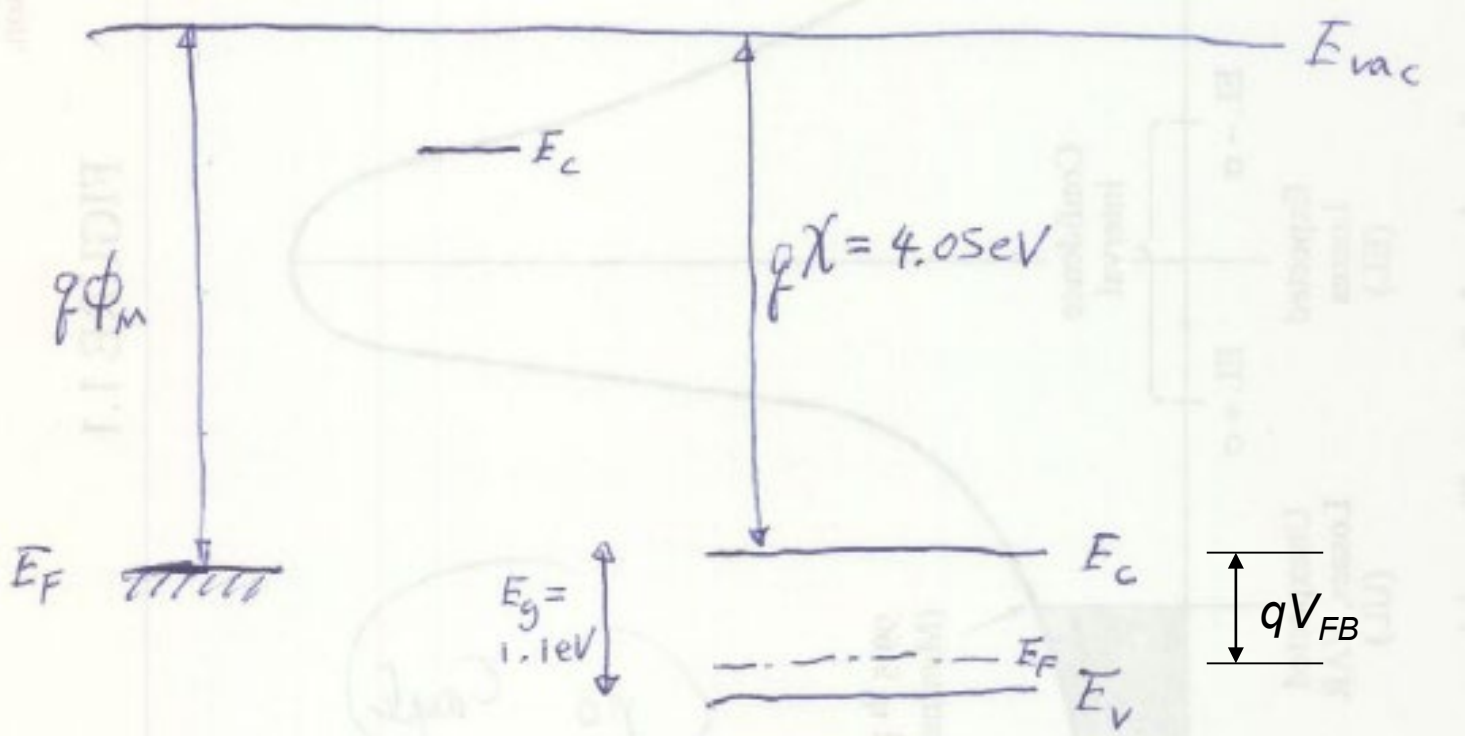
$$V_{th} = V_{FB} + 2\phi_p + \frac{\sqrt{2\varepsilon q N_A (2\phi_p)}}{C_{ox}}$$

Doesn't scale.
Need V_{th} adjustment.

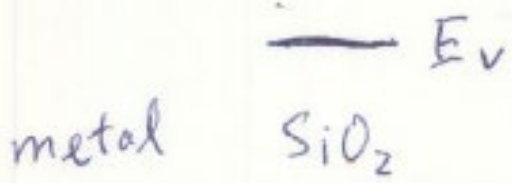
Table 3.2 Full scaling of MOSFET dimensions, potentials, and doping densities

Quantity	Before scaling	After scaling
Channel length	L	$L' = L/S$
Channel width	W	$W' = W/S$
Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox}/S$
Junction depth	x_j	$x_j' = x_j/S$
Power supply voltage	V_{DD}	$V_{DD}' = V_{DD}/S$
Threshold voltage	V_{T0}	$V_{T0}' = V_{T0}/S$
Doping densities	N_A	$N_A' = S \cdot N_A$
	N_D	$N_D' = S \cdot N_D$

($S > 1$)



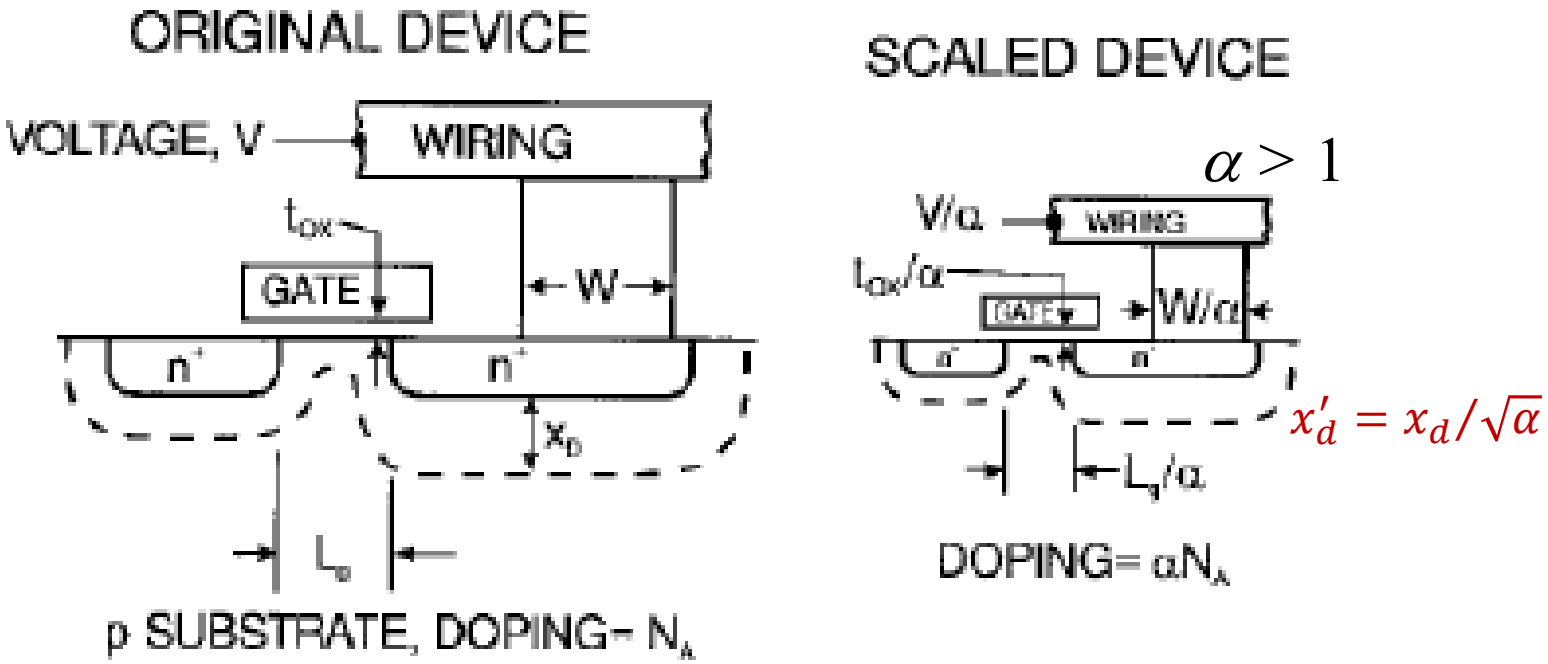
V_{FB} does not scale.



Work out the details of constant-voltage scaling offline

The happy (although with messy adjustments) scaling days are long gone.
There are many issues with scaling… (We are not going to talk about all of them.)
Among them, electrostatic control.

Simple constant-field scaling: $V \rightarrow V/\alpha$, $I \rightarrow \alpha I$



The wafer is still "infinitely thick" for the scaled FET.
The smaller L, the worse leakage.

L	t_{ox}
800 nm	18 nm
20 nm	0.45 nm

Matter (Si, SiO_2, etc.) is "discrete".
We are counting atoms.

The Si-O bond length in SiO_2 is 0.16 nm

Moore's Law

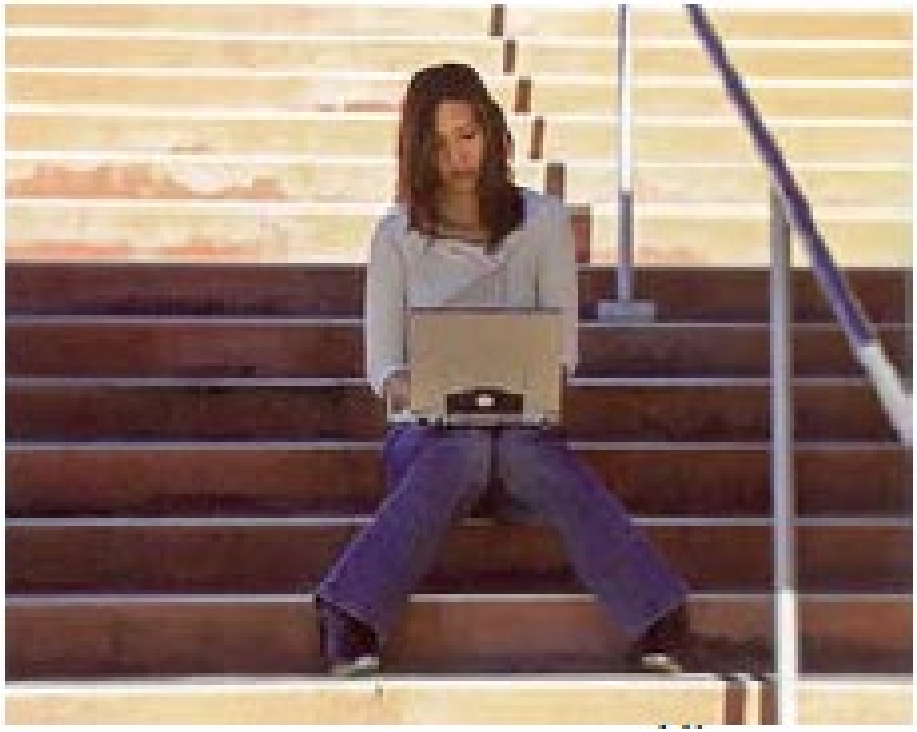
- Gordon E. Moore (born 1929), a co-founder of Intel
- Moore's Law is the **empirical observation** made in 1965 that the number of transistors on an integrated circuit **for minimum component cost** doubles every 24 months (sometimes quoted as 18 months).
- Moore's law is not about just the density of transistors that can be achieved, but about the density of transistors at which the cost per transistor is the lowest.

Why Small (if they are already so small that we can't make them better)?

- To pack more functionality into each unit area
  - With feature size shrinking and wafer size growing, more and better products each wafer – better economics

Transistor radio!

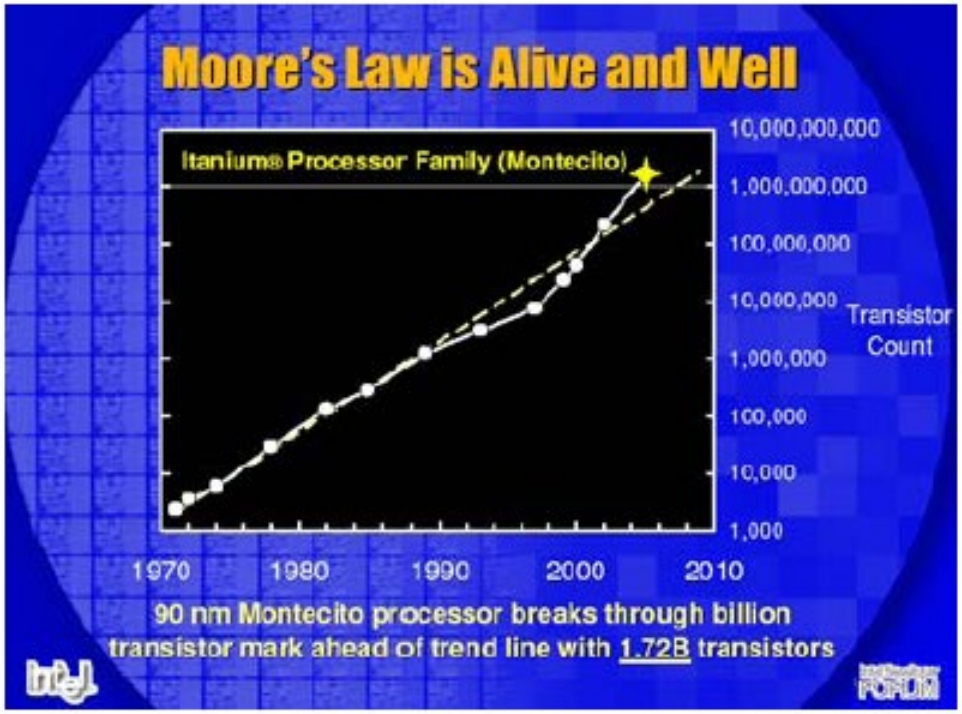
1965: $1/transistor



2006: 1 "microdolar"/transistor

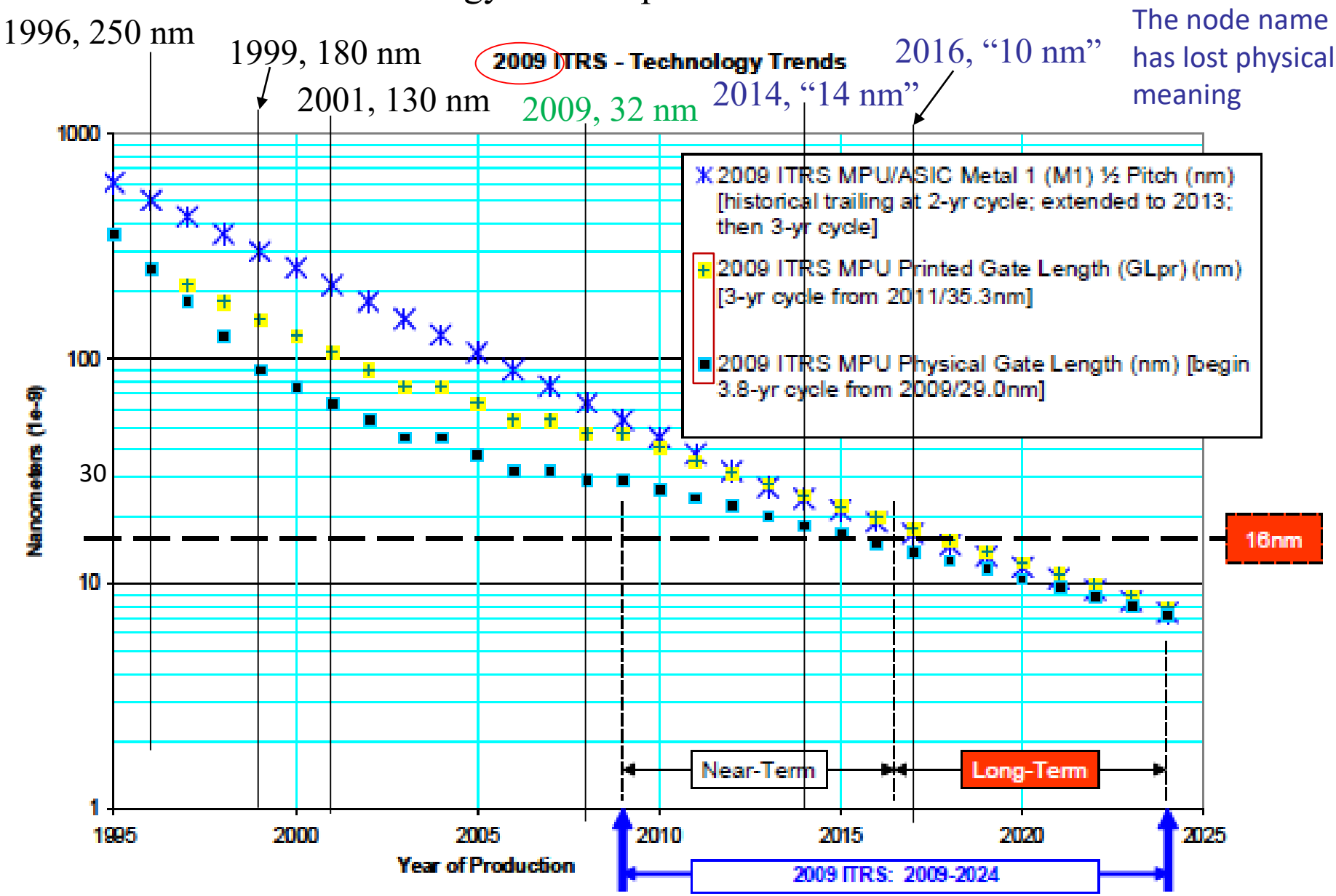
Moore's Law is Alive and Well

(2006)



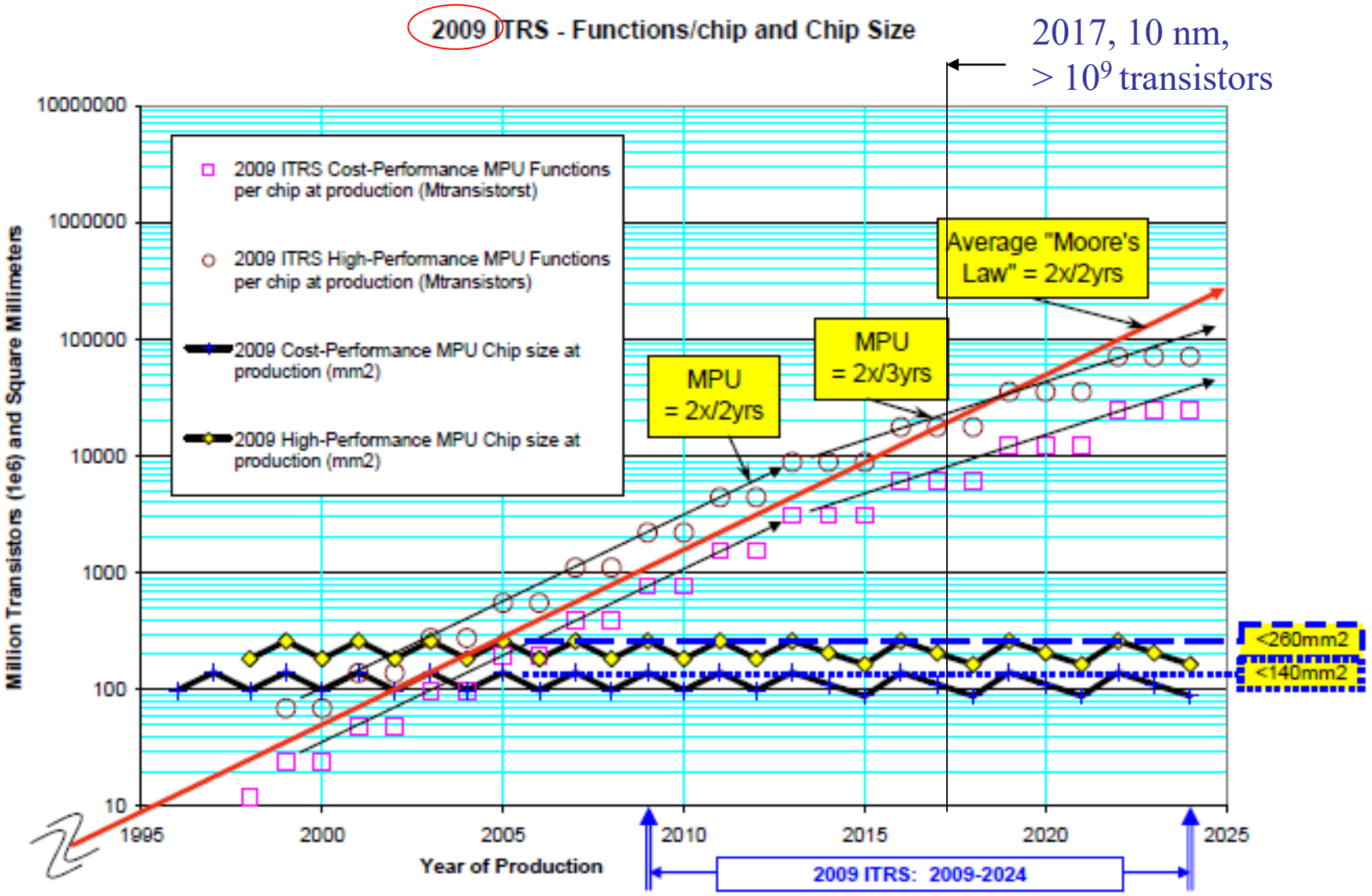
Source: M. Bohr, Intel Development Forum, September 2004.

ITRS: International Technology Roadmap for Semiconductors

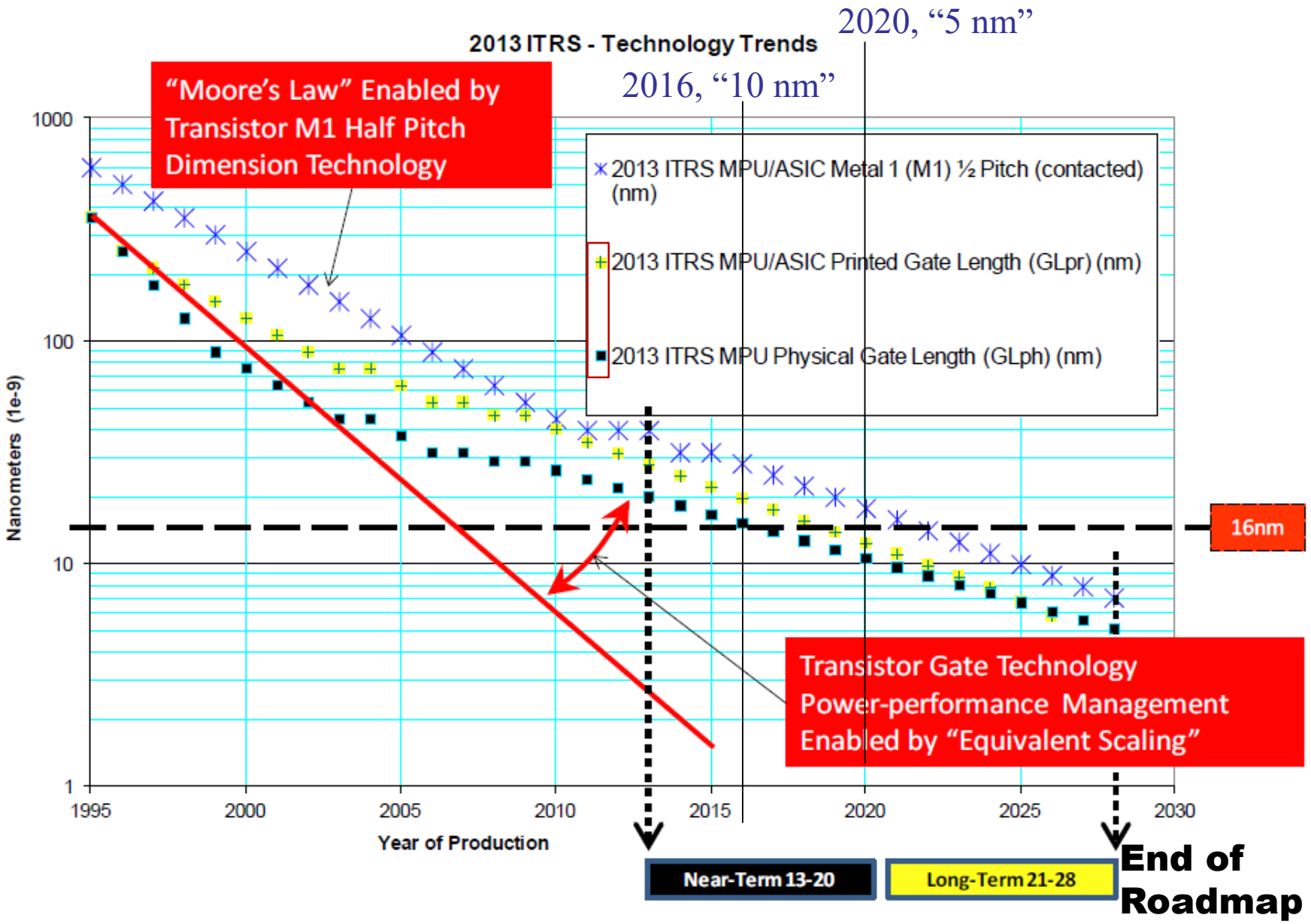


https://www.semiconductors.org/resources/2009-international-technology-roadmap-for-semiconductors-itrs/

For ITRS, see https://en.wikipedia.org/wiki/International_Technology_Roadmap_for_Semiconductors


2009 ITRS - Functions/chip and Chip Size
2017, 10 nm,
> 10^9 transistors
2009 ITRS Cost-Performance MPU Functions per chip at production (Mtransistorst)
2009 ITRS High-Performance MPU Functions per chip at production (Mtransistors)
2009 Cost-Performance MPU Chip size at production (mm2)
2009 High-Performance MPU Chip size at production (mm2)
Average "Moore's Law" = 2x/2yrs
MPU = 2x/3yrs
MPU = 2x/2yrs
<260mm2
<140mm2
Million Transistors (1e6) and Square Millimeters
10000000
1000000
100000
10000
1000
100
10
1995
2000
2005
2010
2015
2020
2025
Year of Production
2009 ITRS: 2009-2024

2013: the last roadmap



https://www.semiconductors.org/resources/2013-international-technology-roadmap-for-semiconductors-itrs/

Sunsetting of Moore's Law

- People had talked about the end for many years.
- Processing limits had been overcome; new materials (e.g. high-k dielectrics) had been introduced.
- New device architectures have been employed.
- We are hitting the physics limits. What's next?

2013 ITRS was the last roadmap (of the type we knew), with end of road at 2028.

ITRS was succeeded by "ITRS 2.0", as announced in 2014.

2015 ITRS 2.0 was the first and the final one.

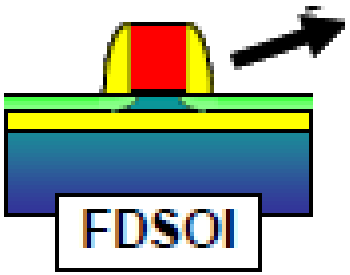
Susetting official, new roadmapping started, named the International Roadmap for Devices and Systems (IRDS).

For overview, see https://en.wikipedia.org/wiki/International_Technology_Roadmap_for_Semiconductors.
For ITRS (& -2.0) documents, http://www.itrs2.net/itrs-reports.html

Device concepts that have kept Moore's law alive

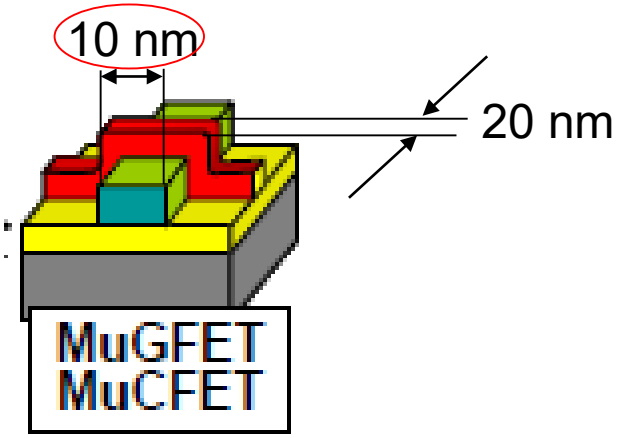
For good electrostatic control, we really need to get rid of the body (bulk)

Two solutions (that are no longer new)



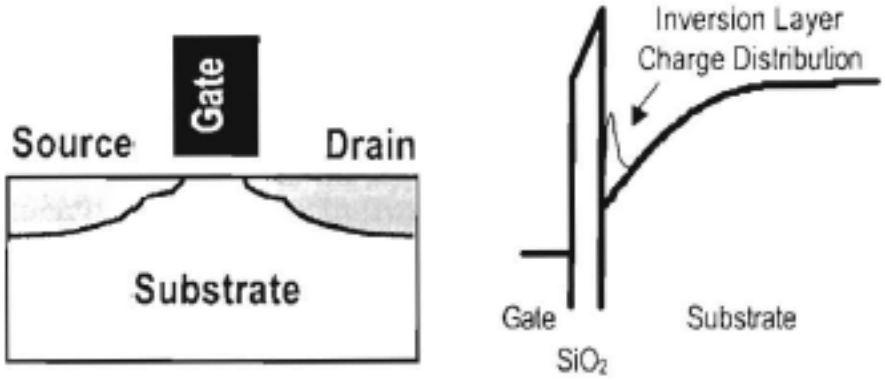
For L = 20 nm,
the Si needs to be
thinner than 5 nm.

Ultra-thin body silicon-on-insulator



FinFET, 3D FET

Further reading: "Transistor Wars," IEEE spectrum, November **2011**
http://spectrum.ieee.org/semiconductors/devices/transistor-wars

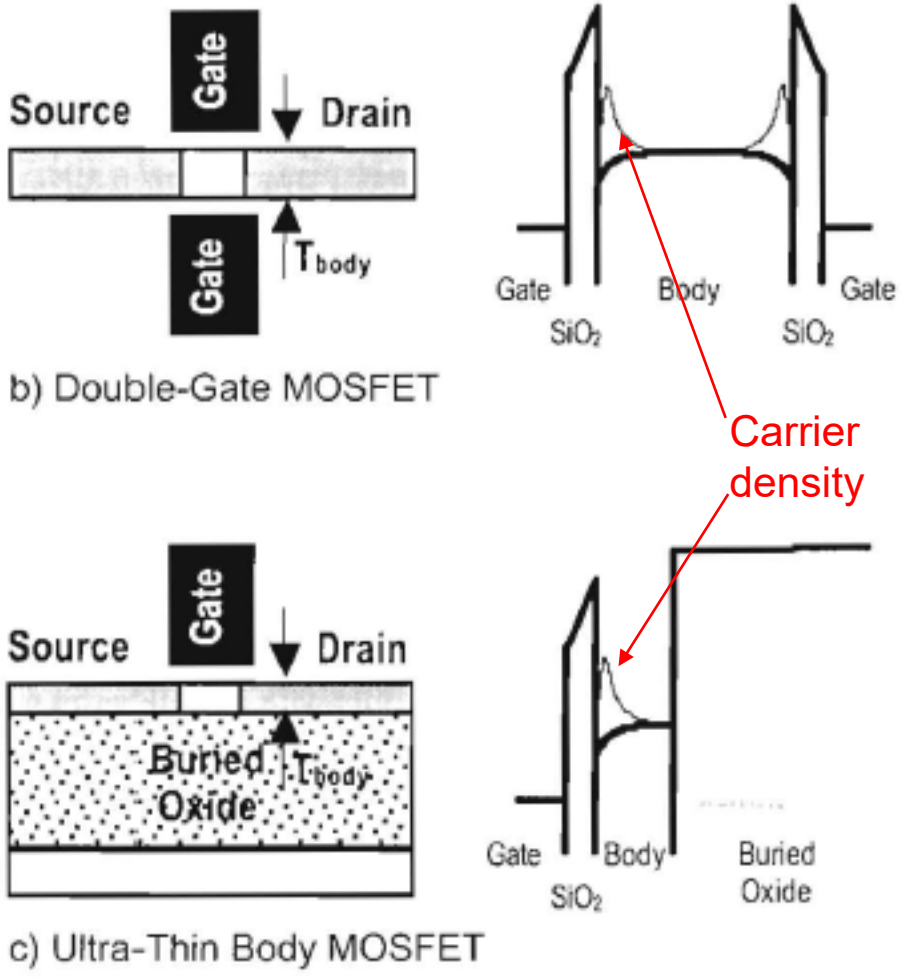


a) Bulk MOSFET

Deplete and then invert.

The bulk is a path for leakage.

Will need very high N_A for the substrate, to scale down the x_d of the S/D junctions, as well as the x_{dmax} of the FET channel. This will cause high S-to-D leakage.



b) Double-Gate MOSFET

c) Ultra-Thin Body MOSFET

Thin bodies don't have to be doped.

➔ No need for depletion

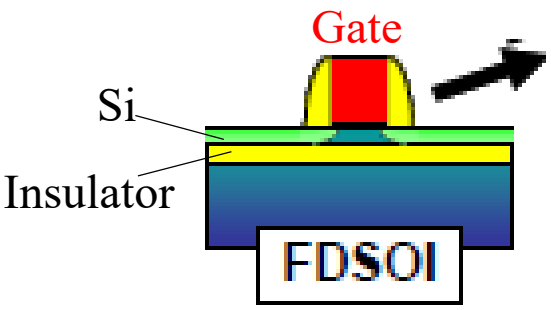
➔ Lower vertical fields

Why is SOI a challenge?

http://en.wikipedia.org/wiki/Silicon_on_Insulator

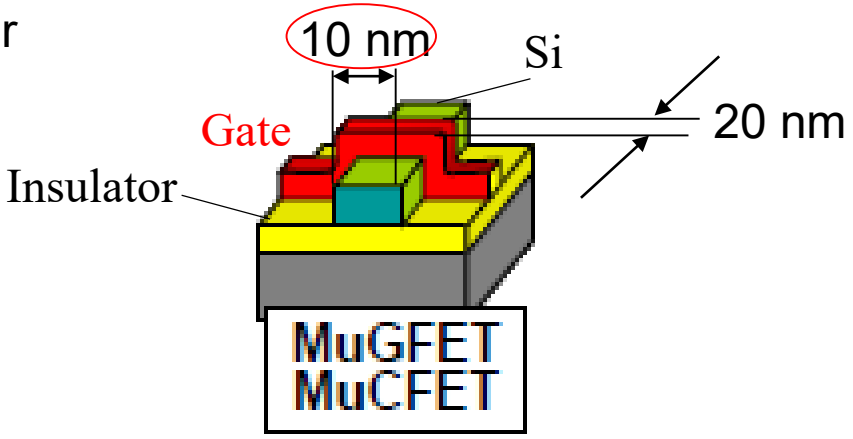
For good electrostatic control, we really need to get rid of the body (bulk)

Solutions (for now)



For L = 20 nm,
the Si needs to be
thinner than 5 nm.

Ultra-thin body silicon-on-insulator

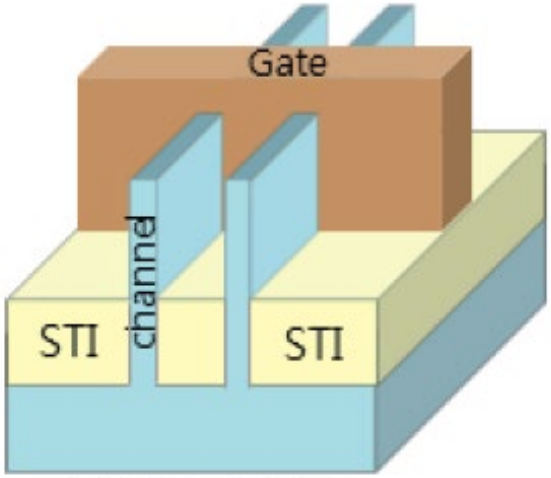


FinFET, 3D FET

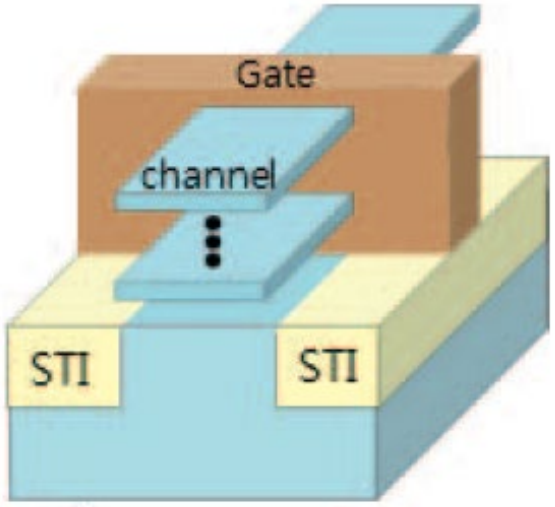
FinFET won this war.
Gate wrapped around channel
→ better electrostatic control.

"Transistor Wars," IEEE spectrum, November **2011**
http://spectrum.ieee.org/semiconductors/devices/transistor-wars

End-of-roadmap device: nanosheet FET



Multiple-channel FinFET



Multiple-channel nanosheet FET: gate all around

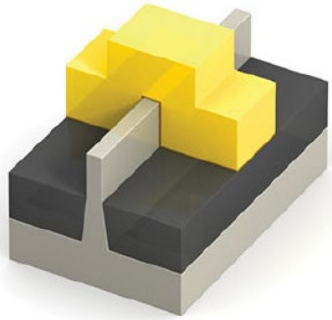
Figures from Bae et al, IEEE IEDM **2018**

References:

Ye et al, The Nanosheet Transistor Is the Next (and Maybe Last) Step in Moore's Law, *IEEE Spectrum* July **2019**.
https://spectrum.ieee.org/semiconductors/devices/the-nanosheet-transistor-is-the-next-and-maybe-last-step-in-moores-law

Johnson, IBM Introduces the World's First 2-nm Node Chip, *IEEE Spectrum* May **2021**.
https://connect.ieee.org/NzU2LUdQSC04OTkAAAF9BQS97DrruM8XkwCjLv66z31NGa5XTkwdpNrnybOGTlHhr3rhY_n6RXkoCokOtjryLNfwpjM=

Ye, *IEEE Spectrum* 2019

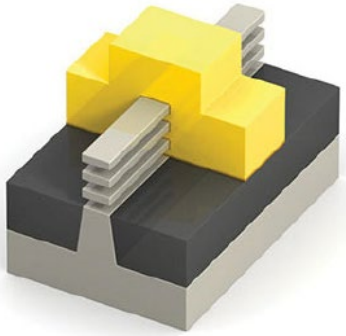


FinFET

Surrounding the channel region on three sides with the gate gives better control and prevents current leakage.

2019 cutting edge: 7 nm

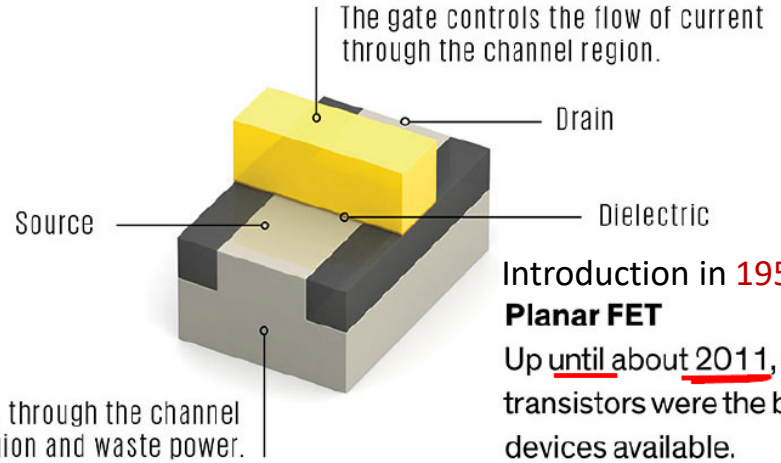
Samsung to go nanosheet at 3 nm



Stacked nanosheet FET

The gate completely surrounds the channel regions to give even better control than the FinFET.

Names: gate-all-around, multibridge channel, nanobeam, nanosheet.



Introduction in 1959

Planar FET

Up until about 2011, planar transistors were the best devices available.

2020: TSMC 5 nm, Si:Ge finFET

TSMC introduced a high mobility channel (HMC) transistor at 5 nm by incorporating germanium into the transistor fin.

FinFETs reaching end of life even with Si:Ge HMC fin.

TSMC to move to nanosheet w/ gate all around at 3 nm.

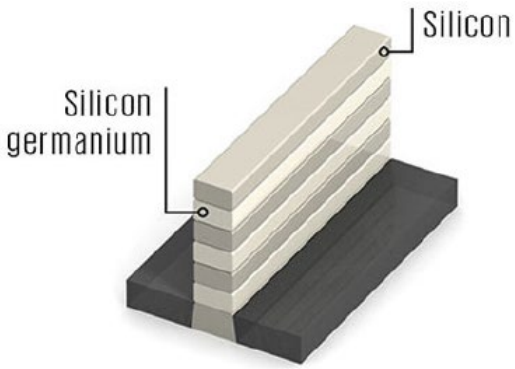
Ref: Scansen, ISSCC 2021: A Bright Foundry Future, *Asia Report* Feb **2021**

TSMC later says to stay with FinFETs just for 3 nm.

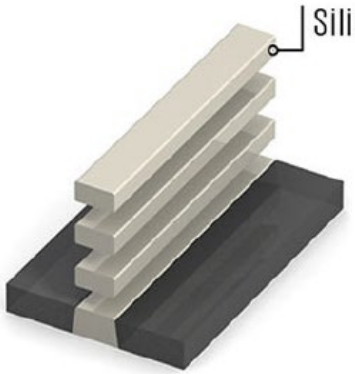
Reorted by S.K. Moore, Samsung's 3-nm Tech Shows Nanosheet Transistor Advantage, *IEEE Spectrum* May 2021;
https://spectrum.ieee.org/nanoclast/semiconductors/memory/samsungs-3nm-tech-shows-nanosheet-transistor-advantage

Confirmed by May 2021 by Johnson, IBM Introduces the World's First 2-nm Node Chip, *IEEE Spectrum* May **2021**.

Nanosheet FET fabrication

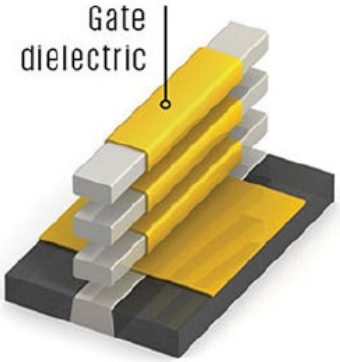


A superlattice of silicon and silicon germanium are grown atop the silicon substrate.

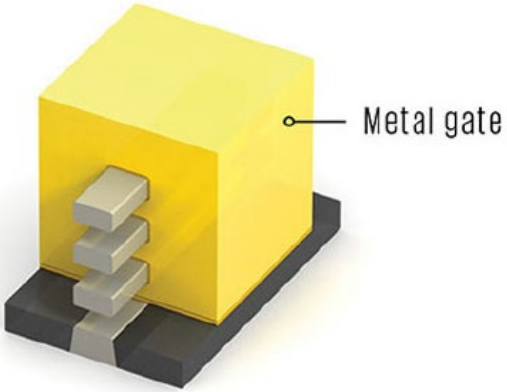


A chemical that etches away silicon germanium reveals the silicon channel regions.

Si nanosheets not floating in space; bridge structure not shown



Atomic layer deposition builds a thin layer of dielectric on the silicon channels, including on the underside.



Atomic layer deposition builds the metal gate so that it completely surrounds the channel regions.

Ye et al, The Nanosheet Transistor Is the Next (and Maybe Last) Step in Moore's Law, *IEEE Spectrum* July **2019**.

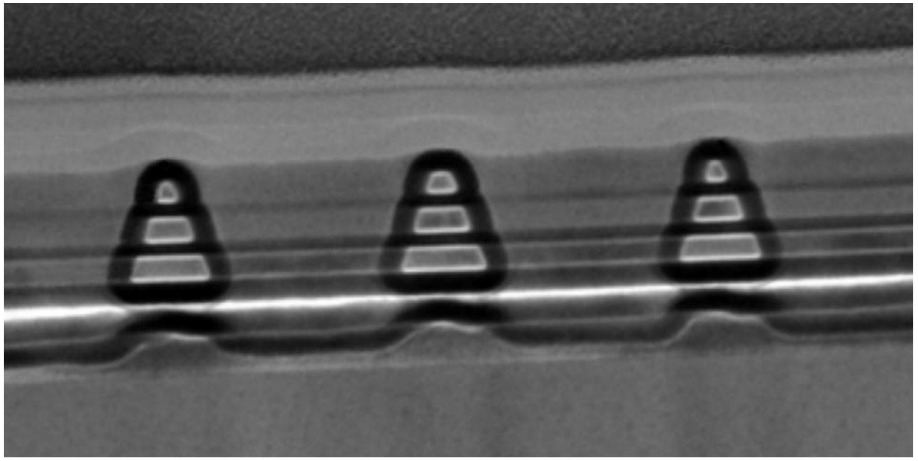
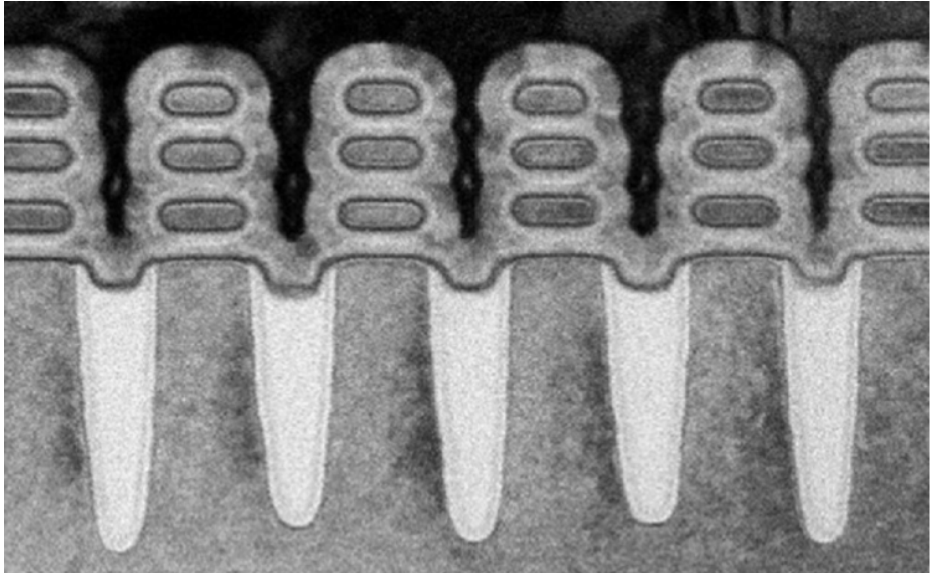
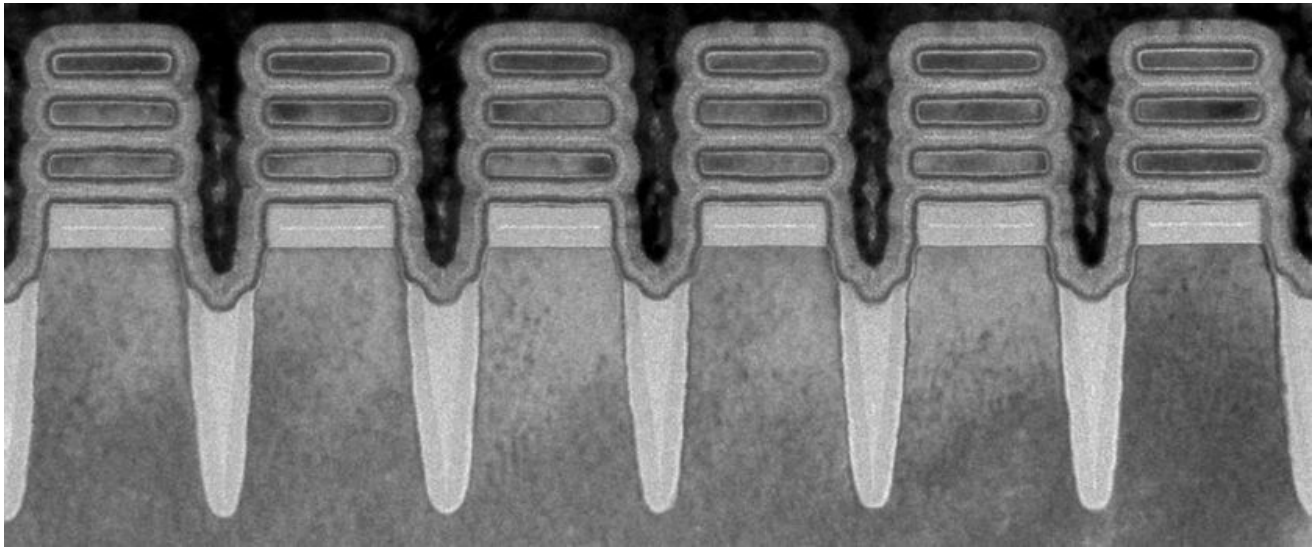


Image: Purdue University



Ye et al, The Nanosheet Transistor Is the Next (and Maybe Last) Step in Moore's Law, *IEEE Spectrum* July **2019**.



Row of 2-nm nanosheet devices IMAGE: IBM

Johnson, IBM Introduces the World's First 2-nm Node Chip, *IEEE Spectrum* May **2021**.

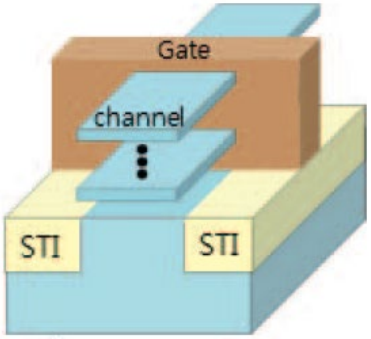


Illustration from Bae et al, IEEE IEDM **2018**

Sunsetting of Moore's Law

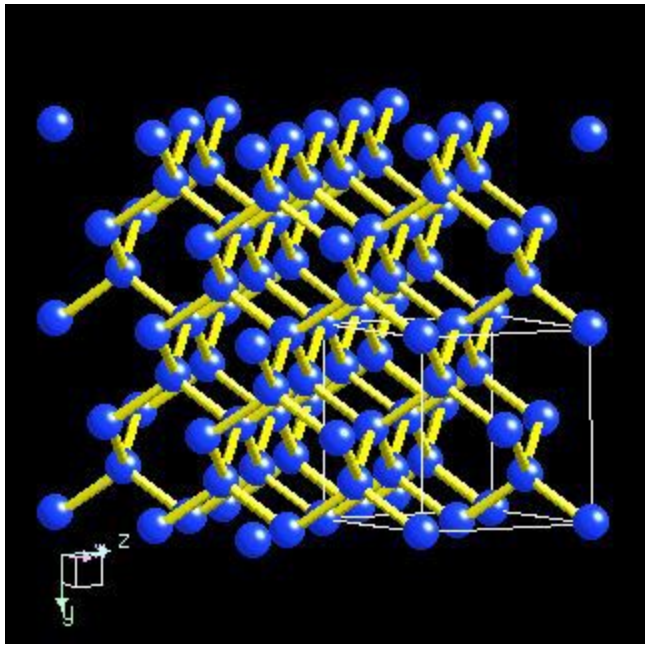
- People had talked about the end for many years.
- Processing limits had been overcome; new materials (e.g. high-k dielectrics) had been introduced.
- New device architectures have been employed.
- We are hitting the physics limits. What's next?

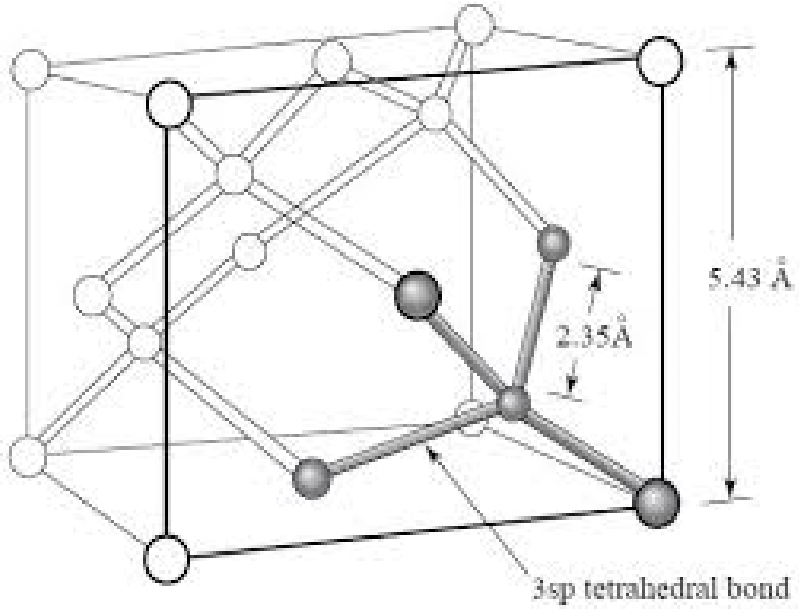
Forget about details.
The crystal constant of Si is 0.54 nm.
5 nm is only ~10 crystal constants!

Do the (semi-classical) semiconductor physics theories we rely on still work?

Are there alternatives to scaling to achieve faster devices?

Crystal structure of Si

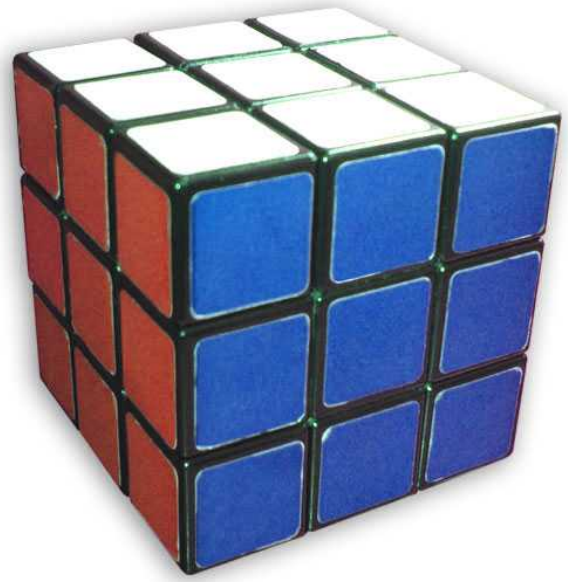




http://www.webelements.com/silicon/crystal_structure.html

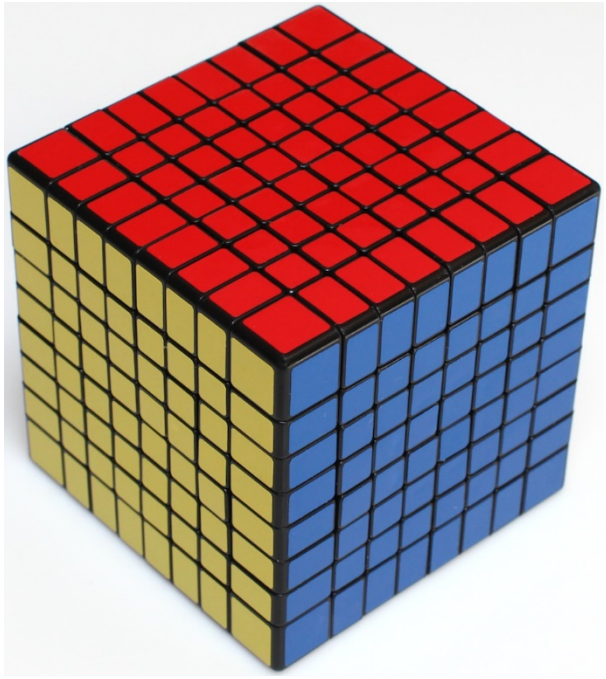
http://onlineheavytheory.net/silicon.html

If several monolayers thin, is Si still the Si as we know it?



$3^3 = 27$

$(3-2)^3 = 1$



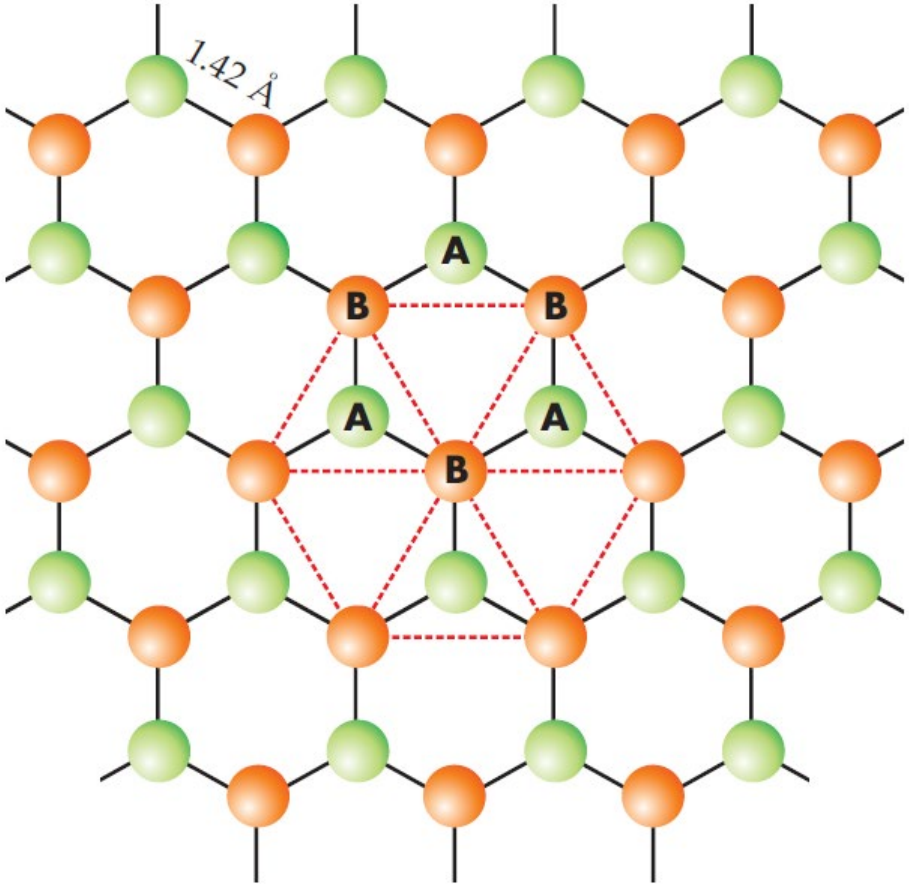
$10^3 = 1000$

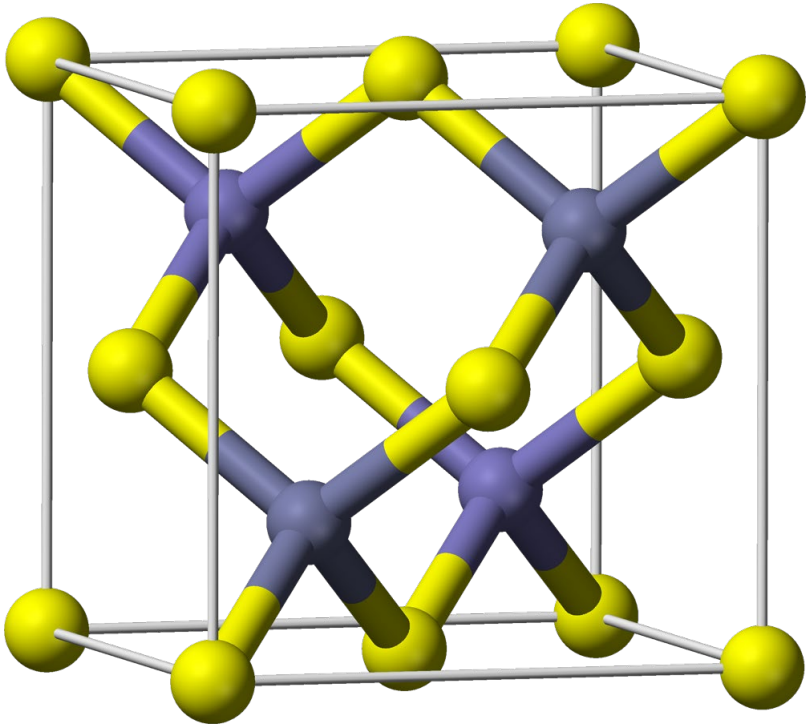
$(10-2)^3 = 512$

Half of the small cubes are on the surface!

How thin can Si (or any 3D stuff) go?
For a 3D material, if we make it a few atoms thin, it's no longer that material as we know it!
(Recall that 10X10X10 cube)

The need for lower dimensional materials

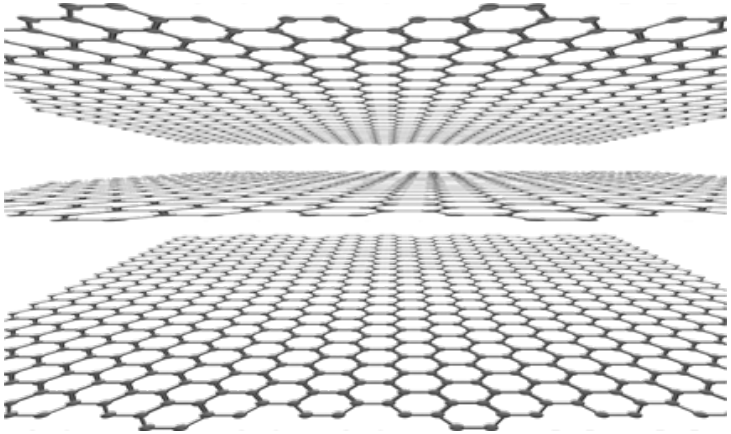




For example, graphene is 2D.
It's 1-atom thin by nature.
The "ultimate SOI" if we put it on an insulator.

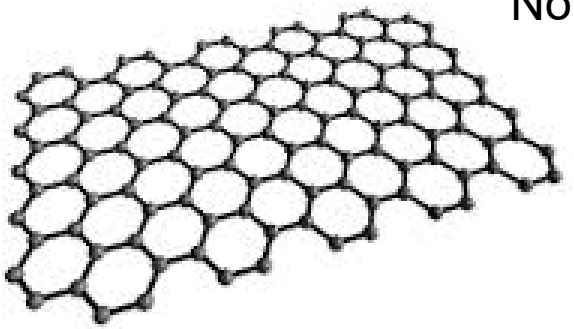
If it ever (?) becomes the post-Si semiconductor, its 2D nature (actually, we may need to turn it into 1D) probably deserves more kudos than its fast moving electrons.

At the end of the road, we look for alternatives.
We want things that are inherently low dimensional (2D or 1D)

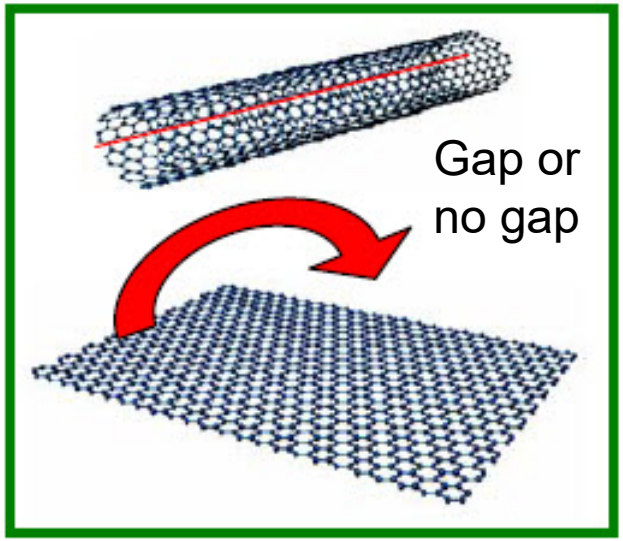


Graphite: 3D but layered (w/ van der Waals gaps)

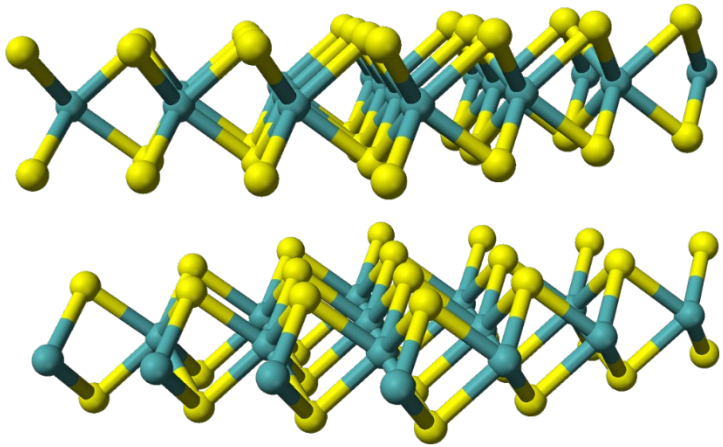
No band gap



Graphene: 2D



Carbon nanotube: (quasi-)1D

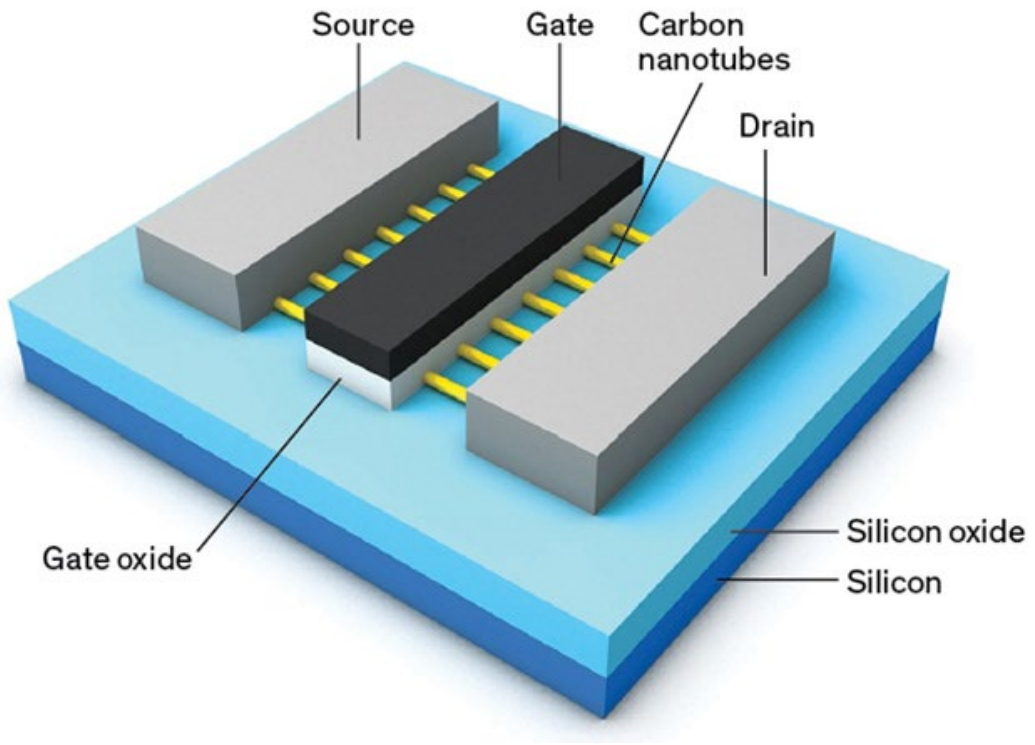


Other 2D materials, e.g. MoS_2, with band gaps

Carbon nanotube FETs are considered promising.

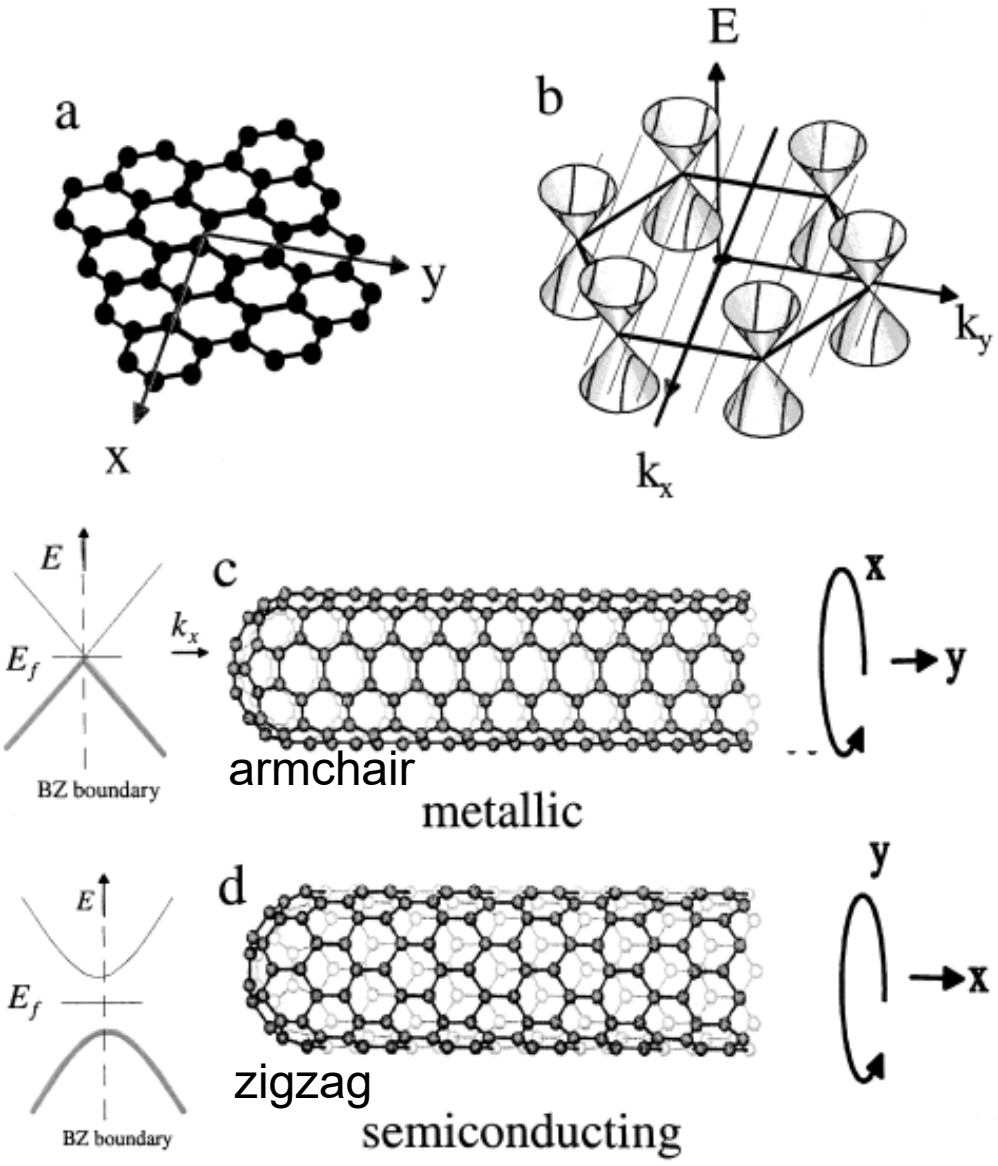
1D. Good electrostatic control.

Challenges:
To achieve uniform diameter and chirality (for uniform band gap)
To place them into a dense, parallel array

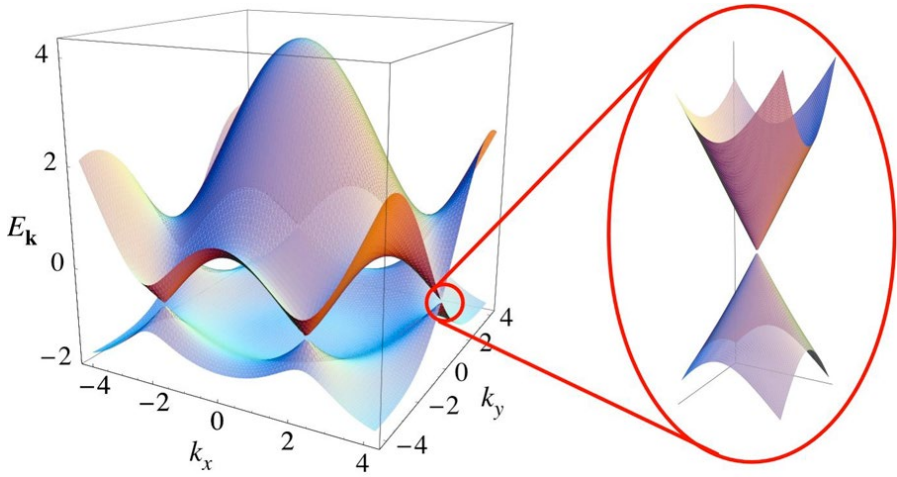


https://spectrum.ieee.org/semiconductors/devices/how-well-put-a-carbon-nanotube-computer-in-your-hand

Band structures of single-wall carbon nanotubes



Band structure of graphene

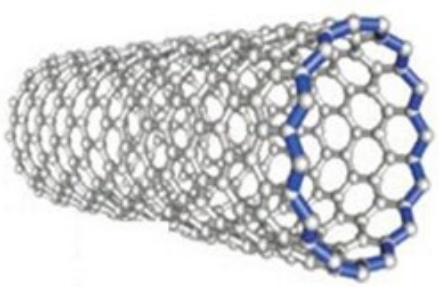


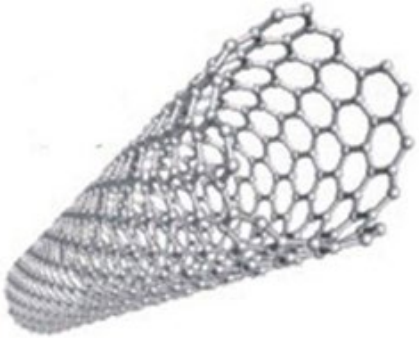
http://exciting-code.org/carbon-graphene-from-the-ground-state-to-excitations

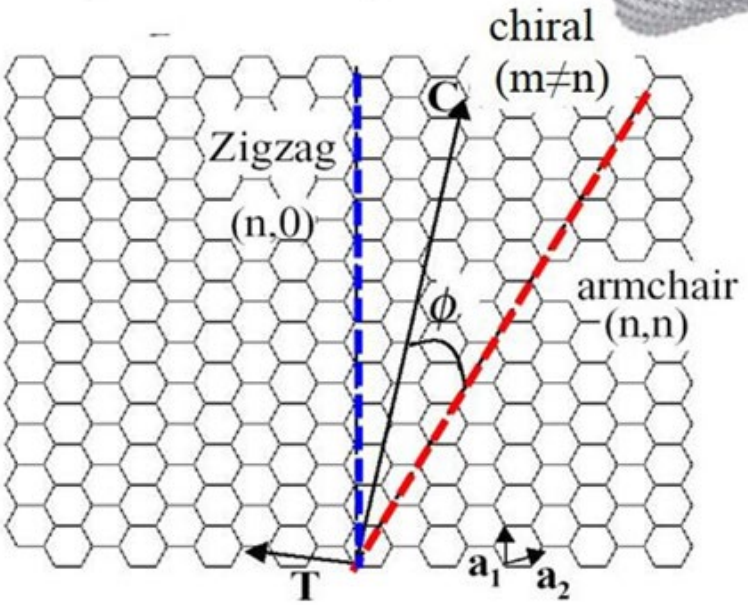
Simple theory to construct nanotube band structure:
Quantizing **k**

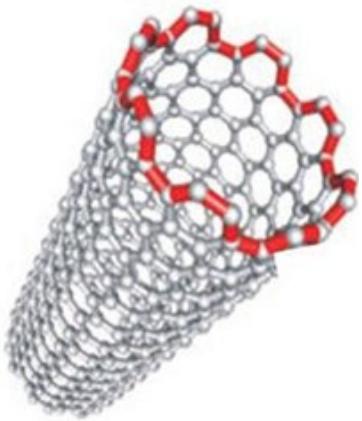
McEuen et al, IEEE Trans on Nanotech **99**, 78 (2002)

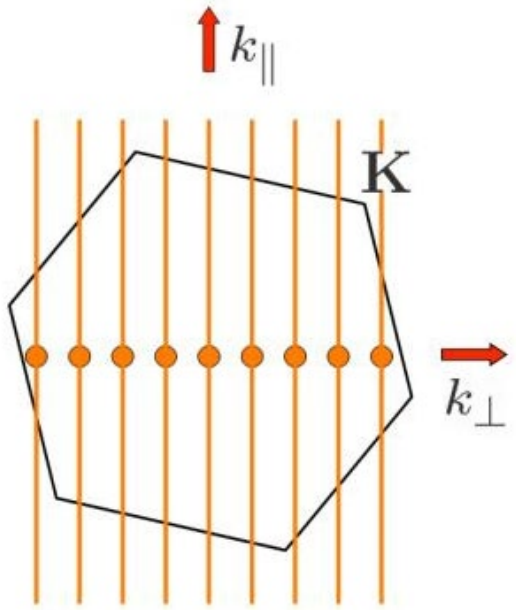
Carbon nanotube indexing











Simple theory to construct nanotube band structure: Quantizing **k**

https://www.frontiersin.org/articles/10.3389/fchem.2015.00059/full

Simple theory (not exact):

$n - m$ = multiple of 3 ➔ metallic

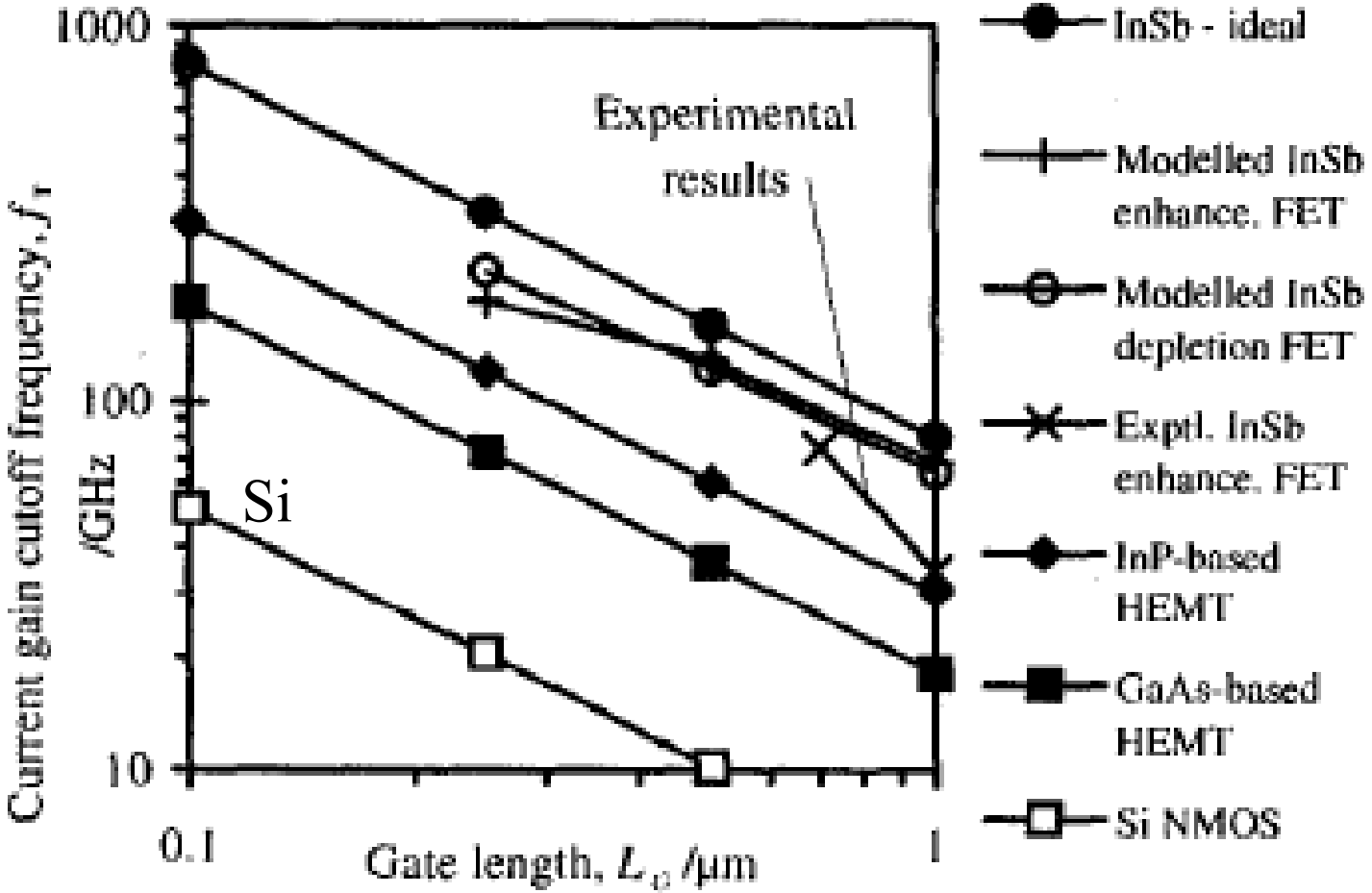
Therefore, armchair (n,n) always metallic, zigzag $(n,0)$ metallic when n = multiple of 3, semiconducting otherwise.

Now you see how challenge it is to get all tubes to have the same band gap.

An alternative is semiconductors in which electrons travel faster.
(If our goal were only to make the device faster.)

But economics is in the driver's seat…

$f_T = v_{sat}/(2\pi L)$



Ashley *et al*, IEEE IEDL '97, 751 (1997).

Reading: Ye, III-V MOSFETs (posted on course website).

Happy scaling (long ago)

↓

Scaling driven by density, cost

↓

New Si MOS structures: FinFETs, nanosheet FETs

↙ ↘

Alternative 3D semiconductors for MOSFETs?
(Higher materials performance so we don't have to scale so aggressively)

Low dimensional semiconductors for MOSFETs?
(Inherently provide better electrostatic control)

Alternative devices, architectures, systems???

Invitation To Enter the NANO-World: Information on a small scale

There's Plenty of Room at the Bottom
An Invitation to Enter a New Field of Physics
by Richard P. Feynman
December 29th, 1959

Why cannot we write the entire 24 volumes of the Encyclopedia Brittanica on the head of a pin?

A future filled with tiny, molecule-sized computers-fast and powerful enough to do things like translate conversations on the fly or calculate complex climate models-may be closer than people think…
American Association for the Advancement of Science (AAAS), Annual Meeting (Boston, February, 2002)