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Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices

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ABSTRACT

It is well-known that conventional field effect transistors (FETs) require a change in the channel potential of at least 60 mV at 300 K to effect a change in the current by a factor of 10, and this minimum subthreshold slope *S* puts a fundamental lower limit on the operating voltage and hence the power dissipation in standard FET-based switches. Here, we suggest that by replacing the standard insulator with a ferroelectric insulator of the right thickness it should be possible to implement a step-up voltage transformer that will amplify the gate voltage thus leading to values of *S* lower than 60 mV/decade and enabling low voltage/low power operation. The voltage transformer action can be understood intuitively as the result of an effective negative capacitance provided by the ferroelectric capacitor that arises from an internal positive feedback that in principle could be obtained from other microscopic mechanisms as well. Unlike other proposals to reduce *S*, this involves no change in the basic physics of the FET and thus does not affect its current drive or impose other restrictions.

It is generally accepted that the ongoing scaling of field effect transistors (FETs, see Figure 1) will be eventually limited by the inability to remove the heat generated in the switching process,[1−4] making it very important to find ways to reduce the power dissipated per switching event. It is also clear that the power dissipation would be lowered significantly, if FETs could be operated at lower voltages. A key factor limiting the operating voltage is the subthreshold swing *S*, which is the inverse of the change of current that can be obtained for a unit change in gate voltage, V_g:

$$S \equiv \frac{\partial V_g}{\partial(\log_{10} I)} = \frac{\partial V_g}{\underbrace{\partial \psi_s}_{\equiv m}} \frac{\partial \psi_s}{\partial(\log_{10} I)} \qquad (1)$$

Standard FET analysis shows that the second term $\partial\psi_s/\partial(\log_{10} I)$ relating the change in the current to the change in the surface potential in the channel cannot be any lower than 60 mV/decade at room temperature. Since V_g and ψ_s are related by a capacitive voltage divider as shown in Figure 1, it is apparent that the first term $\partial V_g/\partial\psi_s$ (often called the body factor "*m*") given by

$$\frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_s}{C_{ins}} \qquad (2)$$

must exceed one, thus putting a lower limit of 60 mV/decade

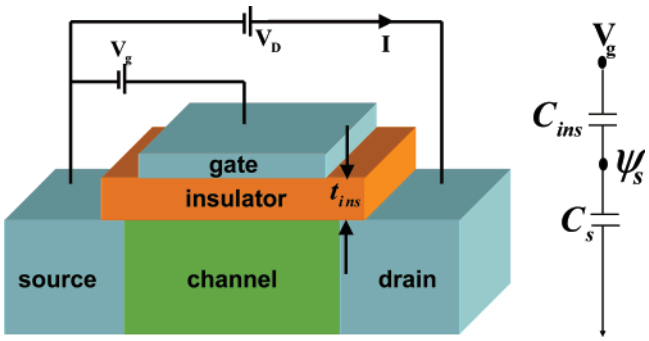

Figure 1. A standard FET structure where the current *I* in the drain circuit is controlled by the gate voltage V_g. The right panel shows an equivalent circuit for the division of the gate voltage between the insulator capacitance and the semiconductor capacitance (that comprises of the depletion, channel to source and channel to drain capacitances).

(corresponding to $m = 1$) on the subthreshold slope *S*. Even high-κ insulators[5] with phenomenally large values of C_{ins} can only reduce the body factor *m* so as to approach one, but cannot make it any smaller.

The objective of this paper is to show that if we replace the conventional insulator with a ferroelectric insulator, having a *P*−*E* (polarization versus electric field) characteristic of the type shown in Figure 2, it should be possible to obtain $\partial V_g/\partial\psi_s < 1$ and hence a value of *S* lower than 60 mV/decade. This can be understood from eq 2 by noting that the ferroelectric capacitor is effectively a negative one because the slope of *P* versus *E* (which is a scaled version of *Q* versus *V*) around the origin is negative (see for example

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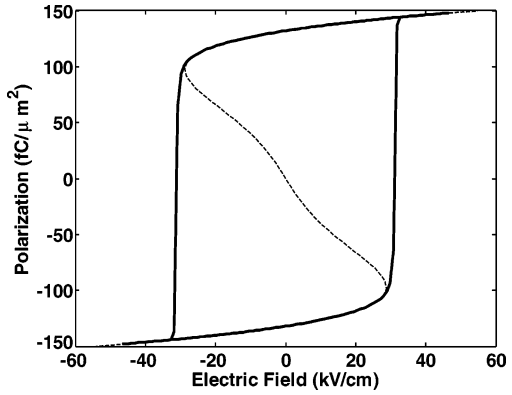

Figure 2. Polarization vs electric field for a typical ferroelectric material calculated from the LK equation (see eq 1) using parameters appropriate for $BaTiO_3$: $\alpha = -1e7$ *m/F*, $\beta = -8.9\ e8$ $m^5/F/coul^2$, $\gamma = +4.5e10$ $m^9/F/coul^4$.[15] The dashed line shows the negative d*P*/d*E* region that is normally unstable but is effectively stabilized when placed is series with a normal capacitor.

ref 22). Ordinarily this negative slope segment is unstable and not directly observed in experiments that exhibit hysteretic jumps in the polarization. But we argue below that if the ferroelectric capacitor is placed in series with a normal capacitor, the negative capacitance segment can be effectively stabilized making it possible for the channel potential ψ_s on an internal node to change more than the voltage V_g applied externally, thus providing a voltage amplifier or more correctly, a step-up voltage transformer. Although we use ferroelectrics to illustrate the concept, we show below that negative capacitance generally arises from a positive feedback that could in principle be obtained through other microscopic mechanisms as well.

Note that our proposal to reduce the first term in eq 1 (that is, the body factor, *m*) is very different from other proposals to reduce *S* that usually assume that *m* cannot be reduced below one and instead seek to improve the second term ($\partial\psi_s/(\log_{10} I)$) by using a different transistor operating principle such as band-to-band tunneling[6] or impact ionization[7] leading to different current and voltage requirements that may offset the advantage gained in *S*. By contrast our proposal requires no change in the basic transistor operation. It simply inserts a step-up voltage transformer in the gate circuit that could help alleviate the device-interconnect "voltage mismatch" emphasized by Yablonovitch.[8] It should also be noted that our approach is very different from the well-studied field of ferroelectric RAM where the focus is on the memory devices (see for example ref 9 and references therein) and ferroelectic FET where the motivation is to use ferroelectric oxide as a high-κ gate material (see for example ref 10 and references therein).

The negative capacitance in ferroelectrics can be understood in terms of a positive feedback[11] mechanism as follows. Suppose we have a (positive) capacitor C_0 (per unit area) that sees a terminal voltage equal to the applied voltage *V* plus a feedback voltage $\alpha_f Q$ proportional to the charge on the capacitor *Q* (per unit area), such that

$$Q = C_0(V + \alpha_f Q)$$

This yields $Q = C_{ins}V$, where

$$C_{ins} = \frac{C_0}{1 - \alpha_f C_0} \tag{3}$$

Clearly with $\alpha_f C_0 > 1$, we have a negative capacitance that would ordinarily lead to an instability so that the charge would increase until limited by the nonlinear terms that we have neglected so far. If we stabilize the negative capacitor by putting an ordinary capacitor C_s in series such that the overall capacitance $[C_s^{-1} + C_{ins}^{-1}]^{-1}$ is positive, then it follows from eqs 2 and 3 that the body factor

$$\frac{\partial V_g}{\partial \psi_s} = 1 - \frac{C_s}{C_0}(\alpha_f C_0 - 1) \tag{4}$$

can, in principle, be made arbitrarily small showing that the negative capacitance can be used as a voltage transformer that steps up the applied potential of V_g into a channel potential of ψ_s. As long as $C_{eq}^{-1} = C_s^{-1} + C_{ins}^{-1}$ remains positive, the composite ferroelectric-semiconductor system will behave like a normal positive capacitor and C_{eq} will be larger than both C_s and C_{ins}. This means that for a fixed *Q*, the energy dissipated during switching, Q^2/C_{eq} will be much smaller than what it would be if C_s and C_{ins} were both ordinary capacitors.

More generally, we could replace the linear capacitor $Q = C_0(V + \alpha_f Q)$ with a general nonlinear capacitance function $Q = F(V + \alpha_f Q)$, such that

$$V = F^{-1}(Q) - \alpha_f Q$$

Noting that the function F^{-1} is generally odd, we could expand it approximately up to the fifth power (the first term being the inverse linear capacitance $1/C_0$) to write

$$V \approx \alpha_0 Q + \beta_0 Q^3 + \gamma_0 Q^5 + \rho_0 \frac{dQ}{dt} \tag{5}$$

where we have also added a possible resistive drop proportional to the current d*Q*/d*t*. Note that the parameter α_0 equals $(1/C_0) - \alpha_f$ and will be negative if we are in the negative capacitance regime where $\alpha_f C_0 > 1$.

Above we have tried to illustrate the generic role of positive feedback in giving rise to negative capacitance, but it should be noted that eq 5 does not just represent a toy model for ferroelectrics. It can just as well be obtained starting from the state-of-the-art approach for modeling the dynamics of ferroelectric capacitors based on the Landau−Khalatnikov (LK) equation[12−14]

$$\rho \frac{d\vec{P}}{dt} + \nabla_{\vec{P}} U = 0 \tag{6}$$

where

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - \vec{E}_{ext}.\vec{P} \quad (7)$$

is the Gibb's free energy given by the sum of the anisotropy energy and the energy due to the external field E_{ext}, and $\vec{P}$ is the polarization charge per unit area. From eqs 6 and 7

$$E_{ext} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho\frac{dP}{dt} \quad (8)$$

where we have dropped the vector signs assuming the spatial variations to be one-dimensional. It is easy to see that if we set $Q = P$ and $V = E_{ext}t_{ins}$ in eq 8 where t_{ins} is the insulator thickness, we obtain eq 5 with $\alpha_0 = 2\alpha t_{ins}$, $\beta_0 = 4\beta t_{ins}$, $\gamma_0 = 6\gamma t_{ins}$, and $\rho_0 = \rho t_{ins}$.

The plot of the steady-state polarization P versus E_{ext} shown earlier (Figure 2) was obtained from eq 8 setting $dP/dt = 0$ and using parameters typical of $BaTiO_3$: $\alpha = -1e7 m/F$, $\beta = -8.9\ e8\ m^5/F/coul^2$, $\gamma = +4.5\ e10\ m^9/F/coul^4$.[15] The negative slope for small P arises from the negative values of α and β, which get suppressed by the positive γ at larger P values. Note that an ordinary linear dielectric with a dielectric constant ϵ would have a positive $\alpha = 1/2\epsilon$, while $\beta = \gamma = 0$.

Let us now assume that the FET shown in Figure 1 has a ferroelectric insulator rather than an ordinary insulator at the gate. The gate circuit can be assumed to be a series combination of the ferroelectric capacitor and another capacitor that we will call C_s representing semiconductor, channel-to-source and channel-to-drain capacitances. For this series combination, a voltage ψ_s appears across C_s, while the rest $V_g - \psi_s$ appears across the ferroelectric such that both have the same charge Q and we can write

$$\psi_s = Q/C_s \quad (9a)$$

$$V_g - \psi_s \approx \alpha_0 Q + \beta_0 Q^3 + \gamma_0 Q^5 + \rho_0\frac{dQ}{dt} \quad (9b)$$

making use of eq 5. Combining these expressions, we can relate the applied voltage V_g to the potential ψ_s that appears inside the channel:

$$\tau\frac{d\psi_s}{dt} + (1 + a_1)\psi_s + a_2{\psi_s}^3 + a_3{\psi_s}^5 = V_g \quad (10a)$$

where

$$\tau = \rho C_s t_{ins}, \qquad a_1 = 2\alpha C_s t_{ins}, \qquad a_2 = 4\beta {C_s}^3 t_{ins}, \quad \text{and} \quad a_3 = 6\gamma {C_s}^5 t_{ins} \quad (10b)$$

The steady-state ψ_s versus V_g is obtained from eq 10a by setting $d\psi_s/dt = 0$

$$(1 + a_1)\psi_s + a_2{\psi_s}^3 + a_3{\psi_s}^5 = V_g \quad (11)$$

Obviously the nature of the ψ_s vs V_g characteristics will depend on the three coefficients a_1, a_2, and a_3, which are scaled versions of the material parameters α, β, and γ (see eq 10). If the parameter values are such that the nonlinear terms a_2 and a_3 are very small compared to a_1, then the relation between ψ_s and V_g is essentially linear

$$\partial V_g/\partial\psi_s \approx 1 + a_1 \quad (12)$$

This is exactly the same as our earlier result in eq 4, as one might expect because we are neglecting the nonlinear terms. But the point to note is that even if a_2 and a_3 are non-negligible, $(1 + a_1)$ represents the slope close to the origin $\psi_s = 0$, $V_g = 0$ and should be positive if we wish the origin to represent a stable operating point. Using eq 10b for a_1, it is easy to see that the condition $(1 + a_1) > 0$ requires the thickness of the ferroelectric insulator to be less than a critical thickness defined as

$$t_{ins} \le \frac{1}{2|\alpha|C_s} \equiv t_c \quad (13)$$

This condition ensures that the ferroelectric capacitor is large enough (or the series capacitor C_s is small enough) that the combination forms a stable positive capacitor, and there is no hysteresis at the origin unlike Figure 2, which corresponds to a very thick ferroelectric. All results we present below assume $t_{ins} < t_c$, because a hysteresis at the origin seems undesirable for device applications.

Figure 3 shows ψ_s versus V_g for different values of t_{ins}, obtained directly from eq 11 using appropriate values of α, β, and γ for $BaTiO_3$, in series with a linear capacitance $C_s = 100\ fF/\mu m^2$.[16] The plots are obtained starting from an initial state with the ferroelectric capacitor fully negatively polarized, sweeping the voltage toward the positive maximum, and then sweeping it back again to the negative maximum. Each point is obtained by solving the full time dependent equation (eq 9) and then finding ψ_s as the system reaches a steady state. Note that the insulator thicknesses we use are less than the critical thickness, which is around 500 nm for this choice of parameters.

As the insulator thickness is increased, the plots become progressively steeper but at the same time, they start to show more and more hysteresis away from the origin (but not at the origin) due to the nonlinear terms a_2 and a_3. Figure 4 shows the corresponding plots for $\Delta\psi_s/\Delta V_g$ as a function of insulator thicknesses for a change in V_g from 0 to 0.2 V. Note that in this voltage range the actual $\partial\psi_s/\partial V_g$ for specific voltages is many times larger than $\Delta\psi_s/\Delta V_g$. Figure 4 shows that with $t_{ins} = 250$ nm, a voltage gain >4 is possible resulting in a channel potential $\psi_s > 0.8$ V for an applied gate voltage V_g of 0.2 V. Figure 3 shows that with this insulator thickness there is a hysteresis in ψ_s versus V_g (away from the origin), but it is small. In general, a trade off may be needed between steepness and hysteresis, unless materials can be engineered to minimize the nonlinear term β relative to the linear term α so as to avoid hysteresis even at large steepness (see Supporting Information).

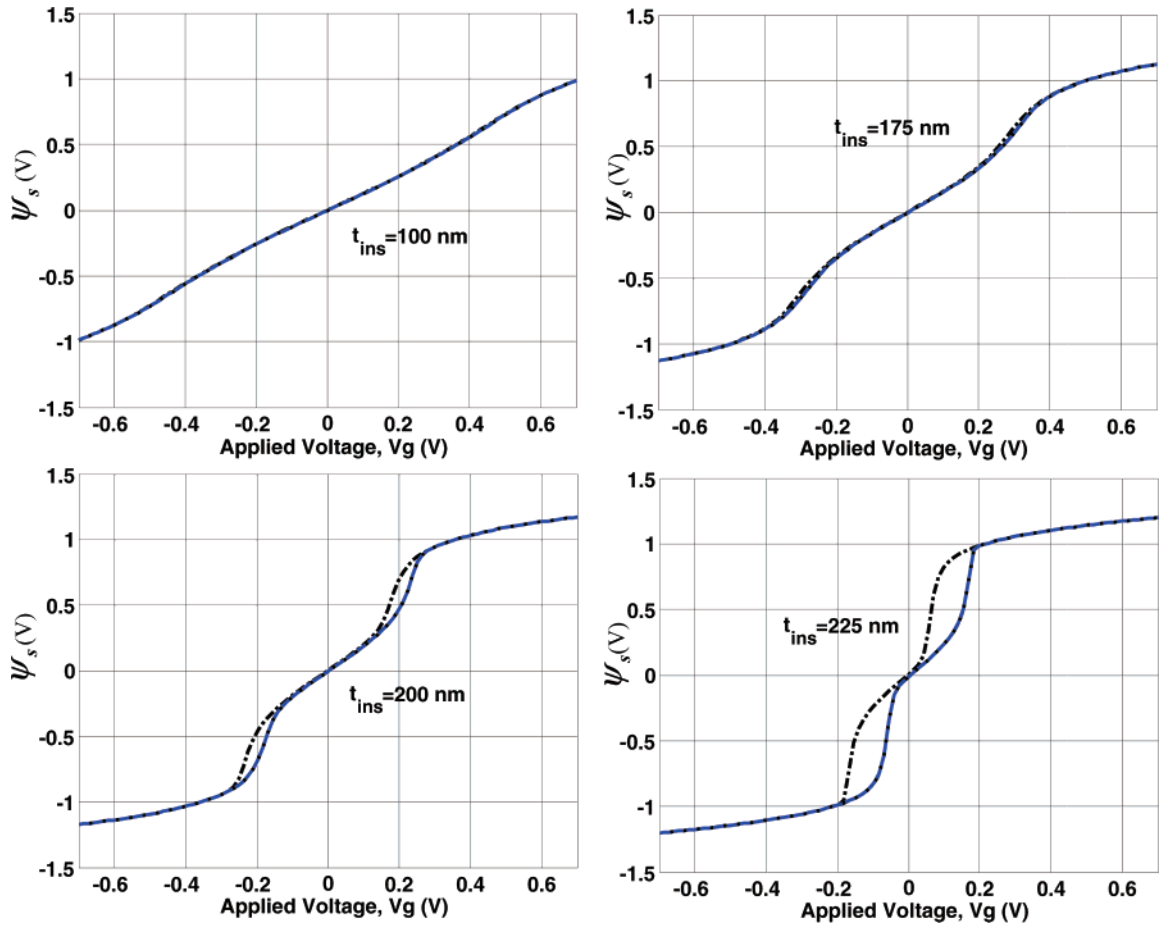

Figure 3. The ψ_s vs V_g plots for different insulator thicknesses. The blue (solid) lines show the sweep from negative to positive voltage and the black (dashed) curve shows the sweep from positive to negative. As the insulator thickness is increased, slope of ψ_s vs V_g becomes increasingly steeper and at some point it starts to open up a hysteresis. For an even larger thickness (not shown) the ψ_s vs V_g plots will no longer pass through origin and resemble a conventional ferroelectric hysteresis curve. Note the similarity of these theoretical plots for $BaTiO_3$ in series with a normal capacitor C_s with the experimental plots in ref 17 (Figure 1) for $BaTiO_3$ raised to temperatures above its $T_c \sim 107$ C.

It will be noted from eq 10 b that if C_s were smaller, the nonlinear terms a_2 and a_3 would become smaller in comparison to the linear term a_1 making the hysteresis negligible in our voltage range of interest. The value for C_s that we have used in this paper is more appropriate for ultrasmall FETs[16] where the short channel effects are significant. For a present day commercial device, the value of C_s should be roughly a factor of 10 lower than that used in this paper and as such should show steep ψ_s versus V_g with negligible hysteresis. However, because the critical thickness is inversely proportional to C_s (see eq 12), the thickness of the ferroelectric insulator will have to be roughly a factor of 10 larger than those shown in Figure 3.

The voltage amplification we are discussing here arises from an internal interaction commonly described by the Landau theory in terms of a free energy functional. Such interactions are quite general in metal oxides and commonly lead to the development of a spontaneous order parameter below a transition temperature. For example, the giant enhancement of longitudinal piezoelectric response recently modeled using the Landau−Ginzburg−Devonshire theory[21] can be attributed to similar mechanisms, The precise correspondence between the effective field in the Landau approach (eq 8) and the effective voltage in a capacitor with positive feedback (eq 5) suggests that any microscopic

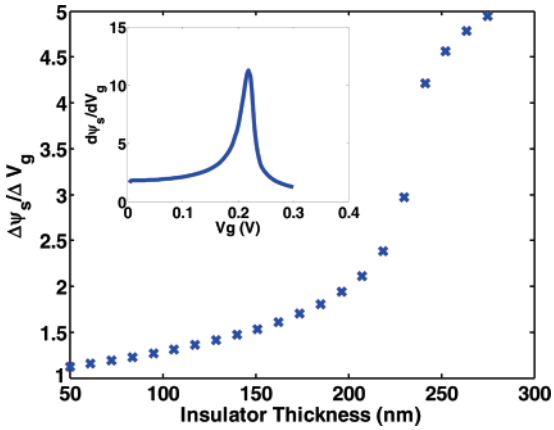

Figure 4. $\Delta\Psi_s/\Delta V_g$ calculated from Ψ_s/V_g at $V_g = 0.2$ V, as a function of insulator thickness. In this manner, the $\Delta\Psi_s/\Delta V_g$ reflects the total change of Ψ_s for an applied $V_g = 0.2$ V. The hysteresis starts to manifest itself around 200 nm. It is evident that with a little bit of hysteresis a huge gain in $\Delta\Psi_s/\Delta V_g$ is possible. Note that the actual $d\Psi_s/dV_g$ for specific voltages is many times more than $\Delta\Psi_s/\Delta V_g$ in this voltage range. Inset shows $d\Psi_s/dV_g$ for $t_{ins} = 225$ nm.

mechanism that can provide the necessary positive feedback can be used to implement a step-up voltage transformer that would allow low-voltage/low-power operation of conventional FETs. For a ferroelectric capacitor, it is the dipole interaction that provides the positive feedback. Other mechanisms such as avalanche breakdown, polaronic effect, etc. within the oxide can possibly provide the positive feedback needed for negative capacitance as well. The parameters α_0, β_0, γ_0, and ρ_0 in eq 5 will be determined by the specific mechanism involved.

Negative capacitance regions (as in Figure 2) are ordinarily unstable and not observed in experiments. But placing such a capacitor in series with a positive capacitor stabilizes it by making the effective α of the composite capacitor positive, provided its thickness is less than the critical thickness defined in eq 12. Because α is proportional to $(T - T_c)$ with T_c being the Curie temperature, the series combination acts like a ferroelectric at a temperature above its T_c. Indeed the plots in Figure 3 look very similar to the experimental results reported for P versus E in the classic work of Merz (ref 17, see Figure 1) for ferroelectrics at temperatures around T_c.

The LK equation used in this paper assumes a single domain ferroelectric insulator. However, the effect is not limited to single domain ferroelectric materials. Rather, any ferroelectric material showing a "run-away" effect in switching, such that once a domain is nucleated the others follow suit, should show similar negative capacitance effect. It is the run-away process or positive feedback that is important for the negative capacitance to manifest itself. In fact, the values of α, β, and γ that we have used in this paper were extracted by Merz[17] by fitting eq 7 to experimental data where the switching was clearly mediated by domain nucleation. In general, materials with α large enough to make β negligible are preferred as their behavior will approach the ideal negative capacitance described by eq 4.

It is evident from eqs 10 and 12 that the time scale for switching is theoretically given by $\tau = \rho C_s t_{ins} \leq \rho/2|\alpha|$. Experimentally, intrinsic switching times of the order of 70∼90 ps have been reported,[18] but it remains to be seen how much the speed can be improved by appropriate materials engineering.

In a recent paper,[19] we used the Landau−Lifshitz−Gilbert equation to show that it should be possible to switch a collection of N interacting spins that act in concert with considerably less energy than that needed to switch N noninteracting spins. A similar physics is possibly at work here with the dipoles in a ferroelectric acting in unison leading to a reduction in the switching energy.

To conclude, we have shown that it should be possible to reduce the subthreshold swing of a FET below the theoretical limit of 60 mV/decade by using a ferroelectric insulator in the gate. The ferroelectric provides a negative capacitance that should make it possible to implement a step-up voltage transformer reducing the subthreshold swing below 60 mV/decade limit, enabling low-voltage/low-power operation. This negative capacitance is a result of the positive feedback among the electric dipoles in the ferroelectric and in principle can be obtained from other microscopic principles as well.

Note Added in Proof: A recent experiment[23] has shown that $BaTiO_3$ can have a negative stiffness which can be stabilized by combining with positive stiffness materials and a huge amplification of total stiffness was observed. This is a mechanical analog of the effect proposed here. This shows that there is no fundamental reason why an inherently unstable system can not be stabilized. In our analysis, we have used a 1-D treatment which should be adequate as $BaTiO_3$ at room temperature is usually in a tetragonal phase.[24] Nevertheless, for a real MOSFET it is important to consider the field distribution in 2-D. This is currently under investigation.

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Supporting Information Available: The support information includes (i) a load line description of the problem and (ii) the behavior of the device as a function of ferroelectric parameters.

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