Chapter 1

Introduction

During the last decade, imaging with semiconductor devices has been continuously replacing conventional photography in many areas. Among all the image sensors, the charge-coupled-device (CCD) is the dominant technology for both user and industry applications. CCD sensors provide higher resolution, wider dynamic range, and higher sensitivity, with which conventional photography can not compete. However, CCD sensors also cost more. For example, a conventional film-based mammography unit costs $50,000 - $90,000, while digital mammography costs over $400,000 [Hindus 99]. To make it worse, some applications like medical imaging require both high resolution and large area, which can be even more expensive. How to achieve large area and high resolution, while at the same time remaining cost-effective is an issue that draws a lot of concern. Since the cost of a sensor is strongly related to the number of defects in the device, defect-free devices are much more expensive than devices with only a few defects. Thus using software methods to compensate for the defects to reduce the overall system cost becomes a practical and economic approach.

Before the discussion of our high resolution, large area imaging system, this chapter first reviews the state-of-the-art of different types of image sensors. It then presents the problems with large area sensors and evaluates several optional solutions. Optimal restoration algorithms which can achieve high resolution are proposed after a survey of existing restoration algorithms. System components and dissertation organization are outlined at the end of the chapter.

1.1 Solid-State Image Sensors - The State of the Art

In the market of image sensors, the charge-coupled-device (CCD) sensor is the dominant technology. Other emerging technologies include the complementary-metal-oxide-semiconductor active pixel sensor (CMOS APS), the charge-injection-device (CID) sensor, and the amorphous-silicon (a-Si) sensor. In 1996, CCDs captured 92% market share of the worldwide image sensor market. However, emerging technologies are expected to gain acceptance and improve their market share to 21% by 2001 (Fig. 1.1) [O'Rourke 97].

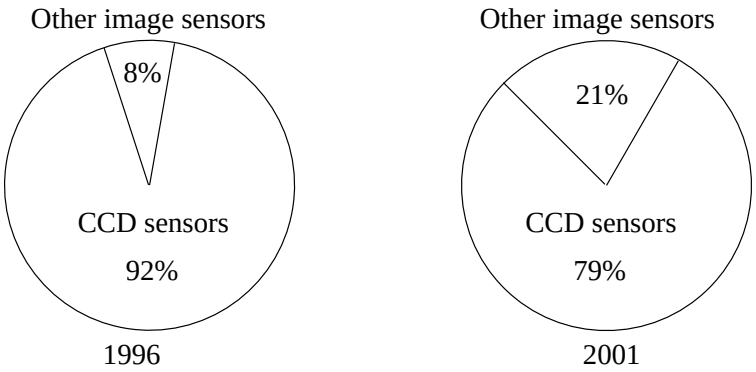


Figure 1.1 Market share of solid-state image sensors.

Solid-state image sensors have many common advantages over traditional film photography. *First of all*, they are faster than film in the sense that they can generate a digital image directly without spending time for film development. *Secondly*, image sensors provide higher sensitivity. Traditional photography records only 0.5% of the light that hits it, that is, the *quantum efficiency* (QE) is 0.5%. While for CCD cameras, QE is up to 90% [Watkins et al. 93]; for a-Si sensors, the peak QE is between 80%-90% at 500-600 nm [Street et al. 98]. *Thirdly*, image sensors are linear which means twice the exposure should record twice as much light. This is definitely not true with traditional photography, especially at extreme exposures. For very short and very long exposures, photographic film is highly nonlinear. A 20-minute exposure in astronomy may have only a little more effect on the film than a 10-minute exposure [Watkins et al. 93]. *Fourthly*, image sensors have a wider dynamic range [Watkins et al. 93] so that they can capture high-quality images.

1.1.1 CCD Sensors

The charge-coupled device (CCD) was invented in 1969 by Boyle and Smith at Bell Laboratories [Boyle and Smith 70]. Conceptually, a CCD image sensor is a two-dimensional array of MOS capacitors that collect and transfer charge generated by photoelectric effect. Each CCD cell (MOS capacitor) is light-sensitive and capable of producing charge in response to the amount of light they receive. By applying a variable voltage to neighboring capacitors, the charge can be transferred (coupled) pixel-by-pixel in a serial fashion to the readout amplifier. Fig. 1.2 is a representative CCD operation of a 3 x 3 array with three gates per pixel [Holst 96].

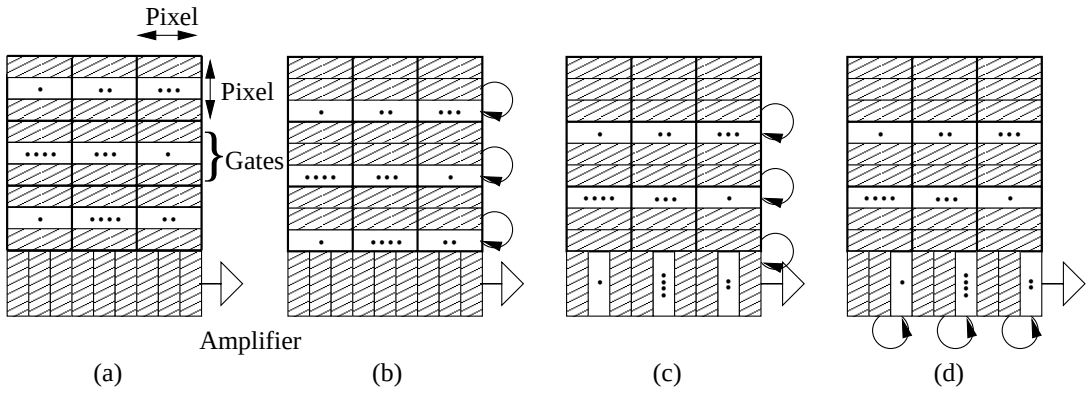


Figure 1.2 A representative CCD operation of a 3 x 3 array with three gates per pixel. (a) The CCD is exposed to light and an electronic image is created. (b) The charges are shifted down in parallel, one gate at a time. (c) Once in the serial horizontal register, the charges are shifted right to the output amplifier. (d) The entire horizontal register must be clocked out before accepting another packet.

The three typical transfer mechanisms for an area image sensor are *full frame transfer* (FFT), *interline transfer* (ILT), and *frame transfer* (FT) [Beynon and Lamb 80][Buil 91], as shown in Fig. 1.3. After integration, the image pixels in FFT array are transferred line-by-line to a horizontal serial register, where the charges are clocked out before the next line can be transferred. FFT usually causes smear, since during the readout process, the capacitors are allowed to continue accumulating the light. One improvement is to use ILT, where the readout regions are interspaced between the imaging regions, and are shielded from the light. At the end of the integration period, the charges are transferred horizontally

to the vertical readout registers in parallel, and then read out line-by-line in a manner similar to FFT. ILT does avoid smear but with the cost of the sensitive imaging areas. Another transfer option is FT, where the array is grouped into two sections: the image section and the storage section. These two sections are identical, except that the storage section is shielded from the light. During the readout, charges are transferred line-by-line into the store by applying same clocking to both sections. Similar horizontal serial register is used to read out each line from the storage section. During the readout of the first frame, a second one can be collected in the image section.

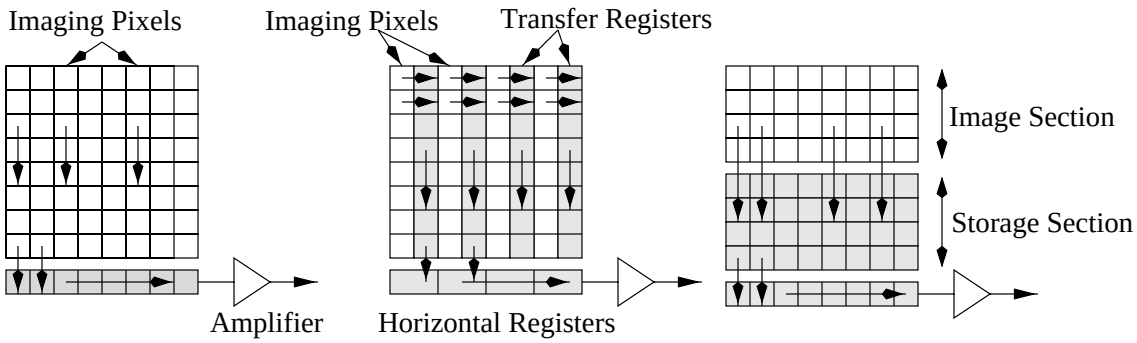


Figure 1.3 Area CCD imager readout mechanisms. From left to right: FFT, ILT, and FT.

The great advantage of the CCD comes from the readout methods described above, where the *actual* collected charge at a pixel site is transferred to the output amplifier, which means there is no unwanted extraneous associated capacitance or resistance to degrade the signal intensity. Therefore, CCD imaging can provide excellent image quality with low noise.

However, this readout method also brings problems. The charges must go all the way down to the one amplifier at the corner which requires perfect silicon crystal quality in order to achieve high charge transfer efficiency (CTE). Since the CCD is essentially a capacitive device, in order to achieve high CTE, it also requires external control signals and large clock swings (5 to 15 V) [Haystead 98]. These off-chip circuits dissipate large amounts of power. Other disadvantages of CCD readout method include: *fixed readout sequence*; *blooming* that happens when CCD cells are excessively illuminated which can cause the accumulated charges spill into adjacent cells, or that the saturated cell can not be

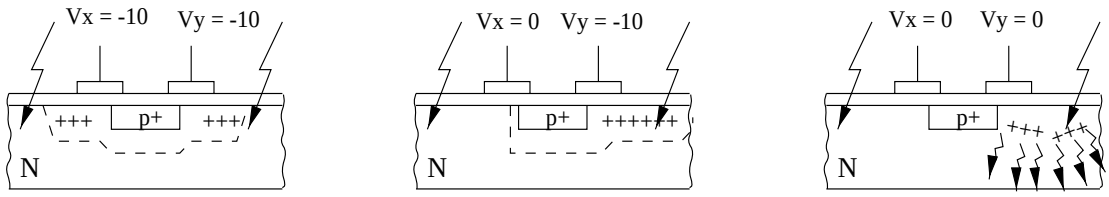
emptied in one or more transfers; *poor yield prospects* due to the fact that if one pixel is bad, all subsequent pixel information that has to be transferred through that bad pixel will be distorted or destroyed causing a partially/complete bad column.

1.1.2 CID Sensors

The charge injection device (CID) was invented in 1973 by Michon at GE [Michon 74]. In [Michon and Burke 80], Michon summarized the CID as “a surface channel device that employs intracell charge transfer and charge injection to achieve the solid-state image sensing function”.

Each CID pixel contains two MOS capacitors, coupled with a diffusion. The two electrodes are placed orthogonal to each other and electrically isolated from their neighbors. The MOS capacitors accumulate light in the same way as CCD pixels do. It is the charge readout mechanism that makes the most difference.

Fig. 1.4 [Michon and Burke 80] shows the cross sections of a pixel site with different values of voltages applied to both electrodes. When the voltages are both negative high, the pixel is in the integration status and the charge is accumulated in the surface inversion region (Fig. 1.4 a); if either of the voltages is removed (goes to zero), the charge stored under that electrode will transfer to the other capacitor through the coupling region (Fig. 1.4 b); if both of the voltages are removed, injection to the substrate will occur to clear the accumulated charge (Fig. 1.4 c). Fig. 1.5 is a typical CID array structure.



(a) Charge Integration (b) Row Readout (c) Injection Readout

Figure 1.4 Cross section of randomly (X-Y) addressable pixel in CID.

The biggest advantage of this arrangement is that it allows pixels to be *randomly accessed* by digital decoders with a certain row and column selection, so that excess charge transfer structure is avoided.

The charge readout can be either *destructive* or *non-destructive*. If charge is sensed by measuring the charge flows upon injection, then the readout process is destructive since the injection clears the charge. If charge is sensed by measuring the voltage change induced by charge transfer between the two capacitors of a pixel, then the readout process is non-destructive. The non-destructive readout allows adaptive exposure control.

The CID imagers are usually fabricated on epitaxial wafers to avoid injection cross talk. The epitaxial CID structure is also resistant to image blooming since each pixel is electrically isolated from its neighbors. The independent pixel structure also makes CID *high yield* since a single defective pixel will not affect other pixels on the same column/ row.

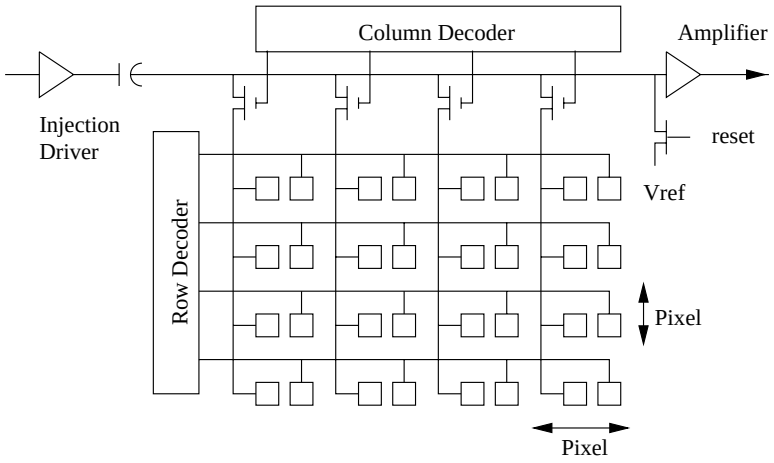


Figure 1.5 A typical CID array structure.

The biggest disadvantage of CIDs compared to CCDs is noise due to the readout method. Michon identified several noise sources in [Michon and Burke 80]. First of all, the readout circuit contains a number of Johnson noise sources, which are usually dominant in large arrays operating at high video rates. The distributed resistance of array lines

used for signal sensing and the line selection switch both contribute temporal noise to the video signal. Also, capacitor reset noise can be significant when certain readout methods are used. Shot noise in the dark current and/or junction leakage current in the MOS line select multiplexers can be significant under certain conditions.

Recent research in CID Technologies Inc. (CIDTEC) [Carbone et al. 93][Wentink and Carbone 94] has reported new CID imagers with low-noise performance, true non-destructive pixel readout, two-dimensional windows (subarray readout), and higher tolerance to radiation (~10^6 gamma).

1.1.3 CMOS APS

The CMOS active pixel sensor (APS) is originally developed in NASA Jet Propulsion Laboratory (JPL) early 1990s [Fossum 93][Mendis and Pain 93]. Since then, an explosion of activity in the area of CMOS image sensors has taken place. The demand for portable, low-power, miniaturized digital imaging systems and the sub-micron photolithography have contributed a lot to the recent emergence of CMOS image sensors [Fossum 98].

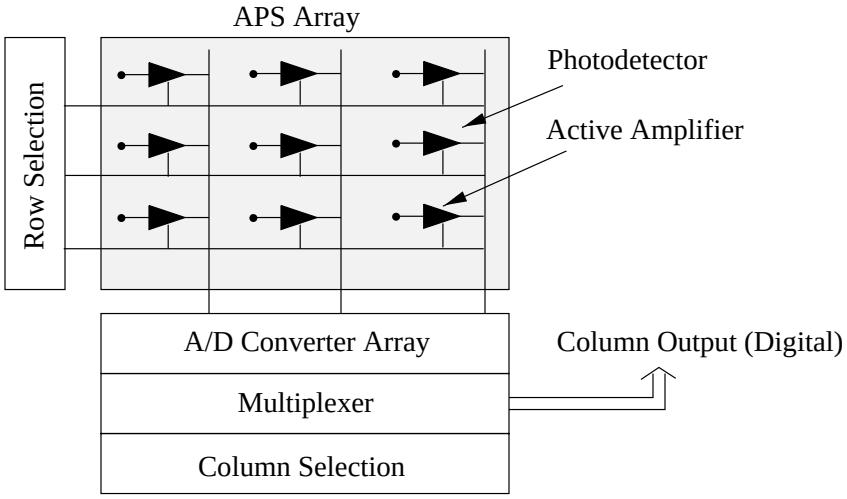


Figure 1.6 CMOS APS structure.

CMOS APS senses light in the same way as CCDs, but beyond that point, everything else is different. APS integrates an amplifier (made from CMOS transistors) at each pixel

Most of the arrays use a-Si:H thin film transistors (TFT) to address pixels. The typical pixel structure is illustrated in Fig. 1.7. The photodiode starts to generate charges when exposed to light. When the “gate” is on, a path is formed from source to drain, through which charges in the photodiode can be read out. It is clear that this readout mechanism allows pixels to be random addressable.

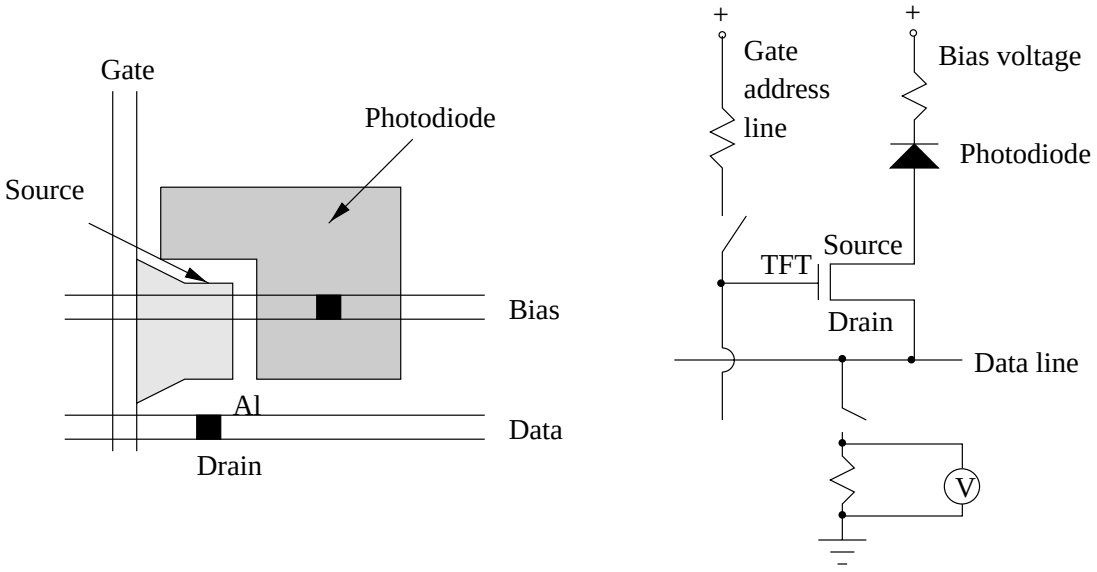


Figure 1.7 A typical imaging pixel using a-Si:H TFT for addressing.

The TFT is required to hold charge on a pixel for the frame time, and transfer the charge quickly when addressed. Even for 60 frame/sec video rate applications, a TFT with a small width-to-length ratio of 2-5 is sufficient. The TFTs also have very low leakage current of <1fA, and can therefore hold the signal charge without loss for very long integration time.

Two major a-Si:H sensor manufacturers are EG&G Amorphous Silicon, and dpiX. *Advanced Imaging* has reported the Senographe 2000D from GE Medical System [Hindus 99], that uses a monolithic flat-panel detector with cesium iodide scintillators over a layer of *amorphous* silicon on a glass substrate. The panel is manufactured by EG&G. The sensor can measure 19 cm x 23 cm with a 100-micron pixel pitch (that is, 100-micron resolution).

site (Fig. 1.6), therefore eliminating the CID capacitance and resistance problems from the array lines. The standard CMOS fabrication techniques can integrate additional functional circuits on the same chip, such as the timing logic and the analog-to-digital converter (ADC). The CMOS design also provides a 100:1 reduction in system power requirements compared to the CCDs.

The photo-generated charge in APS is not transferred, it is instead detected as early as possible by the charge sensing amplifiers. Charge can be read out by simultaneously selecting a row and a column. It then goes through the on-chip ADC, which converts analog signals to digital output.

CMOS APS offers many benefits like lower power, random readout, and ADC and timing fabricated on chip (camera on a chip). However, because of the inherently higher noise of the APS sensors (due to the readout structure), the lower QE (due to the lower fill factor/packing density), and the compromises in semiconductor manufacturing made to incorporate multiple features on a single die, to date APS sensors have only been used for toys and low-end consumer electronics. Although CMOS is generally used to describe a technology family, there are a wide variety of semiconductor processes used to manufacture CMOS devices. Each company tends to focus on optimizing a process to optimize performance for a very specific market niche. This prohibits optimal multi-function CMOS APS devices [Pixel Vision].

From above brief review, we can see that different sensor technologies might be used for different applications. For example, CIDs are more appropriate for use in harsh radiation environment than CCDs and CMOS; CMOS devices are more suitable when portability is a major demand. But due to the mature technology and the lowest noise level of CCDs, they are still the most widely used sensor technology in many areas, especially scientific applications, where high quality is usually required.

1.2 Large Area Sensor Technology (LAST)

Compared to conventional photographic plate, one of the big drawbacks of the above solid-state sensors is the low *spatial resolution*. Spatial resolution is determined by the size of photoelements per pixel. A typical CCD has 512 x 512 pixels, each about 20 x 20 μm^2, providing high resolution, but covering a space of about only $1cm^2$. Large area is particularly significant in some applications like medical and industrial X-ray systems. Neither CCDs, CIDs, nor CMOS APSs can overcome the size restrictions since their size is limited to the size of silicon crystal wafer.

There are three technologies reported so far to solve this problem: Amorphous Silicon (a:Si) sensors, large-area CCDs, and CCD mosaic using butting technology.

1.2.1 Hydrogenated Amorphous Silicon (a-Si:H) Sensors

The a-Si:H technology allows the manufacture of image sensors with much larger active areas than conventional silicon CCDs or photodiode array sensors. Direct 1:1 imaging is achieved by using a scintillator material in contact with the image sensor for converting X-ray radiation to visible light. Since a-Si:H is extremely efficient absorber, only thin layers of such materials are needed to produce the same amount of charge that a thicker layer of a material such as crystalline silicon would produce. (The thickness ratio is about 500:1 for silicon compared with amorphous silicon [Stone 93].) It is also highly resistant to X-ray degradation and can be operated directly in the beam path of an X-ray source.

Starting from the initial devices with 64 x 40 pixels reported by Xerox PARC and dpiX group in 1990, the technology has now progressed to imagers with >7 million pixels and sizes up to 14” x 17”, with excellent image quality. The pixel size in large arrays ranges from 127 micron up to 750 micron. It is also reported [Street et al. 98] that pixel sizes down to at least 80 microns are within the capability of present technology, and can be anticipated within a short time.