Web Appendix K - Sampling Methods

Sampling of electrical signals, usually voltages, is most commonly done with two devices, the *sample-and-hold* (*S/H*) and the *analog-to-digital converter* (*ADC*). Sometimes these two devices are packaged together in one electronic module. The input signal of the S/H is the analog voltage at its input and when the S/H is clocked, it reproduces that voltage as its output signal and holds that voltage until it is clocked to acquire another voltage (Figure K-1).

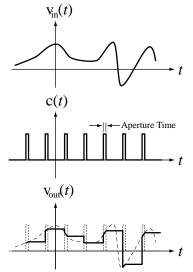


Figure K-1 Operation of a sample-and-hold

In Figure K-1 the signal c(t) is the clock signal. The acquisition of the input voltage signal of the S/H occurs during the *aperture time* which is the width of a clock pulse. During the clock pulse the output voltage signal very quickly moves from its previous value to track the input voltage signal. At the end of the clock pulse the output voltage signal is held at a fixed value until the next clock pulse occurs.

An ADC accepts an analog voltage or current at its input and converts it into a set of binary bits (often called a *code*). The ADC output signal can be serial or a parallel. If the ADC has a serial output signal, it produces on one output pin a single output signal voltage or current that is a timed sequence of high and low voltages representing the 1's and 0's of the set of binary bits. If the ADC has a parallel output signal there is a output signal voltage or current for each bit and each bit appears simultaneously on a dedicated output pin of the ADC as a high or low voltage or current representing a 1 or a 0 in the set of binary bits (Figure K-2).

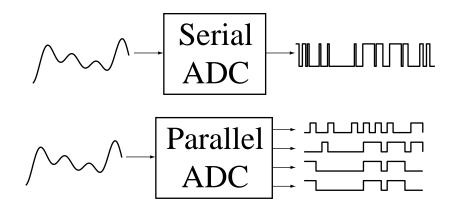


Figure K-2 Serial and parallel ADC operation

Usually an ADC is preceded by a S/H to keep its input signal constant during the conversion time.

The input signal to the ADC is a continuous-time signal and the output signal is a discrete-time signal. Not only is the output signal of the ADC discrete-time but it is also quantized and encoded. The number of binary bits produced by the ADC is finite. Therefore the number of unique bit patterns it can produce is also finite. If the number of bits the ADC produces is n, the number of unique bit patterns it can produce is 2^n . Quantization is the effect of converting a continuum of (infinitely many) input signal values into a finite number of output signal values. Since the output signal has an error due to quantization, it is as though the signal has noise on it and this noise is called quantization noise. If the number of bits used to represent the output signal is large enough, quantization noise is often negligible in comparison with other noise sources. After quantization the ADC encodes the signal also. Encoding is the conversion from an analog voltage to a binary bit pattern. So the input signal to an ADC is an analog (CT) voltage and the output signal is a sequence of binary numbers (or codes). The relation between the input and output signals of an ADC whose input voltage signal voltage range is $-V_0 < v_{in}(t) < +V_0$ is illustrated in Figure K-3 for a 3-bit ADC. (A 3-bit ADC is rarely, if ever, actually used but it does illustrate the quantization effect nicely because the number of unique bit patterns is small and the quantization noise is large.)

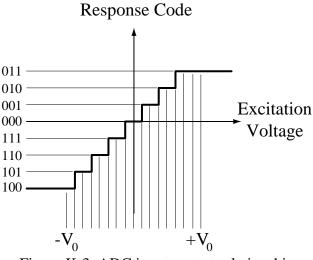


Figure K-3 ADC input-output relationship

The effects of quantization are easy to see in a sinusoid quantized by a 3-bit ADC (Figure K-4).

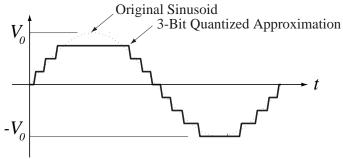


Figure K-4 Sinusoid quantized to 3 bits

When the signal is quantized to 8 bits the quantization error is much smaller (Figure K-5).

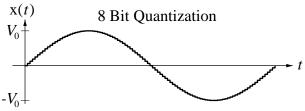


Figure K-5 Sinusoid quantized to 8 bits

The opposite of analog-to-digital conversion is obviously digital-to-analog conversion and the device that does that is called a *digital-to-analog converter (DAC)*. A DAC accepts binary bit patterns as its input signal and produces an analog voltage as its output signal. Since the number of unique bit patterns it can accept is finite, the DAC output signal is an analog voltage that is quantized. The relation between input signal and output signal for a 3-bit DAC is shown in Figure K-6.

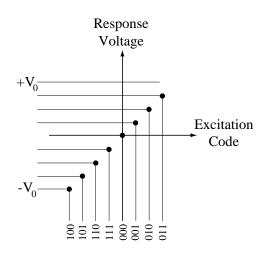


Figure K-6 DAC input-output relationship

In the material to follow, the effects of quantization will be not be considered. The model for analyzing the effects of sampling will be that the sampler is ideal in the sense that the output signal's quantization noise is zero.

In Chapter 11 we introduced the idea of sampling a signal by multiplying a pulse train by the signal and then extended the concept to impulse-sampling (Figure K-7).

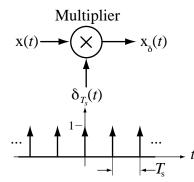


Figure K-7 An impulse modulator producing an impulse-sampled signal

The CTFT of the impulse-sampled signal in Figure K-7 is

$$\mathbf{X}_{\delta}(f) = \mathbf{X}(f) * (1/T_s) \delta_{1/T_s}(f) = f_s \mathbf{X}(f) * \delta_{f_s}(f)$$

We then showed that if a bandlimited signal is impulse-sampled for all time at a sampling rate that is more than twice the bandlimit of the signal, the original signal can be exactly reconstructed. This statement is called the sampling theorem. In the section which follows we will explore these ideas in more depth and develop the sampling theorem based directly on a discrete-time signal formed from a continuous-time signal by sampling instead of being based on impulse-sampling which, as a practical matter, cannot be done.