A High-Temperature, High-Voltage SOI Gate Driver IC with High Output Current and On-Chip Low-Power Temperature Sensor

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Abstract

High-temperature power conversion modules (DC-DC converters, inverters, etc.) have enormous potential in extreme environment applications, including automotive, aerospace, geothermal, nuclear, and well logging. Power-to-volume and power-to-weight ratios of these modules can be significantly improved by employing Silicon Carbide (SiC) based power switches (MOSFET or JFET). Wide bandgap material such as SiC is capable of much higher temperature operation than conventional Silicon based power devices. For successful realization of such high temperature power conversion modules, associated control electronics also need to perform at high temperature. This paper presents a Silicon-on-Insulator (SOI) based high-temperature, high-voltage gate driver integrated circuit (IC) with improved peak output current drive over previous work as well as an on-chip low-power temperature sensor. This driver IC has been primarily designed for automotive applications where the under hood temperature can reach 200°C. This new gate driver prototype has been designed and implemented in a 0.8-micron, 2-poly, and 3-metal Bipolar-CMOS-DMOS (BCD) on SOI process and has been successfully tested up to 200ºC ambient temperature driving a SiC MOSFET or a SiC normally-ON JFET. In this design, the peak output current capability of the driver is 5 A and is thus capable of driving several power switches connected in parallel. An ultra low-power on-chip temperature supervisory circuit has also been integrated into the die to safeguard the driver circuit against excessive die temperature (≥ 220°C). This approach utilizes the increased diode leakage current at higher temperature to monitor the die temperature. Up to 200°C, the power consumption of the proposed temperature sensor circuit is below 10 µW.

Key Words: High-temperature, gate driver, temperature sensor, silicon-on-insulator.

I. High Temperature Electronics in Automotives

Operation of most integrated circuits (ICs) used in consumer electronics and industrial electrical systems are limited to a narrow operating temperature range of −55°C to 125°C. Fig. 1 shows the temperature range for different classes of commercially available ICs. Operation of electronics outside the traditional temperature range is typically defined as extreme temperature operation. This covers both the very low temperatures, down to absolute zero (0 K), and the high temperatures, anything above +125°C. Electronic devices and circuits are exposed to high temperature in a variety of applications under various environmental conditions. Integrated solid-state electronics capable of operation at ambient temperatures higher than 150°C without external cooling have tremendous potential in the automotive, aerospace, well-logging, nuclear, and geothermal energy production industries.

The Automotive industry is often considered as the primary and the largest near-term market for high-temperature electronics. This industry is developing hybrid electric vehicles (HEVs), plug-in hybrid electric vehicles (PHEVs), and all electric vehicles (EVs) to achieve better fuel efficiency compared to the traditional internal combustion engines [1]. The volatile nature of gasoline prices and the potential shortage of supply in the future are creating a growing demand for the development of

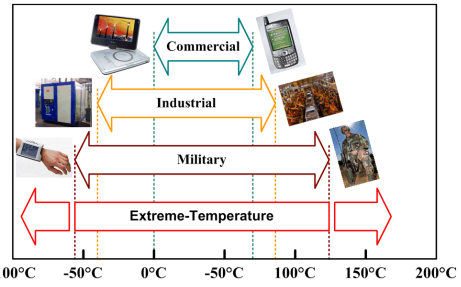

Fig. 1. Operating temperature range of semiconductor ICs.

electric vehicles. Research in the hybrid automobile industry has generated an enormous need for different power electronic modules (such as DC-DC converters and DC-AC inverters) for bidirectional power conversion between the energy storage units (battery or ultracapacitor) and the traction system [2, 3].

Ambient temperature under the hood of the automobile is usually above 150°C, and it can even reach 200°C near the engine [4, 5]. Current HEV technologies require a separate 70°C cooling loop for commercially available power electronic circuits which are mostly rated for 85°C ambient temperature. The future goal of the automotive industry is to use the same 105°C cooling loop that is used for the engine to cool the electronics under the hood. By removing the extra cooling unit and by reducing the size of the heat sink, an order of magnitude savings in overall mass and volume of the power electronic modules can be achieved. To minimize the cost and to improve the efficiency of HEVs, there is a pressing demand for miniaturization and weight reduction of the power converter modules. To achieve this goal, electronic circuits capable of operating at higher ambient temperatures (175°C and above) with minimal thermal management are in great demand.

In all power electronic circuits, a gate driver is an essential component to control the turning ON and OFF operation of the power switches. In electric vehicles typically the power converter modules along with the driver circuits are required to be placed under the hood. Hence, the ambient temperature of the electronics inside the power modules will be 150°C or higher. To the best of the authors' knowledge, at present time there is no high temperature (≥ 175°C) gate driver integrated circuit available in market or reported in literature with high current drive capability (> 1 A). This work presents a Silicon-on-Insulator (SOI) based high-temperature, high-voltage integrated gate driver circuit with large current drive. Circuit topology and operation along with test results of the earlier prototype of this SOI gate driver circuit was presented in [6, 7]. In this paper, an improved version of that gate driver circuit is discussed. Design focus of this iteration was to increase the current drive capability and the robustness of the circuit across a wide temperature range. An on-chip low-power temperature sensor circuit is also incorporated with the core gate drive circuit to safeguard it from excessive die temperature.

II. Material Choice for High-Temperature Power Electronics

More than 98% of current electronic devices use silicon (Si) as the semiconductor material [5]. Si-based power devices dominate the power electronics and power system applications. Applications where power devices are required to operate at higher than 150°C junction temperature, high voltages, high switching frequencies, and high power densities are growing. Si-based devices are not able to meet these challenging requirements without expensive cooling systems, which increases the weight and volume of the power converters [8].

Table 1 shows the physical properties of different semiconductor materials [8, 9]. The superior material properties of the wide bandgap (WBG) semiconductors offer a lower intrinsic carrier concentration (10-35 orders of magnitude), a higher electric breakdown field (4-20 times), a higher thermal conductivity (3-13 times), and a larger saturated electron drift velocity (2-2.5 times), when compared to silicon [8]. These properties of WBG semiconductors make them most effective in high-power and high-temperature applications.

Among the WBG materials, Silicon Carbide (SiC) has emerged as an alternative semiconductor to overcome the limitations of silicon especially in extreme environment conditions. SiC device operation at up to 500°C has been reported in the literature [10], whereas Si-based devices can only operate at a maximum junction temperature of 150°C [10, 11]. Hence the SiC-based power switches are expected to be the switch of choice for power electronic circuits in harsh environments where the ambient temperature can exceed 200°C. However, SiC-based power transistors are not yet commercially available in large volumes. In addition, the SiC-based integrated circuit design technology will take even longer time to be commercially available. For low or medium power needs up to 300°C, the solution is Silicon-on-Insulator (SOI) which is commercially available for integrated circuit development [12-14].

Table 1. Semiconductor material properties

Property	Si	GaAs	4H-SiC	GaN
Bandgap (eV)	1.1	1.43	3.26	3.45
Saturation Electron Velocity (x 10^7 s^{-1})	1.0	1.0	2.0	2.2
Electron Mobility (cm^2/V-s)	1500	8500	1140	1250
Hole Mobility (cm^2/V-s)	600	400	50	850
Breakdown (x 10^5 V cm^{-1})	3	6	30	>10
Dielectric Constant	11.8	12.5	9.6	9
Thermal Conductivity (W cm^{-1} K^{-1})	1.5	0.46	4.9	1.3

In high-temperature electronics, junction leakage is a major concern for bulk CMOS processes. This causes higher junction temperature compared to the ambient and potentially leads to the failure of the circuit. Si-based CMOS with reduced OFF-state leakage current for higher temperature operation can be realized by the SOI structure. The buried insulator layer in the SOI structure greatly decreases the leakage path associated with the drain and source p-n junctions. In SOI technology the leakage area of the junction is decreased by a factor of 100 compared to the bulk silicon process [12]. The buried oxide layer also reduces off-state source-to-drain carrier emission leakage that physically occurs deeper in the substrate of the bulk MOSFETs. The threshold voltage variation with temperature is smaller in SOI devices than in the bulk devices [14]. SOI also provides improved latch-up immunity, which ultimately increases the reliability of the circuit operation at higher temperature [14]. These features make SOI-based circuits capable of operating successfully in the 200°C-300°C temperature range. For our work, a process that combines the advantages of high-voltage devices with SOI technology has been chosen for the design and implementation of the high-temperature, high-voltage gate driver circuit.

III. High-Temperature, High-Voltage Gate-Driver IC with Large Drive Current

In any power converters (DC-DC converter, inverter, etc.), the flow of power from the source to the load is controlled by the power switch through its turning ON and OFF operations. The performance of the system highly depends on the characteristics of the switch and the ability of its driver to efficiently turn it ON and OFF. Input pulses to the driver are low power pulses, generated by microcontroller-based system, that can not directly drive the power switch gate. For most cases, voltage magnitude of this logic level signal is lower than the threshold voltage of the power switches and lacks the current drive capability to charge and discharge the gate capacitance fast enough to minimize the switching losses.

At the present time to the best of our knowledge, there is no high temperature gate driver integrated circuit available in market or reported in literature for SiC power switches with large current drive capability. The SOI gate driver circuit developed by Cissoid [15] is rated for −55°C to 225°C junction temperature. However, the peak output current of this driver IC is only 80 mA at 225°C junction temperature. This paper presents the design of a high-temperature (≥ 200°C), high-voltage (10 V to 30 V) gate driver IC with high drive current (5 A) for wide bandgap power switches.

An earlier prototype of the proposed SOI-based high-temperature, high-voltage gate driver circuit was presented in [6, 7]. The design focus of this iteration was to increase the current drive capability and to make the critical functional blocks more robust across a wide temperature range. Several protective features, namely temperature sensor based thermal protection, under voltage lock out (UVLO), and short circuit protection have also been incorporated with the core gate drive circuit.

A block diagram level schematic of the gate driver circuit implemented in this design iteration is shown in Fig. 2. This circuit has seven critical building blocks, namely (1) half-bridge high-voltage output stage (transistor pair M_H and M_L), (2) low-side and high-side buffers, (3) on-chip bootstrap capacitor based charge pump, (4) constant current bias low-side to high-side level shifters, (5) temperature independent dead-time controller, (6) edge detection circuit, and (7) input stage.

The input stage receives the logic control signal from the external source which can be a microcontroller or a DSP board. Logic control units are expected to be placed in a relatively cooler space, far away from the power modules. Often these signals are corrupted by noise. In the SOI gate driver,

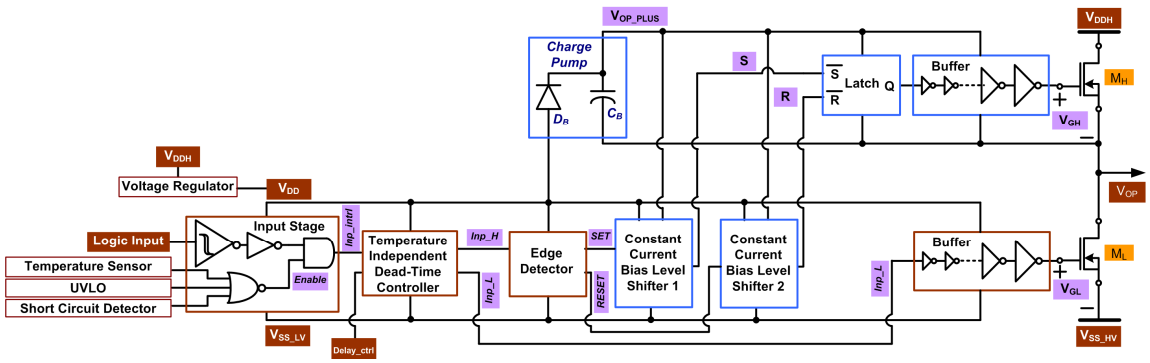

Fig. 2. Schematic of the high-temperature, high-voltage gate driver circuit with high output current.

a Schmitt trigger buffer in the input stage helps filter this noise. The Schmitt trigger design used here has a 2.5-V hysteresis across a wide temperature range (–60°C to 250°C). This input stage also generates an *Enable* signal based on the feedback received from the protection circuits. If any one of the three feedback signals indicates a fault in the system, then the *Enable* signal will become zero, which will force the *inp_intrl* signal going to the dead-time controller circuit to a logic low state. This will make the gate driver output low and the power switch will be turned OFF.

The all-NMOS (M_H and M_L) transistor based half-bridge output stage handles the large drive current requirement of the driver circuit. A large number of 45 V n-type LDMOS devices (each with aspect ratio of $40\ \mu m\ /\ 1.6\ \mu m$) transistors are connected in parallel to form both the M_H and M_L switches within the gate driver. Current sourcing and sinking capabilities of this half-bridge stage are higher than 6 A and 4 A at −50°C and 200°C, respectively. The bootstrap capacitor (C_B) based charge pump establishes a voltage (V_B) above the available highest rail voltage (V_{DDH}) for all the high-side devices and circuits. The dead-time controller circuit generates two non-overlapping copies (*inp_L* and *inp_H*) of the incoming logic signal (*inp_intrl*) with temperature independent dead-time injected between them, which ensures the complementary turn ON and OFF operation of the transistors in the output stage. An edge detector circuit generates two narrow pulses (*SET* and *RESET*) at the rising and falling edges of the *inp_H* signal. The level shifter provides conversion of the incoming narrow pulses (*SET* and *RESET*) from the low-side voltage level to the high-side voltage level. The *S* and *R* signals generated by the level shifter circuits are used to generate a voltage level shifted copy of *inp_H* using a SR latch circuit. The output of the latch circuit and *inp_L* signals are passed through buffers to drive the relatively large capacitances at the gate terminals of the M_H and M_L transistors. Temperature independent design of the dead-time controller and level shifter circuit are discussed in section IV and V, respectively.

IV. Temperature Independent Dead-Time Controller

To reduce the power consumption of the chip and to ensure the reliability of the circuit, it is very important to maintain complementary turning ON and OFF of the high-voltage transistors in the output stage. Overlapping turn-ON of both transistors will create a short circuit between the rail voltages (V_{DDH} and V_{SS}) resulting in large short circuit or "crowbar" current. This large current will increase the die temperature much higher than the ambient temperature. To ensure a break-before-make type operation, a temperature independent dead-time controller circuit has been designed to generate two non-overlapping copies of the *inp_intrl* logic signal. Fig. 3 shows the schematic of the proposed dead-time controller circuit. By applying logic high or low voltages to the *Delay_ctrl* terminal, the dead-time between *inp_H* and *inp_L* can be adjusted..

The main building block of this circuit is the adjustable delay controller circuit that can inject a temperature independent phase lag to an incoming logic signal. A temperature-independent current bias circuit has been designed to provide constant current biasing to the adjustable delay controller circuit. Fig. 4 shows the schematic of the temperature-independent current bias network developed using the zero-temperature coefficient (ZTC) [16] bias conditions of the NMOS and the PMOS transistors. Sizes of M_{P1} and M_{N1} transistors are selected such that their saturation drain-source current at ZTC bias voltage, I_{DS_ZTC} become equal i.e. $I_{bias1} = I_{bias2}$. Since the current through both the PMOS and NMOS current mirror branches are equal, then the drain voltage of M_{N1} transistor tracks the V_{GS_ZTC} voltage of M_{N2} NMOS. Similarly, the drain voltage of M_{P2} tracks V_{SG_ZTC} of M_{P1}. The resistance value required to keep these transistors operating in saturation with the ZTC bias voltages is calculated by:

$$R_{eq} = R_{11} + R_{12} = R_{21} + R_{22} = \frac{(V_{DD} - V_{SS}) - V_{SG\_ZTC} - V_{GS\_ZTC}}{I_{DS\_ZTC}}$$

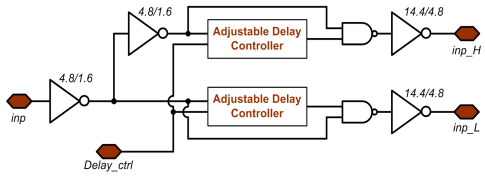

Fig. 3. Temperature independent dead-time controller circuit.

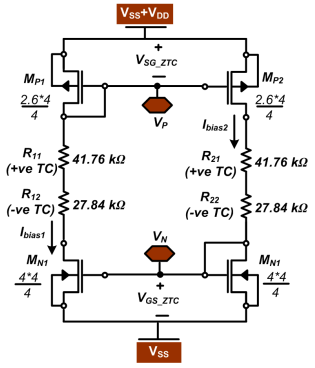

Fig. 4. Schematic of the temperature independent current bias network.

To minimize the net resistance variation with temperature, both positive and negative temperature coefficient resistors available in the SOI process were used. Using this circuit, constant bias voltage V_P for PMOS and V_N for NMOS transistors is generated.

$$V_P = V_{DD} - V_{SG\_ZTC} \quad \text{and} \quad V_N = V_{GS\_ZTC} - V_{SS}$$

Fig. 5 shows the DC simulation of this bias network from −60°C to 250°C temperature. Bias currents in both branches are exactly the same and vary less than 2 µA over the 310°C temperature sweep. V_N and V_P voltages are almost constant across the temperature range. Fig. 6 shows the schematic of the adjustable delay controller circuit with the temperature independent bias network. Constant bias voltage V_P is supplied to the gates of all the PMOS transistors, which source constant pull-up currents to the inverters, and thus capacitors get charged by a constant current across the entire temperature range. Similarly, the constant bias voltage V_N is provided to all the NMOS transistors, which sink the constant pull down current from the inverters. This ensures the same rate of discharge of the capacitors over temperatures. Since the capacitors get charged and discharged by constant currents for the entire temperature range, hence the phase shift injected by this circuit remains virtually constant over temperature. The dead-times achieved between the non overlapping copies generated by the dead-time controller at different temperatures are shown in Table 2.

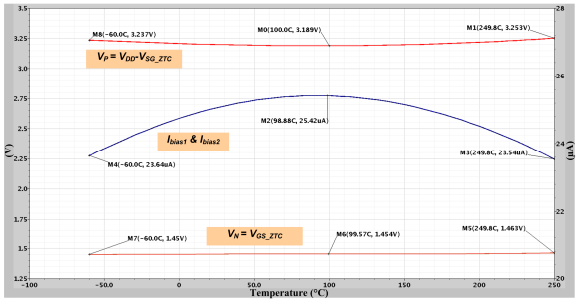

Fig. 5. DC simulation results of the temperature independent bias network.

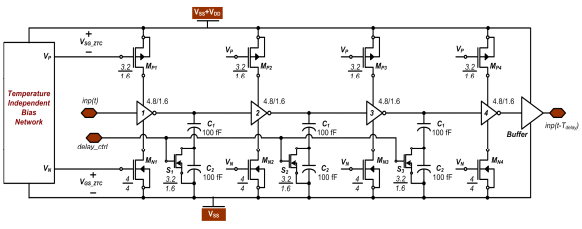

Fig. 6. Schematic of the temperature independent adjustable delay controller circuit.

V. Constant Current Bias Level Shifter Circuit

The level shifter circuit converts the logic level pulses (*SET* and *RESET*) into currents, and then in the high-voltage side converts this current back into a voltage signal referenced to the high-side voltage. For the all-NMOS transistor based half-bridge implemented in this work, the level translation is from (V_{SS} ~ V_{SS}+V_{DD}) to (V_{OP} ~ V_{OP}+V_B). The source terminal of the M_H transistor is connected to the output terminal (V_{OP}). Therefore, its gate voltage needs to be either at V_{OP} (to turn it OFF) or at $V_{OP\text{-}PLUS}$ = V_{OP} + V_B (to turn it ON). Two constant current bias level shifter circuits are used to generate *S* and *R* signals from the *SET* and *RESET* pulses, respectively, generated by the edge detector circuit.

Fig. 7 shows the schematic of the constant current bias level shifter circuit incorporated in this iteration of the gate driver circuit. The I_{bias3} current in the right most branch creates a voltage drop across R_{31}+R_{32} that works as the active low *S* or *R* signal for the SR latch. If I_{bias3} varies with temperature, then the magnitude will also vary. If the current is too low, then the voltage might not be sufficiently large to trigger the latch; and, if it is too large, then this voltage drop may exceed the gate-source breakdown voltage limit of the MOS devices in the latch circuit. Hence, it is critical to maintain constant current flow through this branch in response to the *SET* or *RESET* pulses. This constant current bias is guaranteed through the ZTC biasing of the PMOS and NMOS current mirrors as shown in Fig. 7. Resistors in all three branches are constructed by a combination of positive and negative temperature co-efficient resistors to ensure fixed voltage drop across them over the entire temperature range.

This level shifter circuit consumes power only when the *SET* or *RESET* pulses are applied in the M_{SW} switch. The duty cycle of these pulses is only 0.04%. Therefore the average power consumption of this circuit is very small. Diodes D_1 to D_3 and transistor M_C work as a voltage clamping circuit to protect against transient voltage spikes across R_{31}+R_{32}.

Table 2. Dead-time at different simulation temperatures.

delay_ctrl	C_{eq} (*fF*)	Dead-time (ns)			
		-60°C	**100°C**	**175°C**	**250°C**
"High"	100	190	180	180	200
"Low"	50	110	110	110	140

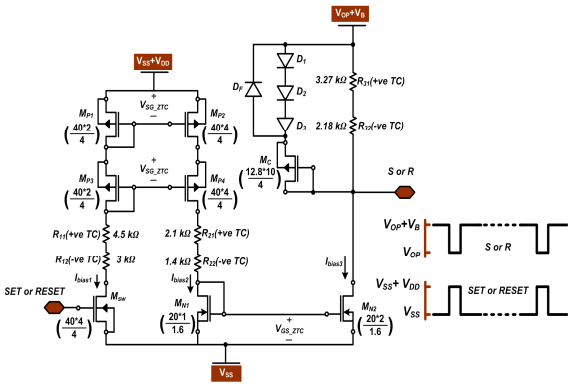

Fig. 7. Schematic of the temperature independent level shifter circuit.

Diode D_F is the free wheeling diode for the voltage clamp circuit.

VI. Ultra Low-Power Temperature Supervisory Circuit

An ultra low-power temperature supervisory circuit has been designed to protect the proposed high-temperature gate driver circuit. Most often on-chip temperature sensors use the base-emitter voltage difference between two substrate PNP transistors (thermal diode) of the same size, which are forward biased by two different DC currents, usually in the range of hundreds of micro amperes [17-20]. One drawback of this approach is the continuous power loss even when the die temperature is in the normal operating range. These conventional approaches are also restricted to limited operating temperature range (≤130°C).

The temperature sensing scheme proposed in this work utilizes the exponential increase in diode leakage current with the increase of temperature to determine the die temperature. Fig. 8 shows the measured and simulated leakage current variation vs. temperature plot for a p-n junction diode. As this figure shows, the diode leakage current remains negligibly small until the die temperature reaches 150°C and beyond that it increases exponentially.

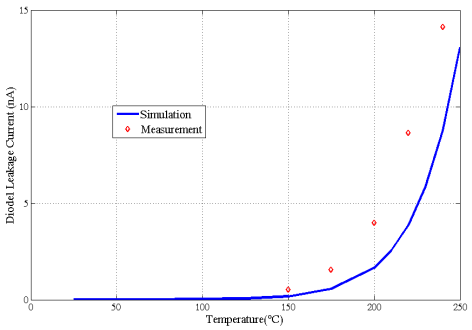

Fig. 8. Diode leakage current vs. temperature.

This temperature variation has been utilized to keep the power consumption of the sensor circuit at a very low level in the desired temperature range (≤200°C) for the high-temperature gate driver circuit.

Fig. 9 shows the schematic of the proposed temperature sensor circuit. The core temperature sensing element of this circuit is the reverse-biased diode, D_{sense}. Several (M number) p-n junction diodes are connected in parallel to increase the total leakage current which depends on the die temperature. Diode leakage current, which is typically in the nA range, is first multiplied by the PMOS current mirror with 1:30 ratio and then converted to a voltage signal by the resistor R_L. The voltage drop across the resistor R_L is applied to the input of a Schmitt trigger which is buffered using a digital inverter circuit to drive the output node. With the increase in die temperature, voltage drop across R_L goes high, and once it exceeds the low-to-high threshold voltage of the Schmitt trigger, V_{out} transitions to a logic high (V_{DD}) indicating a fault condition. This feedback signal is sent to the input stage of the gate driver circuit. The high-to-low threshold voltage of the Schmitt trigger is set at a lower value corresponding to a 15°C reduction in die temperature. This hysteresis will prevent the circuit from being inappropriately triggered by a temporary recovery of the fault condition.

VII. Simulation and Test Results

This proposed high-temperature gate driver circuit has been designed and implemented in a 0.8-µm bipolar-CMOS-DMOS (BCD) on SOI process. The gate driver circuit, including on-chip temperature sensor occupies an approximate area of 10 mm^2 (4,050 µm × 2,600 µm) including the bonding pads and the ESD protection circuits. Fig. 10 shows the layout of the core gate driver circuit and the on-chip temperature sensor. This is a part of a larger die which also includes several voltage regulators, UVLO, and short circuit protection unit.

Schematic level simulations of the proposed

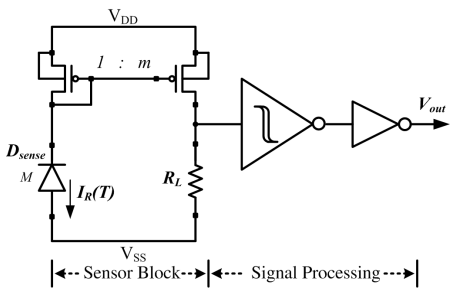

Fig. 9. Schematic of the proposed low-power on-chip temperature sensor circuit.

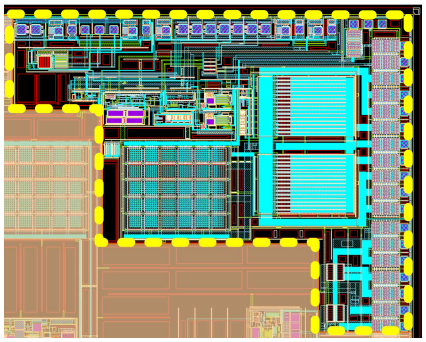

Fig. 10. Layout of the proposed gate driver and temperature sensor circuit.

gate driver circuit were performed over a wide temperature range (−60°C to 250°C). A capacitive load of 10 nF in series with 2-Ω resistor is used in the simulations to mimic the gate of a SiC power switch. Fig. 11 shows the gate drive voltage (V_{op}) generated by this circuit along with the current carried by the M_H and M_L transistors. Low-to-high transition of V_{op} indicates the turning ON operation of the power switches. During this transition, sinking current through M_L is zero and the large drive current is sourced by the M_H transistor. During the high-to-low transition of V_{OP}, which indicates turning OFF operation of the power switch, a large sinking current passes through the M_L transistor and the current through M_H remains zero. Repeating these simulations at different temperatures (−60°C, 95°C, and 250°C) confirms the complementary switching of the M_H and M_L transistors. This reduces the power dissipation through these devices and helps to keep the junction temperature closer to the ambient.

Earlier prototypes of this gate driver circuit were successfully tested without any heat sink and cooling mechanism up to 200°C temperature while driving prototype SiC MOSFETs or JFETs [6]. Extensive characterization of this improved gate driver circuit will also be carried out with SiC power switches at and above 200°C.

Fig. 12 shows the sensor output signal, V_{out} with the increase in die temperature for two different settings of the number of reverse-biased diodes ($M=20$ and $M=5$) used as sensing elements. Twenty diodes in parallel set the fault triggering temperature to 230°C, whereas five diodes set the fault triggering temperature to 263°C. Fig. 12 also shows the logic high-to-low transition for V_{out} when the die temperature decreases. By proper design of the Schmitt trigger, 15°C hysteresis was provided in the sensor circuit. Power consumption of this sensor circuit is only 0.6 µW at 150°C, which goes to just under 10 µW at 200°C.

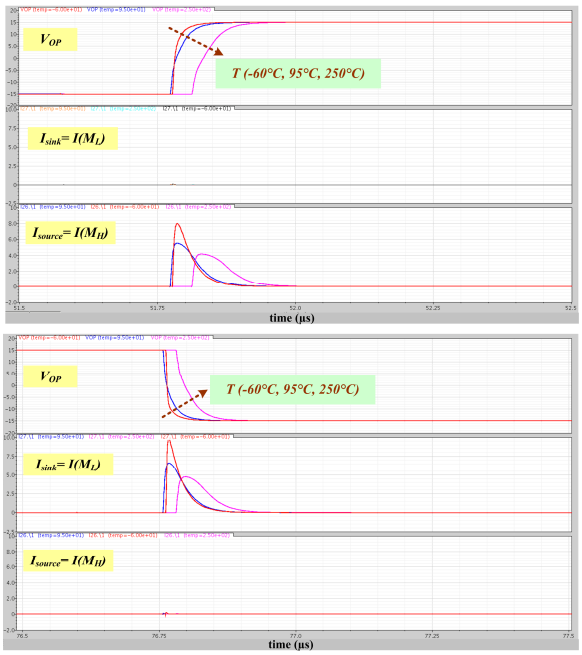

Fig. 11. Simulation results of the proposed high-temperature gate diver circuit at different temperatures (*Red: −60°C, Blue: 95°C, and Pink: 250°C*).

VIII. Conclusions and Future Work

The proposed SOI gate driver circuit has the current drive strength of 6 A at −50°C and 4 A at 200°C. Large current drive is necessary to drive power switches with large current ratings. Often several power switches are connected in parallel to boost the current handling capability of the system, which also requires large drive current from the gate driver circuit. Simulation results indicate that the proposed driver circuit can drive a 10 nF capacitive load in less than 50 ns and 70 ns at −50°C and 200°C respectively. The switching frequency of the driver can reach 500 kHz which will help to reduce the required size of the power converter modules by reducing the size of the filtering elements.

Monte Carlo simulation across the wide temperature range (−50°C to 250°C) shows very little variation in the gate driver circuit performance. The on-chip low-power temperature sensor circuit incorporated in the chip to safeguard the gate driver consumes very little power up to 200°C temperature.

For efficient and effective integration of wide bandgap power devices into power electronic modules, SOI-based integrated circuits capable of working above 200°C ambient temperature are needed to interface them with control circuitry. The improved high-temperature and high-voltage gate-driver circuit presented in this paper is part of an on-

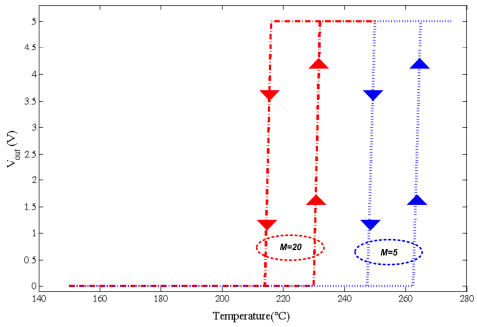

Fig. 12. Temperature sensor circuit's output with the increase and decrease of die temperature.

going research effort to design a heat-sink-less, air cooled DC-DC converter and three phase inverter that can be placed under the hood of hybrid or plug-in hybrid electric vehicles. Although this gate driver circuit has primarily been designed for automotive applications, this could be easily incorporated into any power electronic module developed for harsh environment applications where conventional bulk silicon-based circuits cannot deliver efficient, reliable solutions.

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References

[1] M. Ehsani, Yimin Gao, and J. M. Miller, "Hybrid electric vehicles: architecture and motor drives", *Proceedings of the IEEE*, 2007. Vol. 95, No. 4, pp. 719-728, 2007.

[2] M. Marchesoni and C. Vacca, "New DC-DC converter for energy storage system interfacing in fuel cell hybrid electric vehicles", *IEEE Tran. on Power Electronics*, Vol. 22, No. 1, pp. 301-308, 2007.

[3] F. H. Khan and L. M. Tolbert, "A multilevel modular capacitor-clamped DC-DC converter", *IEEE Tran. on Industry Applications*, Vol. 43, No. 6, pp. 1628-1638, 2007.

[4] R. W. Johnson, J. L. Evans, P. Jacobsen, and R. Thompson, "High-temperature automotive electronics", *Proceedings of International Conference on Advanced Packaging and Systems*. Reno, NV, March 10-13, pp. 77-87, 2002.

[5] R. Sharp, "The current status of high temperature electronics for automotive use", *Automotive Electronic Standareds; Are They? (Ref. No. 1999/206), IEE Seminar on*, pp. 6/1-6/5, 30 Nov. 1999.

[6] M. A. Huque, L. M. Tolbert, B. Blalock, and S. K. Islam, "SOI-based high-voltage, high-temperature integrated circuit gate driver for SiC-based power FETs", *IET Proceedings on Power Electronics*, vol. 3, 2010, (accepted – in press).

[7] M. A Huque, B. J. Blalock, C. Su, R. Vijayaraghavan, S. K. Islam, and L. M. Tolbert, "SOI based integrated circuits for high-temperature applications", *Proceedings of International Conference and Exhibition on High Temperature Electronics (HiTEC 2008)*, Albuquerque, New Mexico, May 13 - 15, 2008.

[8] A. Elasser, and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems", *Proceedings of the IEEE*, Vol. 90, No. 6, pp. 969-986, 2002.

[9] M. N. Yoder, "Wide bandgap semiconductor materials and devices", *Electron Devices, IEEE Transactions on*, Vol. 43, No. 10, pp. 1633-1636, 1996.

[10] B. Ozpineci, L. M. Tolbert, S. K. Islam, and M. Hasanuzzaman, "System impact of SiC power devices", *Frontiers in Electronics*, pp. 233-242, 2002.

[11] R. W. Johnson, J. L. Evans, P. Jacobsen, J. R. Thompson, and M. Christopher, "The changing automotive environment: high-temperature electronics", *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 27, No. 3, pp. 164-176, 2004.

[12] P. G. Neudeck, R. S. Okojie, and L.Chen, "High-temperature electronics - a role for wide bandgap semiconductors?", *Proceedings of the IEEE*, Vol. 90, No. 6, pp. 1065-1076, 2002.

[13] B. Gentinne, J. P. Eggermont, D. Flandre, and J. P. Colinge, "Fully depleted SOI-CMOS technology for high temperature IC applications", *Materials Science and Engineering B*, Vol. 46, No. 1-3, pp. 1-7, 1997.

[14] J. P. Colinge, "SOI for hostile environment applications", *Proceedings of 2004 IEEE International SOI Conference*, pp. 1-4, 2004

[15] http://www.cissoid.com

[16] F. S. Shoucair, "Analytical and experimental methods for zero-temperature-coefficient biasing of MOS transistors", *Electronics Letters*, Vol. 25, No. 17, pp. 1196-1198, 1989.

[17] V. Szekely, C. Marta, Z. Kohari, and M. Rencz, "CMOS sensors for on-line thermal monitoring of VLSI circuits", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 5, No. 3, pp. 270-276, 1997.

[18] M. A. P. Pertijs, G. C. M. Meijer, and J. H. Huijsing, "Precision temperature measurement using CMOS substrate PNP transistors", *IEEE Sensors Journal*, Vol. 4, No. 3, pp. 294-300, 2004.

[19] M. A. P. Pertijs, A. Niederkorn, M. Xu, B. McKillop, A. Bakker, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ±0.5°C from -50°C to 120°C", *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 2, pp. 454-461, 2005.

[20] M. Tuthill, "A switched-current, switched-capacitor temperature sensor in 0.6µm CMOS", *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 7, pp. 1117-1122, 1998.