High Temperature Packaging of 50 kW Three-Phase SiC Power Module

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Abstract **-- Research on silicon carbide (SiC) power electronics has shown their advantages in high temperature and high efficiency applications. This paper presents a SiC JFET based, 200 °C, 50 kW three-phase inverter module and evaluates its electrical performance. With 1200 V, 100 A rating of the module, each switching element is composed of four paralleled SiC JFETs (1200 V/25 A each) and two anti-parallel SiC Shottky Barrier Diodes (SBDs). The substrate layout inside the module is designed to reduce package parasitics. Then, experimental static characteristics of the module are obtained over a wide range of temperature, and low on-state resistance is shown up to 200 °C. A gate driver, with different turn-on, turn-off gate resistances and RCD network, is designed to optimize the switching performances. The module is verified to have low power loss, fast switching characteristics at 650 V dc bus voltage, 60 A drain current, in both simulation and experiments. Finally, switching time and losses, obtained from simulation and experiment, are compared.**

Index Terms **— High Power, High Temperature, Packaging, SiC JFET Power Module.**

I. INTRODUCTION

With the increasing demand for high frequency, high power and high temperature applications, Si power devices are now facing material limits. SiC is the most promising alternative to Si due to its attractive properties. It can withstand much higher voltage stress with much lower on-state resistance, and the large band gap energy of it results in a much higher temperature capability. Meanwhile, SiC has a higher thermal conductivity, which leads to important benefits for power dissipation and higher power handling capability. Research on SiC power devices has revealed their better efficiency compared to Si power devices due to the reduction in both conduction and switching losses [1-3]. Furthermore, with high temperature packaging, the high temperature capability of SiC power devices can be utilized [4].

Unipolar devices like SiC MOSFET and SiC JFET have been improved through the years and have been commercialized [5]. Research on the application of SiC MOSFETs and SiC MOSFET based power module has been done [6-11]. However, MOSFET has the inherent oxide interface issues at high temperatures that need to be solved if it is to be applied in extreme temperature applications [12]. The JFET does not have any interface issues.

The structure of the SiC JFET was discussed in detail in [13-15]. The modeling characterization of SiC JFET, and its system applications have been reported in several papers [15-21]. Several SiC JFET and SiC diode based power modules have been presented [22-24].

In high power applications, power devices are often used in parallel in order to achieve a higher current rating. The performance of the individual SiC JFET during parallel operation in the module has been studied in [5]. A SiC JFET and SiC Schottky diode based phase-leg power module has been developed at 200 °C and used in three-phase inverter system in [24]. The power of this three-phase inverter system was 18 kW.

This paper presents a SiC JFET and Schottky Barrier Diode (SBD) based, 200°C, 50 kW multi-chip three-phase inverter power module, which is designed for use in switching applications such as AC motor control, motion/servo control, uninterruptible power supplies, and photovoltaic systems. The electrical characterizations of this module is presented, and the module is verified to have low on-state resistance and low power losses as well as fast switching characteristics at 650 V, 60 A, and 200 °C in simulation and 150 °C in experiments.

This paper starts with the description of the high power, high temperature, SiC JFET and SiC SBD based power module in Section II. The static characteristics of it are presented in Section III. The switching characteristics of this module, including the gate drive design for it, are provided in Section IV. The final conclusions are discussed in the last section.

II. SIC JFET MODULE OVERVIEW

In order to meet high power, high temperature and high efficiency application needs, the authors have developed a 200 °C, 50 kW three-phase inverter module with 1200 V, 100 A power rating. Each switching element consists of four 4.17 mm x 4.17 mm normally-on SiC JFETs with two 2.7 mm x 2.7 mm anti-parallel SiC SBDs. All devices are from SiCED [25]. The JFETs have a nominal pinch-off voltage of -17 V and breakdown voltage of -26 V. The maximum junction temperature is designed to be 200 °C. Fig. 1 and Fig. 2 show the circuit and layout of a single phase-leg. Devices in the same natural current commutation path are put close in order to reduce the package parasitics.

Three substrates are prepared for the module, and each substrate forms a single phase, as shown in Fig. 3. Ceramic gate substrates with thin film metal are soldered on the direct bond copper (DBC) on Si_3N_4 substrate. SiC dies are soldered to the substrate. Two copper pins for control contacts are used to reduce package parasitics. SiC dies and busbars are wire bonded using 5 mil and 8 mil aluminum wires, respectively. Fig. 4 shows a picture of the module with the double pulse test board.

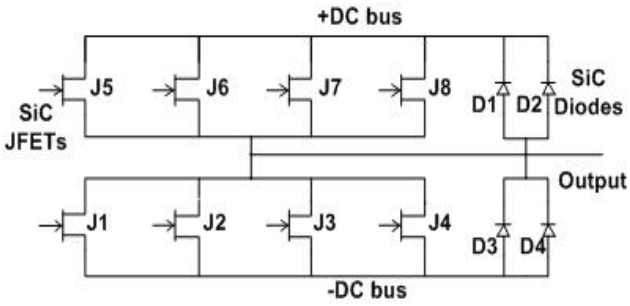

Fig.1. Single phase-leg circuit.

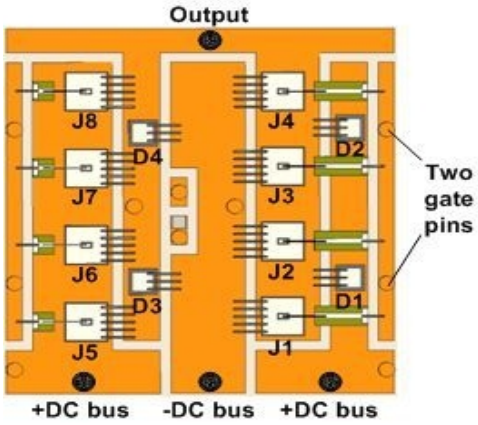

Fig. 2. Substrate layout of single phase-leg.

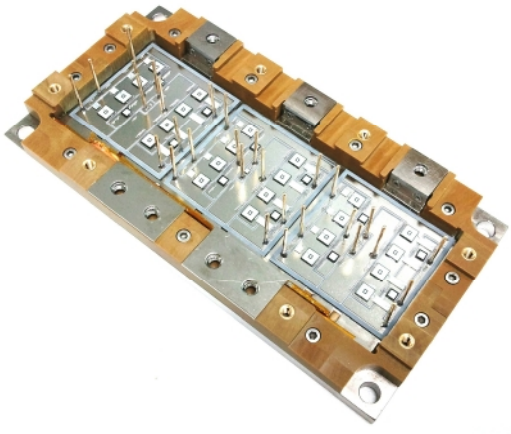

Fig. 3. Module inside structure.

III. Static Characteristics

The forward characteristics of the four paralleled SiC JFETs in a phase-leg are obtained at different temperatures from 25 °C to 200 °C, as shown in Fig. 5. The forward characteristics are obtained at the gate-source voltage of 0 V since they are normally-on devices. Fig. 6 shows the on-state resistance changes over a temperature range from 25 °C to 200 °C. From Fig. 6, the on-state resistance of the four paralleled SiC JFETs in the module increases with higher temperature, from 25 mΩ at 25 °C to 55 mΩ at 200 °C. Fig. 7 to Fig. 9 show the SiC JFET phase-leg forward characteristics at different gate-source voltages at 25 °C, 125 °C, and 200 °C, respectively.

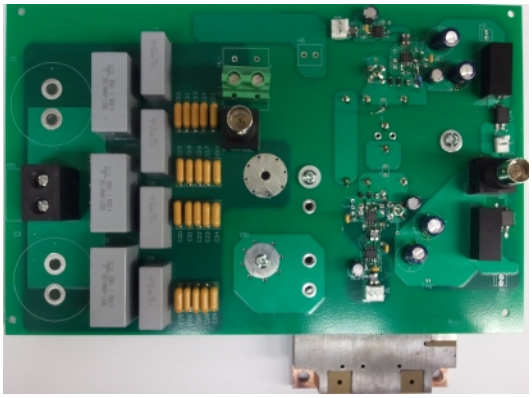

Fig. 4. SiC JFET-based power module with the double pulse test board.

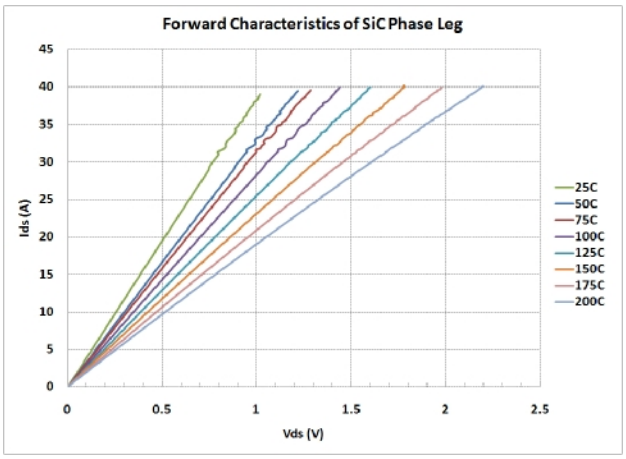

Fig .5. Forward characteristics of four paralleled SiC JFETs in the module.

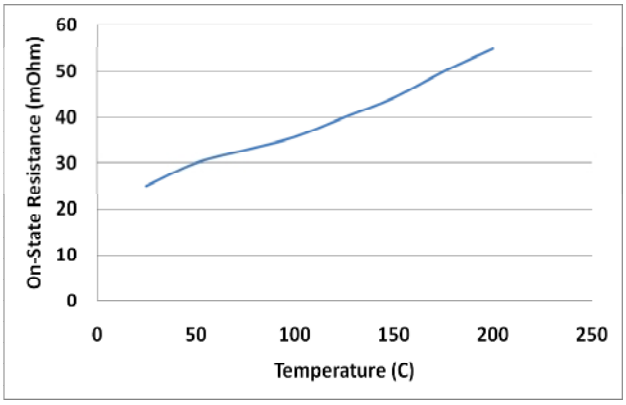

Fig. 6. On-state resistance of four paralleled SiC JFETs in the module.

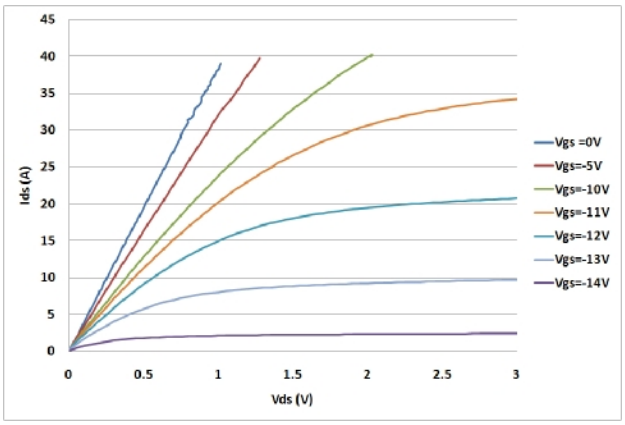

Fig.7. Module's four paralleled SiC JFETs forward characteristics with different gate-source voltage at 25 °C.

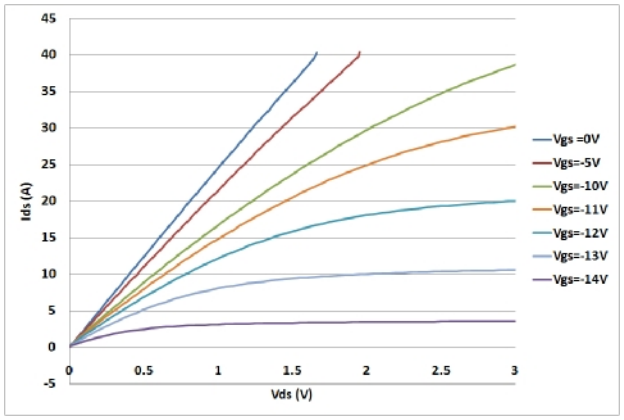

Fig.8. Module's four paralleled SiC JFETs forward characteristics with different gate-source voltage at 125 °C.

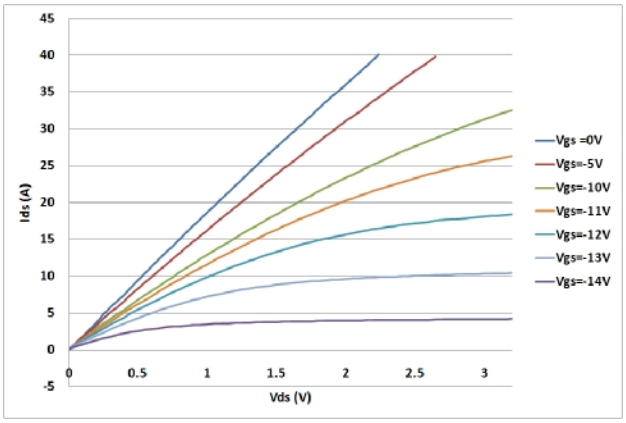

Fig.9. Module's four paralleled SiC JFETs forward characteristics with different gate-source voltage at 200 °C.

Fig. 10 shows the forward characteristics of the two paralleled SiC SBDs. From Fig. 10, SiC SBDs conduction resistance R_D also increases with increasing temperature. However, the threshold voltage of the SBDs decreases when the temperature increases.

Fig. 11 shows the transfer characteristics of the four paralleled SiC JFETs at different temperatures. Since the SiC JFET is normally-on, the pinch-off voltage is negative. From Fig. 11, the pinch-off voltage decreases with increasing temperature.

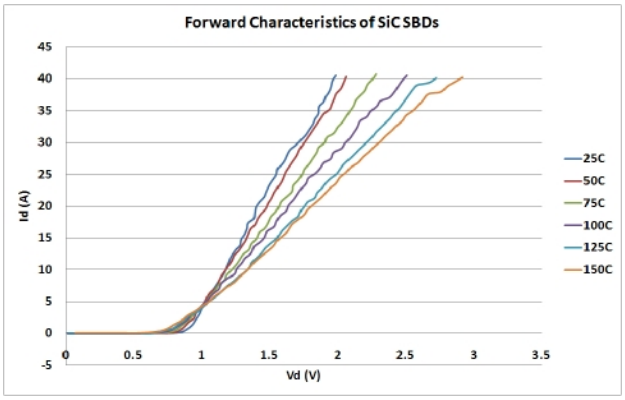

Fig. 10. Forward characteristics of two paralleled SiC SBDs in the module.

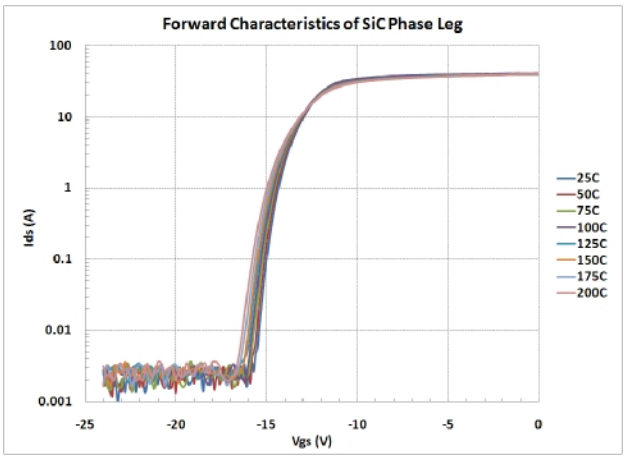

Fig. 11. Transfer characteristics of four paralleled SiC JFETs in the module.

IV. Switching Characteristics

A. *Gate Drive Design*

Switching characteristics of the power module are evaluated by double pulse test. Fig. 12 shows the gate drive circuit used for the module switching test. Considering JFET pinch-off and breakdown voltage values, and their variation in four paralleled JFETs, 0 V is chosen for turn-on and -24 V is used for turn-off. A 10 kΩ resistor and a 10 nF capacitor are used in RCD network, which will limit avalanche current and supply high gate current peaks [15]. Gate resistances are chosen differently for turn-on and turn-off transients. In the test, for four paralleled JFETs, turn-on resistance is 4 Ω and turn-off resistance is 10 Ω, which can aid fast switching while avoiding shoot-through caused by high dv/dt. Also, a common mode (CM) choke is used to reduce the CM current induced by fast switching which will impair the switching waveform measurement, and the two isolated gate signals are sent to the input side of the CM choke. The driver IC is IXDD414, which is based on PMOS-NMOS totem-pole structure.

A 0.1 Ω shunt resistor is used to measure the switching current Ids with little parasitic inductance's influence. Probe Tip Adapter (PTA) is used to measure the gate-source voltage Vgs. BNC is used to measure drain-source voltage Vds. The shunt, PTA, and BNC share the same ground; a non-differential probe is used for all the three measurements in the switching period with minimum distortion from the real curves.

For phase-leg test, shoot-through protection is needed, especially for the phase-leg with normally-on JFETs. In the test, the shoot-through protection of phase-leg is realized by an IGBT which is series connected in +DC bus. It is driven by a current-sensing single-channel drive (IR2127). Once shoot-through happens, the IGBT is turned off to separate the phase-leg from DC power supply.

In the double pulse test, the four high side JFETs are off, and the double pulse signal is applied to the gates of the four low side JFETs. The load in the test is a 1 mH inductor.

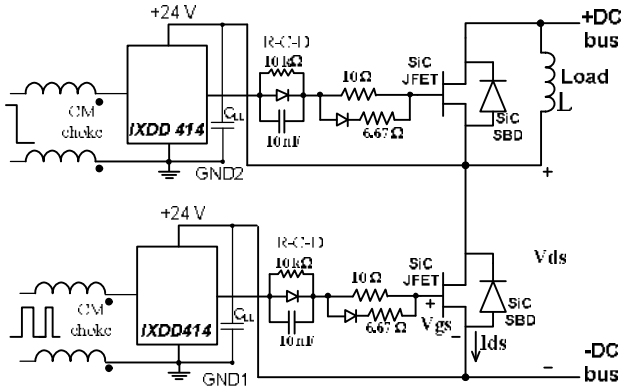

Fig. 12. Gate drive circuit for SiC JFET based module.

B. Simulation Results

The double pulse test simulation for a single phase leg is done in Saber, under 650 V dc bus voltage, 60 A load current and 200 °C junction temperature.

Fig. 13 and Fig. 14 respectively show the simulation waveforms of turn-on and turn-off transient. Ids is the total drain current of the four low side paralleled JFETs; Vgs and Vds are gate voltage and drain to source voltage of low side JFETs. Table I shows the turn-on, turn-off time and power loss of each paralleled JFET. Here, the turn-on time is defined as the time from the current rising to 10% of its peak value until the voltage falls to 10% of the dc voltage value. Similarly, turn-off time is defined from the time the current falls to 90% until the voltage rises to 90% of its dc value. The power loss differences of each JFET come from the unbalanced current, which is caused by parameter variation of each JFET and different package parasitics in each JFET loop. Fig. 15 shows the unbalanced current of the four paralleled JFETs during turn-on transient.

During low side JFETs turning on, the Miller capacitances of high side JFETs oscillate Vgs by their charging and discharging currents and then shoot-through happens. Large gate loop parasitic inductance makes shoot-through happen easily since the voltage across it causes Vgs to exceed the pinch-off voltage. To avoid shoot-through, turn-on transient has to be slowed down, which will lead to high turn-on loss. For four paralleled JFETs in the module, the gate loop inductances are 36, 27, 27, 36 nH respectively if only one gate pin is put in the middle of four JFETs, as shown in Fig. 16. However, if two gate pins are put in between two closer JFETs to make the distance evenly distributed among four JFETs, their gate loop inductances will all be balanced to be 27 nH, as shown in Fig. 17. The gate loop parasitic inductances of the 1st and 4th JFETs are reduced and current unbalance is improved too.

TABLE I
SWITCHING TIME AND LOSS OF EACH PARALLELED JFET IN THE MODULE (SIMULATION RESULTS)

	J1	J2	J3	J4
Turn-on time (ns)	130			
Turn-on loss (uJ)	787.1	677.6	666.8	608.8
Turn-off time (ns)	140			
Turn-off loss (uJ)	602.5	626.4	628.3	647.9

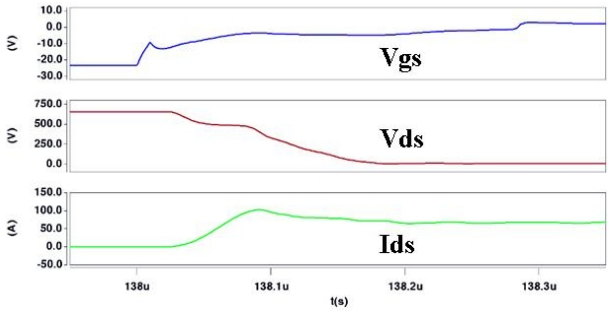

Fig. 13. Simulation turn-on waveforms at 200 °C.

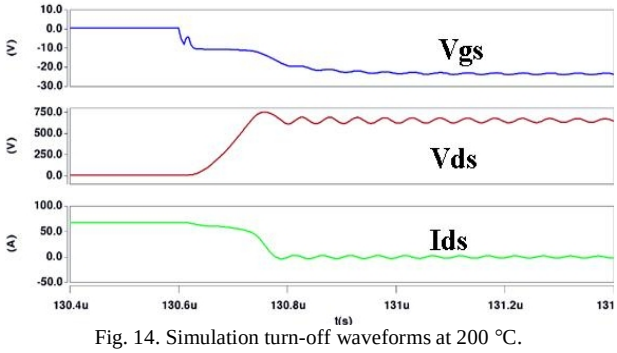

Fig. 14. Simulation turn-off waveforms at 200 °C.

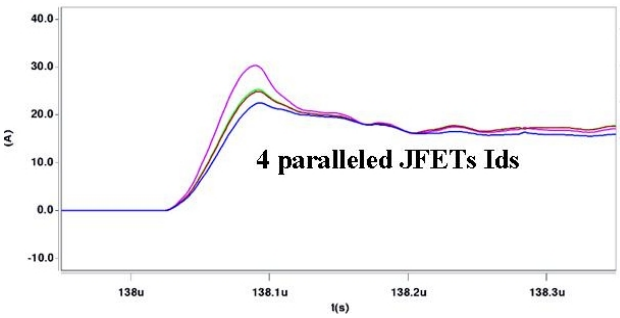

Fig. 15. Unbalanced current during turn-on.

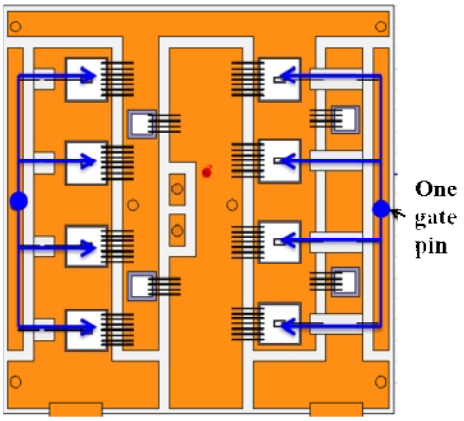

Fig. 16. One gate pin layout.

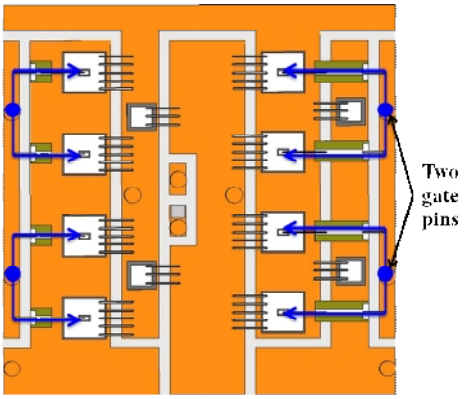

Fig. 17. Two gate pins layout.

C. Experimental Results

The double pulse test is done under 650 V dc bus voltage, 60 A load current and 150 °C junction temperature. Fig. 18 shows the high temperature test setup which is used to test the switching performances of the power module at high temperature. The module is heated by connecting to hot plate on the bottom side of the test board. A fan is used cool the gate driver and shunt to make sure they will not be heated to high temperature. The temperature is monitored by thermocouples. Fig. 19 shows the photo of the high temperature testing setup.

Fig. 20 and Fig. 21 are experimental waveforms of turn-on and turn-off, respectively. The turn-on overshoot current is not very high even at high temperature (18 A) due to the freewheeling SiC SBDs, which has no reverse recovery. So the switching power losses will be reduced. Fig. 22 shows the switching power losses as a function of load current at 150 °C, both under 325 V DC bus voltage and 650 V DC bus voltage.

Table II lists switching time and loss obtained from simulation and experiments. From the results, it is obvious that this SiC JFETs and SiC SBDs based, high power, multi-chip, three-phase inverter module can be operated at fast switching and low switching losses at high temperature.

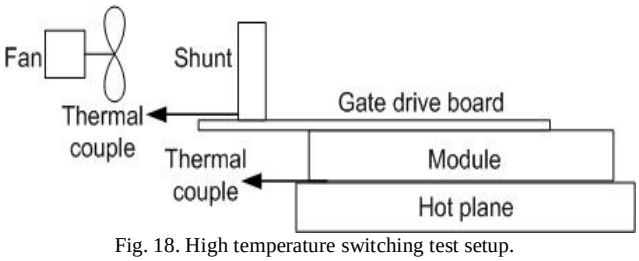

Fig. 18. High temperature switching test setup.

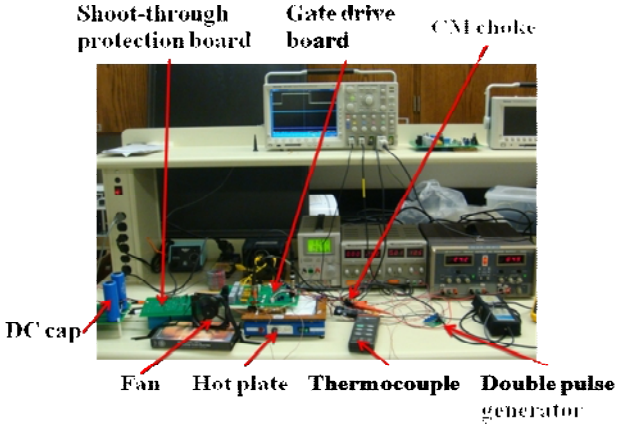

Fig. 19. Testbed for high temperature switching test.

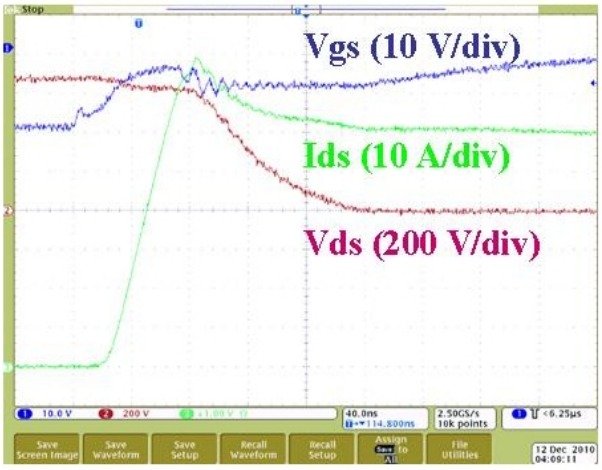

Fig. 20. Experimental turn-on waveforms at 150 °C.

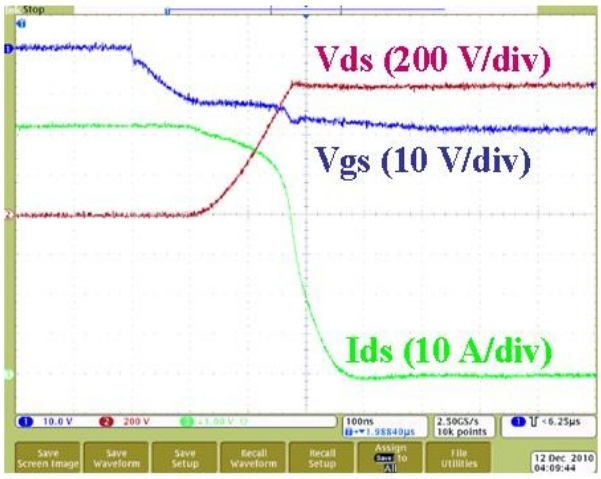

Fig. 21. Experimental turn-off waveform at 150 °C.

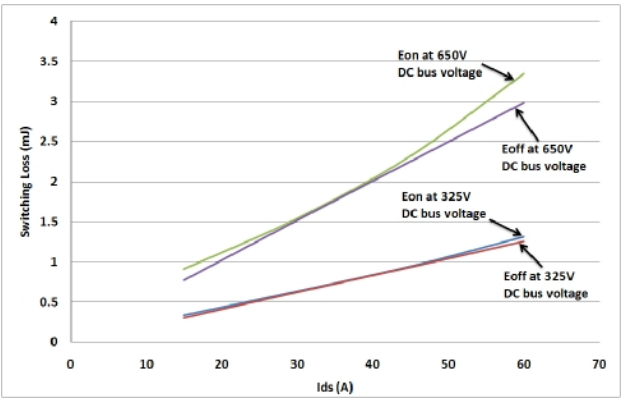

Fig. 22. Switching losses plotted as a function of load current for various DC bus voltage at 150 °C.

TABLE II
SWITCHING TIME AND LOSSES OF FOUR PARALLELED JFETS IN THE MODULE
(SIMULATION AND EXPERIMENTAL RESULTS)

	Simulation results	Experimental results
Turn-on time (ns)	130	140
Turn-on loss (mJ)	2.85	3.34
Turn-off time (ns)	140	170
Turn-off loss (mJ)	2.53	2.89

V. CONCLUSIONS

A SiC JFET and SiC SBDs based, 50 kW, multi-chip, three-phase inverter power module with high temperature packaging (200 °C) is designed and demonstrated. Each switching element consists of four paralleled normally-on SiC JFETs with two anti-parallel SiC SBDs. Short natural current commutation path and two gate control pins are designed to reduce package parasitics. The static test results exhibit the on-state resistance of the phase-leg is 55 mΩ at 200 ºC. Different turn-on and turn-off resistances are used to improve its switching characteristics at high temperature. Double pulse test simulation at 200 °C junction temperature and experimental results of double pulse test, under 650 V dc bus voltage, 60 A load current and 150 °C junction temperature, show its fast switching and low switching power losses, which is 3.34 mJ for turn-on and 2.89 mJ for turn-off.

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