Capacitor Voltage Control in a Cascaded Multilevel Inverter as a Static Var Generator

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***Abstract*— The widespread use of non-linear loads and power electronics converters has increased the generation of non-sinusoidal and non-periodic currents and voltages in power systems. Reactive power compensation or control is an important part of a power system to minimize power transmission losses. Given a modulation index, the switch times can be chosen to achieve the fundamental while eliminating specific harmonics. However, the resulting total harmonic distortion (THD) depends on the modulation index (see [1][2]). This work considers the control of the DC capacitor voltage in such a way that one can operate at the modulation index which results in the minimum THD. This paper presents the development of specific control algorithms for a cascaded multilevel inverter to be used for static var compensation.**

***Index Terms*— Multilevel Inverter, Static Var Generator (SVG), Cascade inverter.**

I. Introduction

Multilevel inverters have gained much attention in recent years as an effective solution for various high power and high voltage applications. A multilevel inverter is a power electronic device built to produce ac waveforms from small voltage steps by utilizing isolated dc sources or a bank of series capacitors. The multilevel inverter is ideal for connecting distributed dc energy sources (solar cells, fuel cells, the rectified output of wind turbines) to an existing three phase power grid [3].

Multilevel inverter structures have been developed to overcome shortcomings in solid-state device ratings so that they can be applied to high-voltage, high power electrical systems. As pointed out in [3][4][5], the advantage of the cascaded multilevel inverter includes: (1) its active devices switch at (or nearly) the fundamental frequency drastically reducing the switching losses, (2) it eliminates the need for a transformer to provide the requisite voltage levels, (3) packaging is much easier because of the simplicity of structure and lower component count, and (4) as there are no transformers, it can respond much faster.

It is widely acknowledged that a major concern in any power system is power quality, and especially to have low harmonic content. This is because of the effects harmonics have on the energy efficiency of the power system as well as the detrimental effect they have on the reliability of the equipment connected to it. Because the multilevel inverter is switching at the fundamental frequency, its generated harmonics are much lower in frequency than high-carrier frequency based PWM systems. As a result, a major concern in designing a static var compensator based on the multilevel inverter is to ensure that its total harmonic distortion is within allowable standards.

Previous work in [1][2] has shown the switching angles in the multilevel inverter are found so as to produce the required fundamental voltage while at the same time not generate higher order harmonics. However, for 3-level multilevel inverter, if modulation index is out of the range 1.18 through 2.5, there exists no set of switching angles such that the fundamental can be controlled while at the same time completely eliminating the 5th and 7th order harmonics. In this work, a control strategy is presented to vary the level of the DC capacitor voltage so that use of the staircase switching scheme (with its inherent low switching losses).

II. Cascaded H-bridges

A cascaded multilevel inverter is made up from a series of H-bridge (single-phase full bridge) inverters, each with their own isolated dc bus. This multilevel inverter can generate almost sinusoidal waveform voltage from several separate dc sources (SDCSs), which may be obtained from solar cells, fuel cells, batteries, ultracapacitors, etc. Figure 1 shows a single-phase structure of an M-level H-bridges multilevel cascaded inverter. Each level can generate three different voltage outputs $+V_{dc}, 0$ and $-V_{dc}$ by connecting the dc sources to the ac output side by different combinations of the four switches.

The output voltage of an M-level inverter is the sum of all of the individual inverter outputs. It is clear from Figure 1 that to have an M-level cascaded multilevel inverter we need $\left(\frac{M-1}{2}\right)$ H-bridge units in each phase. An example phase voltage waveform for a 7-level cascaded multilevel inverter with three dc sources and three full bridges is shown in Figure 2. The output phase voltage is given by $v_{an} = v_{a1} + v_{a2} + v_{a3}$.

As Figure 2 illustrates, each of the H-bridge's active devices switches only at the fundamental frequency, and each H-bridge unit generates a quasi-square waveform by phase-shifting its positive and negative phase legs' switching timings. Further, each switching device always conducts for 180^o (or 1/2 cycle) regardless of the pulse width of the quasi-square wave so that this switching method results in equalizing the current stress in each active device.

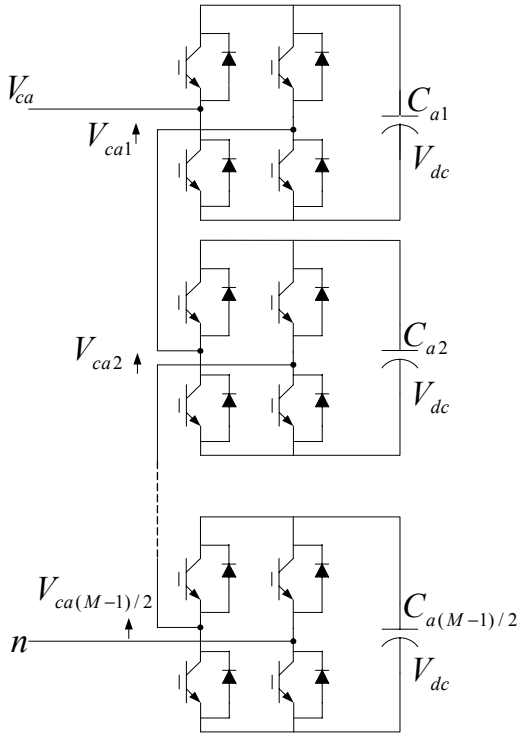

Fig. 1. Single-phase structure of a m-level H-bridges multilevel cascaded inverter.

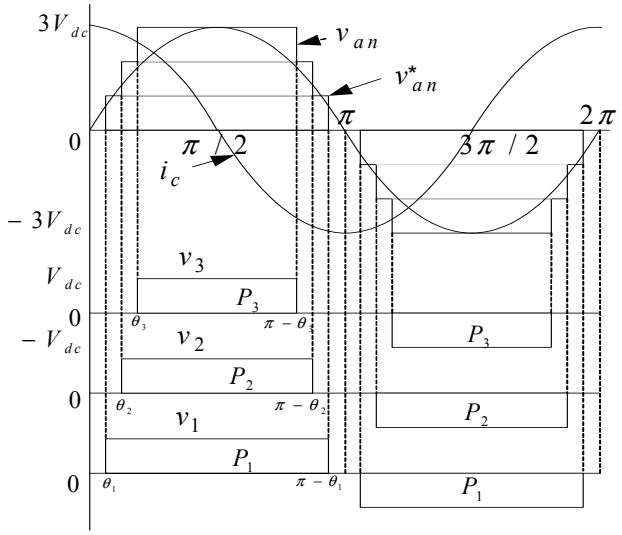

Fig. 2. Output waveform of a 7-level cascade multilevel inverter.

III. SVG SYSTEM CONFIGURATION AND OPERATION

Figure 3 shows the system configuration and control block diagram of a Static Var Generator (SVG) using a cascaded multilevel inverter, where L_c is the inverter interface inductance, v_s represents the source voltage, I_c^* (or q_c^*) is the reactive current (or reactive power) reference, and V_{dc}^* is the dc link voltage reference (see [6]). The switching pattern table shown in Figure 3 generates the switching gate signals by given modulation index and phase angles through a look-up table. The look-up table is made from the switching angles which are computed off-line to minimize harmonics for each modulation index m. θ is the phase angle of the source voltage. α_c is phase-shift angle of the output voltage.

Here the modulation index m is defined by

$$m = s\frac{V_c^*}{V_{c\max}}, \tag{1}$$

where V_c^* is the magnitude reference of the inverter output voltage. Using the techniques in [3][6],

$$V_c^* = \sqrt{v_{ca}^{*2} + v_{cb}^{*2} + v_{cc}^{*2}}. \tag{2}$$

$V_{c\max}$ is the maximum obtainable magnitude of voltage when all the switching phase angles are zero:

$$V_{c\max} = \sqrt{\frac{3}{2}}\frac{4}{\pi}sV_{dc}, \tag{3}$$

where s is the number of sources.

Figure 4 shows the equivalent circuit of the SVG system (see [6]). A leading reactive current (capacitive current) is drawn from the line when the amplitude of the output voltage V_C is larger than the source voltage's amplitude which means vars are generated. A lagging reactive current (inductive current) is drawn from the line when the amplitude of the output voltage V_C is smaller than the source voltage's amplitude which means vars are absorbed. Since phase current i_{ca} is leading or lagging the phase voltage v_{can} by 90^o as shown in Figure 2, the average charge on each dc capacitor will be zero which means there is no net real power exchange between the multilevel inverter and the utility line. To compensate the switching device loss and capacitor loss, the multilevel inverter should be controlled so that some real power is delivered to the dc capacitor. In principle, each dc capacitor voltage can be controlled to be exactly the dc desired voltage, V_{dc}^*.

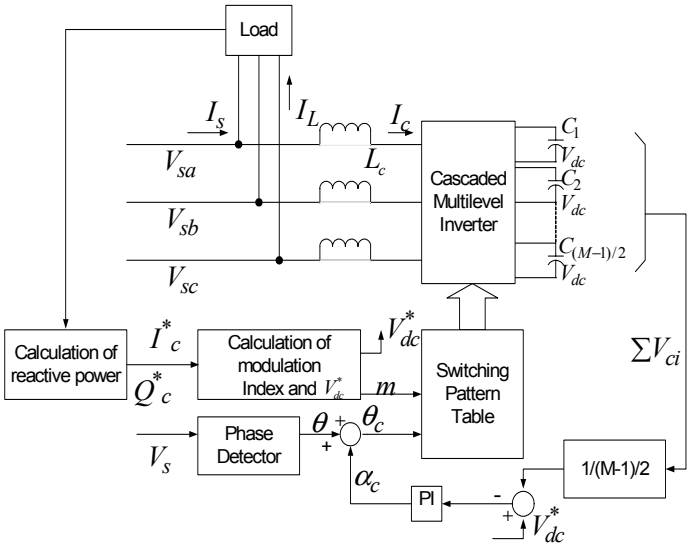

Fig. 3. SVG system configuration using the cascaded multilevel inverter.

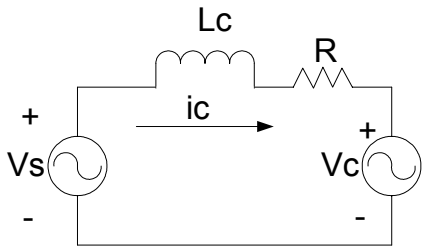

Fig. 4. Equivalent circuit of the SVG system.

IV. DYNAMIC MODELS OF SVG SYSTEM

Following [6] the source voltage v_s, output voltage of the multilevel inverter v_c, and SVG system current i_c can be represented in the $\alpha\beta$-frame using the $abc-\alpha\beta$ transformation

$$C = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \tag{4}$$

matrix, then by using the synchronous reference frame transformation

$$T = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \tag{5}$$

v_s can be represented by dq-coordinate expressions. Thus the equivalent circuit of the SVG system can be represented by

$$L_c \frac{d}{dt} \begin{bmatrix} I_{cd} \\ I_{cq} \end{bmatrix} + \omega L_c \begin{bmatrix} -I_{cq} \\ I_{cd} \end{bmatrix} + R \begin{bmatrix} I_{cd} \\ I_{cq} \end{bmatrix} = \begin{bmatrix} V_{sd} - V_{cd} \\ V_{sq} - V_{cq} \end{bmatrix} \tag{6}$$

and

$$v_s = \begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} = \begin{bmatrix} V_s \\ 0 \end{bmatrix}, \tag{7}$$

where V_s is the rms value of the line-to-line voltage, and θ is the phase angle.

The instantaneous active power P_c flowing into the SVG, and instantaneous reactive power Q_c drawn by the SVG can be represented by

$$P_c = V_s I_{cd} \quad \text{and} \quad Q_c = V_s I_{cq}, \tag{8}$$

where I_{cd} and I_{cq} are the active current and reactive current of SVG respectively.

Based on equation (6), in order for the SVG system to generate the desired the active current and reactive current, the modulation index should be given by the following

$$\begin{bmatrix} V^*_{cd} \\ V^*_{cq} \end{bmatrix} = \begin{bmatrix} V_{sd} + \omega L_c I^*_{cq} - \left(L_c \frac{d}{dt} I^*_{cd} + R I^*_{cd}\right) \\ V_{sq} - \omega L_c I^*_{cd} - \left(L_c \frac{d}{dt} I^*_{cq} + R I^*_{cq}\right) \end{bmatrix} \tag{9}$$

$$V^*_c = \sqrt{V^{*2}_{cd} + V^{*2}_{cq}} \quad \text{and} \quad m = \frac{V^*_c}{\sqrt{\frac{3}{2}} \frac{4}{\pi} V_{dc}}. \tag{10}$$

V. CONTROL SCHEME OF SVGS

A cascaded multilevel inverter is used as a static var generator to minimize the non-active power/current, which is shown in Figure 3. In this work, an RL load is used. The desired reactive current to be injected by SVG is obtained by

$$Q^*_c = 3 V_{sph} I_{sph} \left|\sin\left(\theta_V - \theta_I\right)\right| \tag{11}$$

$$I^*_{cd} = 0 \quad \text{and} \quad I^*_{cq} = \frac{Q^*_c}{\sqrt{3} V_{sph}} \tag{12}$$

where V_{sph} and I_{sph} are the rms value of the phase-to-phase voltage and current of voltage source. θ_V and θ_I are the phase angles of V_{sph} and I_{sph} separately.

The modulation index m is obtained by equation (9) and (10). For each m, switching angles are computed off-line to eliminate the 5^{th} and 7^{th} harmonics (see [1][2]) and are plotted in Figure 5. Figure 6 shows the THD out to the 49^{th} harmonic. However, one may note that outside the range $m = 1.18$ through $m = 2.5$ and some intervals between $m = 2.4$ and $m = 2.5$, there exists no set of switching angles such that the fundamental can be controlled while at the same time completely eliminating the 5^{th} and 7^{th} order harmonics. So for modulation indices outside this interval, other switching schemes can be used, however, they will typically result in a larger THD.

A control method is proposed here so that m is operated close to the value that gives the minimum THD. By equation (10), it can be seen that in order to generate the desired output voltage (or desired reactive power) with smallest THD, changing the dc link voltage of each level can also force the modulation index to be in the range 1.18 through 2.4 where a solution exists that eliminates the lower order harmonics. In other words, one would not regulate the capacitor voltage to a constant value, but rather they would be changed according to the steady-state operating conditions.

Given the Q^*_c (or I^*_c), modulation index m is computed by equations (9) and (10). If m is in the range 1.18 through 2.4, then

$$V^*_{dc} = V_{dc}. \tag{13}$$

If m is out of the range $1.18 - 2.4$, fix $m = 2.0$, then

$$V^*_{dc} = \frac{V^*_c}{\sqrt{\frac{3}{2}} \frac{4}{\pi} m} = \frac{V^*_c}{\sqrt{\frac{3}{2}} \frac{4}{\pi} 2.0}. \tag{14}$$

A PI controller is used to control each capacitor voltage equal to V^*_{dc}. The control principle can be explained with the aid of Figure 7. In Figure 7, v_s is the source voltage, i_c is the current flowing into the inverter, and v_c is the multilevel inverter output voltage. v_c is controlled so that it lags or leads v_s by α_c, then the total real power P_i flowing between the multilevel inverter and the utility line is

$$P_i = \frac{V_s V_c \sin\alpha_c}{X_{Lc}} \tag{15}$$

where X_{Lc} is the impedance of interface inductor. If v_c lags v_s by α_c, and P_i flows into the multilevel inverter, and the capacitor is charged. If v_c lags v_s by α_c, and P_i flows from the multilevel inverter to the utility line, the capacitor is

discharged. By controlling the charging and discharging of the capacitor voltage, and the capacitor voltage is kept equal to v_{dc}^*.

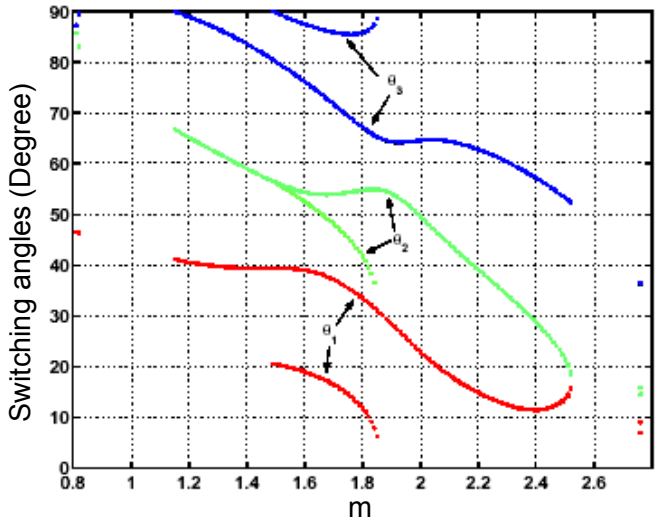

Fig. 5. Switching angles vs modulation index m for 3 dc sources multilevel inverter.

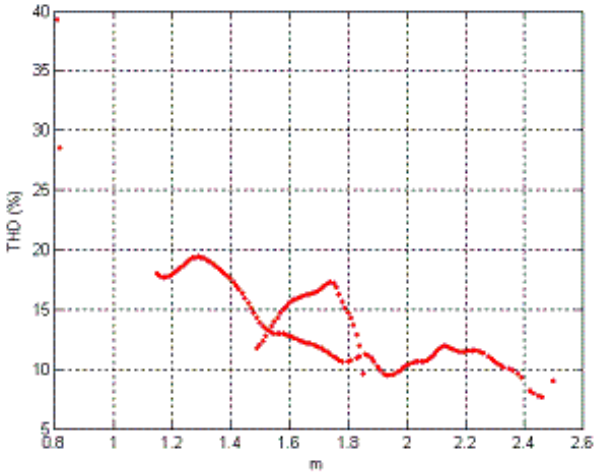

Fig. 6. THD vs modulation index m for 3 dc sources multilevel inverter.

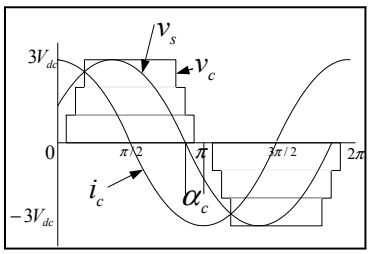

Fig. 7. Control principle for the capacitor voltage of multilevel inverter.

The switching angles are computed in the work [1][2] assuming the dc capacitor voltage of each source of multilevel inverter is the same. To keep the dc voltage balanced between the capacitors of each inverter, the rotated switching scheme using fundamental frequency switching is used, where the switching patterns are rotated every cycle. Figure 8 shows the control logic scheme of rotating the switching patterns (see [7]). By rotation of the switching patterns, all dc capacitors are equally charged and discharged, as well as each of the switching devices having the same switching and current stresses.

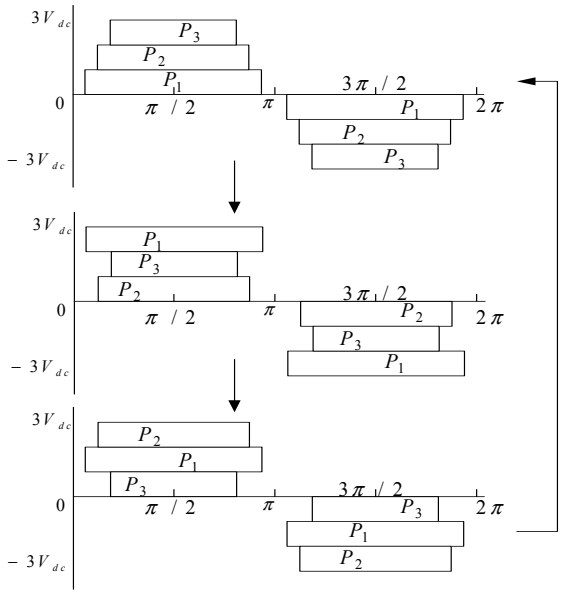

Fig. 8. Rotated switching pattern.

VI. SIMULATION RESULTS

A mathematical model of a 7-level cascaded multilevel inverter is built using Matlab/Simulink. A SVG system and the control system is modeled. In this work an RL load is used, source voltage (rms value of the line-to-line voltage) $V_s = 240$ V, DC link voltage (initial capacitor voltage) $V_{dc} = 70$ V, interface inductance $L_C = 32$ mH, total ac resistance $R = 1.0$ Ω, and fundamental frequency $f = 60$ Hz.

Figure 9 shows the simulation results. By equation (11) and (12), the reactive power Q_c^* or equivalently the reactive current I_c^* needed to be injected into the utility system is computed. This gives $Q_c^* = 520.8$ var or desired reactive current $I_{cd}^* = 0$, $I_{cq}^* = 2.170$ A. In Figure 9, the multilevel inverter is connected to the utility line at $t = 100T = 1.667$ S. It can be seen that the voltage and current sources are out of phase before the multilevel inverter is connected. The modulation index m is computed according to (10), results in $m = 2.32$. Since m is in the range 1.18 through 2.4, $V_{dc}^* = V_{dc} = 70$ V will suffice. A PI controller is used to keep each capacitor voltage at 70 V. The PI gain is chosen as $K_p = K_I = 0.001$. From Figure 9, it can be seen after 1 or 2 cycles, the source voltage v_s and the i_s are in phase.

Figures 10 and 11 show the simulation results when the load is changed. The total reactive power $Q_c^* = 262.8$ var or desired reactive current $I_{cd}^* = 0$, $I_{cq}^* = 1.095$ A is needed for injection into the utility line. In Figure 10, the multilevel inverter is

connected to the utility line at $t = 100T = 1.667$ S. It can be seen that the voltage and current sources are out of phase before the multilevel inverter is connected. The modulation index m is again obtained using (10), giving $m = 2.439$. Since m is not in the range 1.18 through 2.4, then fix $m = 2.0$ and $V_{dc}^* = 85.35$ V (by equation (14)). A PI controller is again used to change each capacitor voltage equal to V_{dc}^*, where the PI gain is chosen as $K_p = K_I = 0.001$. From Figures 10 and 11, after 3 seconds, the source voltage v_s and the source current i_s are in phase.

VII. Conclusions

A cascaded multilevel inverter has been presented for static var compensation/generation application. This paper has introduced a control strategy to vary the level of the DC capacitor voltage so that use of the staircase switching scheme (with its inherent low THD) can be applicable for a wider range of modulation indices. The simulation results corresponded well with the predicted results.

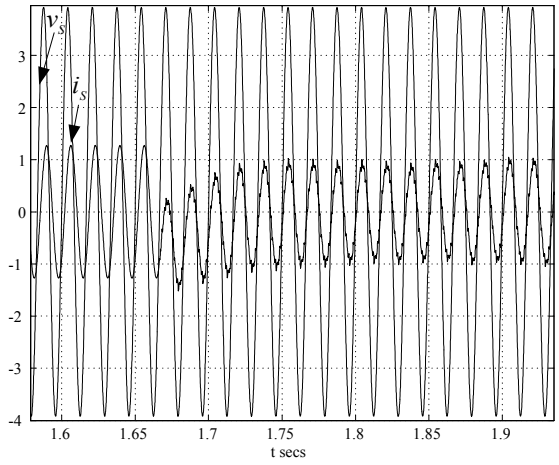

Fig. 9. Source voltage (scaled 0.02) v_s and source current i_s.

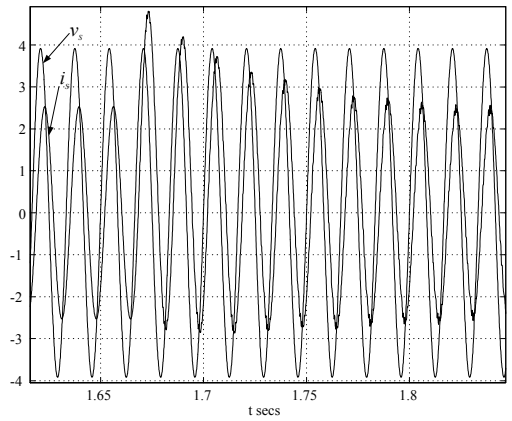

Fig. 10. Source voltage (scaled 0.02) v_s and source current i_s.

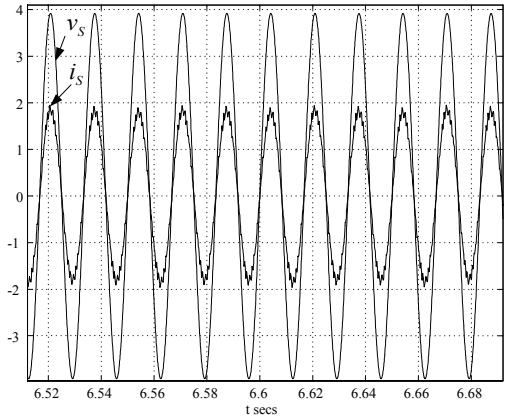

Fig. 11. Source voltage (scaled 0.02) v_s and source current i_s.

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