Modulation Index Regulation of a Multilevel Inverter for Static Var Compensation

Leon M. Tolbert, *Senior Member, IEEE*, John N. Chiasson, *Member, IEEE*,
and Fang Z. Peng, *Senior Member, IEEE*[1]

***Abstract*—A strategy is presented to minimize the voltage total harmonic distortion when controlling a multilevel converter to act as a static var compensator. Use of resultant theory has enabled the complete set of solutions to be found for switching a multilevel inverter's power electronic devices at the fundamental frequency while eliminating the lower order harmonics. A scheme is also presented to regulate the voltage levels of the multilevel inverter so that it operates in an optimum amplitude modulation index regime.**

***Index Terms*—static var compensation, multilevel inverter, resultants, harmonic elimination.**

I. Introduction

THE widespread use of non-linear loads and power electronic converters has increased the generation of non-sinusoidal and non-periodic currents in power systems. The compensation of this reactive, or nonactive, power is essential to minimizing transmission losses, regulating the supply voltage, and maximizing power transmission capability. Accordingly, considerable efforts have been undertaken to design and implement static var compensators (SVCs) to provide reactive power.

In addition to helping to achieve a near-unity power factor at its point of coupling, an SVC should be energy efficient, cost effective, and react quickly to changing line conditions. In [1] and [2], the multilevel converter has been proposed for static var compensation as it is energy efficient (due in part to its fundamental switching scheme) and cost effective because it does not require a transformer. However, the multilevel converter has challenges it must overcome to be a viable alternative to standard PWM methods or static var compensators that incorporate multiple phase shifting transformer connections. These include limiting the harmonic content of its output voltage and balancing the charge on its dc capacitors [5].

Because the individual power electronic devices in a multilevel converter can be controlled to switch at fundamental frequency, its generated harmonics are much lower in frequency than high carrier frequency based PWM systems [4]. One major concern in designing a static var compensator based on the multilevel inverter is to ensure that its total harmonic distortion (THD) is within allowable standards [3].

In this paper, the complete solution to the harmonic elimination problem for multilevel inverters switching at the fundamental frequency is given. This includes not only the fundamental staircase scheme, but all possible switching schemes at the fundamental frequency. This allows the control designer to choose the particular solution that gives the smallest THD.

It has been shown in [11] that the fundamental staircase scheme (Figure 2a) gives the lowest THD compared to the other possible switching schemes (see Figure 2). However, it has also been shown in [13] that switching angle solutions for the staircase scheme exist for only a limited range of the modulation index. It is desirable to operate the multilevel converter at modulation indices where lower frequency harmonics are eliminated and the higher frequency harmonics are a minimum. This paper presents a proposed scheme to control the voltage of each of the individual levels' capacitors in a way that the staircase scheme of Figure 2a can be used for a much larger range of the modulation index so the output voltage THD is kept to a minimum.

II. Multilevel Inverters

A transformerless multilevel inverter holds real promise as a technology for static var compensation. The general function of a multilevel inverter is to synthesize a desired ac waveform from several levels of dc voltages, which are capacitors in the case of a SVC. Additionally, the THD of the voltage waveform produced by the multilevel inverter must be minimized for it to have an efficient interface with the utility system. In medium to high voltage three-phase systems, the goal is normally to eliminate the odd non-triplen lower order harmonics (5^{th}, 7^{th}, 11^{th}, 13^{th}, etc.) and then filter the remaining higher order harmonics.

Figure 1(a) illustrates one multilevel converter topology – the cascaded H-bridges inverter. As illustrated in this figure, the converter is composed of a series of single-phase H-bridge inverter units. The desired voltage waveform can then be generated by combining the outputs of each of these H-bridge units to produce a staircase waveform that closely approximates a sine wave as shown in Fig. 1(b). Several of the single-phase multilevel inverter units shown in Fig. 1(a) can be connected in wye or delta for three-phase systems also. Other multilevel topologies have been proposed for static var compensation including the diode-clamped and capacitor-clamped (flying capacitor) topologies [17], [18].

L. M. Tolbert and J. N. Chiasson are with the Department of Electrical and Computer Engineering, The University of Tennessee, Knoxville, TN 37996-2100 USA (e-mail: tolbert@utk.edu, chiasson@utk.edu.

F. Z. Peng is with the Department of Electrical and Computer Engineering, Michigan State University, East Lansing, MI 48824-1226 USA (e-mail: fzpeng@egr.msu.edu).

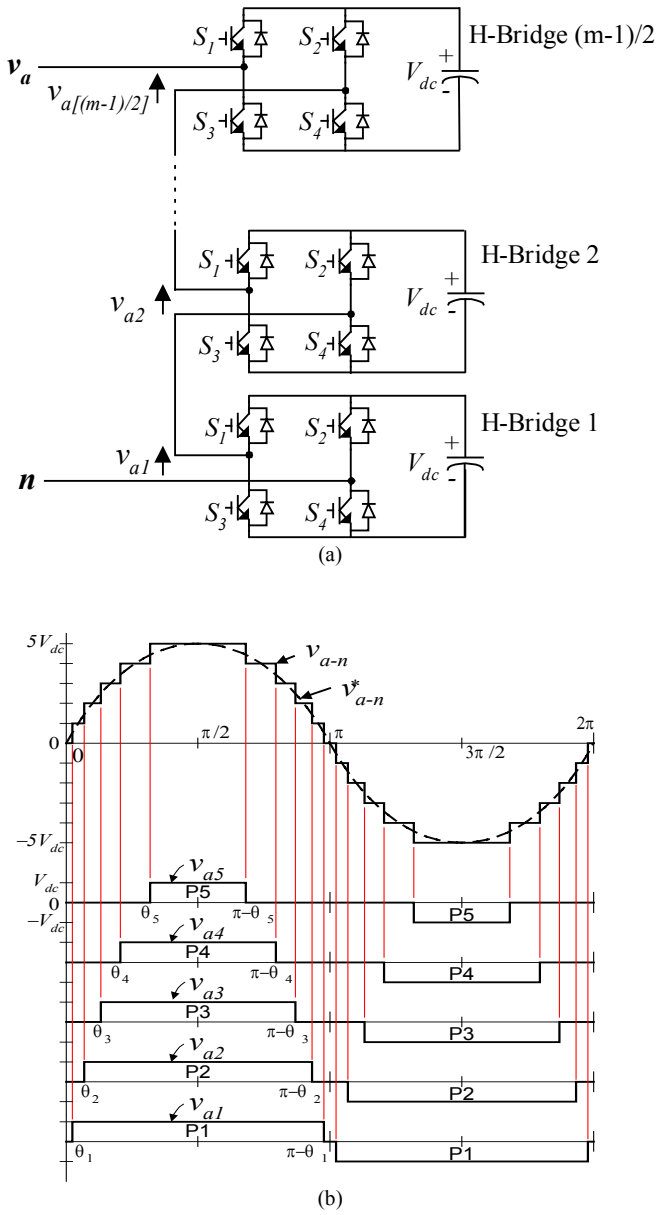


Fig. 1. (a) Multi-level cascaded H-bridges converter and (b) staircase output waveform.

As shown in Fig. 1, the output voltage v_{an} is composed of the output voltages of each of the individual H-bridges such that $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$. Also, for s dc voltage sources (capacitors), the number of output phase voltage levels in a cascaded H-bridges inverter is $2s + 1$, and the line-line voltage will have $4s + 1$ levels. The near-sinusoidal output voltage shown in Fig. 1(b) is produced with only fundamental frequency switching of individual power electronics devices. No high frequency PWM or the use of bulky, expensive phase-shifting transformers is necessary [4].

III. Mathematical Model of Switching

The staircase switching scheme shown in Fig. 1(b) is not the only possible low frequency switching scheme that can be used to eliminate lower-order harmonics in the multilevel converter's output voltage. To illustrate this point, Fig. 2 shows all of the possible switching schemes for a multilevel inverter with 3 separate dc sources per phase ($s = 3$) and with the number of switchings limited to 4 per quarter cycle. Note that Fig. 2(a) is a special case of Fig. 2(b) with $\theta_4 = \pi/2$. All of the switching schemes shown in Fig. 2(b)–(f) can eliminate the 5th, 7th, and 11th harmonics while producing the desired fundamental frequency voltage. These other schemes are considered because they may produce a voltage waveform with lower THD than the staircase method, particularly at lower amplitude modulation indices [6]-[9].

The waveforms shown in Fig. 2 can be expressed as the Fourier series expansion of the form:

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sin(n\omega t)\times\sum_{n}^{\infty}\frac{1}{n} \left(\ell_1\cos(n\theta_1)+\ell_2\cos(n\theta_2)+\ell_3\cos(n\theta_3)+\ell_4\cos(n\theta_4)\right) \quad (1)$$

where $0 \le \theta_1 \le \theta_2 \le \theta_3 \le \theta_4 \le \pi/2$ and $\ell_i = \pm 1$, depending on the switching scheme shown in the table given in (2).

Scheme	$\ell = (\ell_1, \ell_2, \ell_3, \ell_4)$
Fig. 2(b)	(+1, –1, +1, –1)
Fig. 2(c)	(+1, +1, +1, –1)
Fig. 2(d)	(+1, +1, –1, –1)
Fig. 2(e)	(+1, –1, +1, +1)
Fig. 2(f)	(+1, +1, –1, +1)

(2)

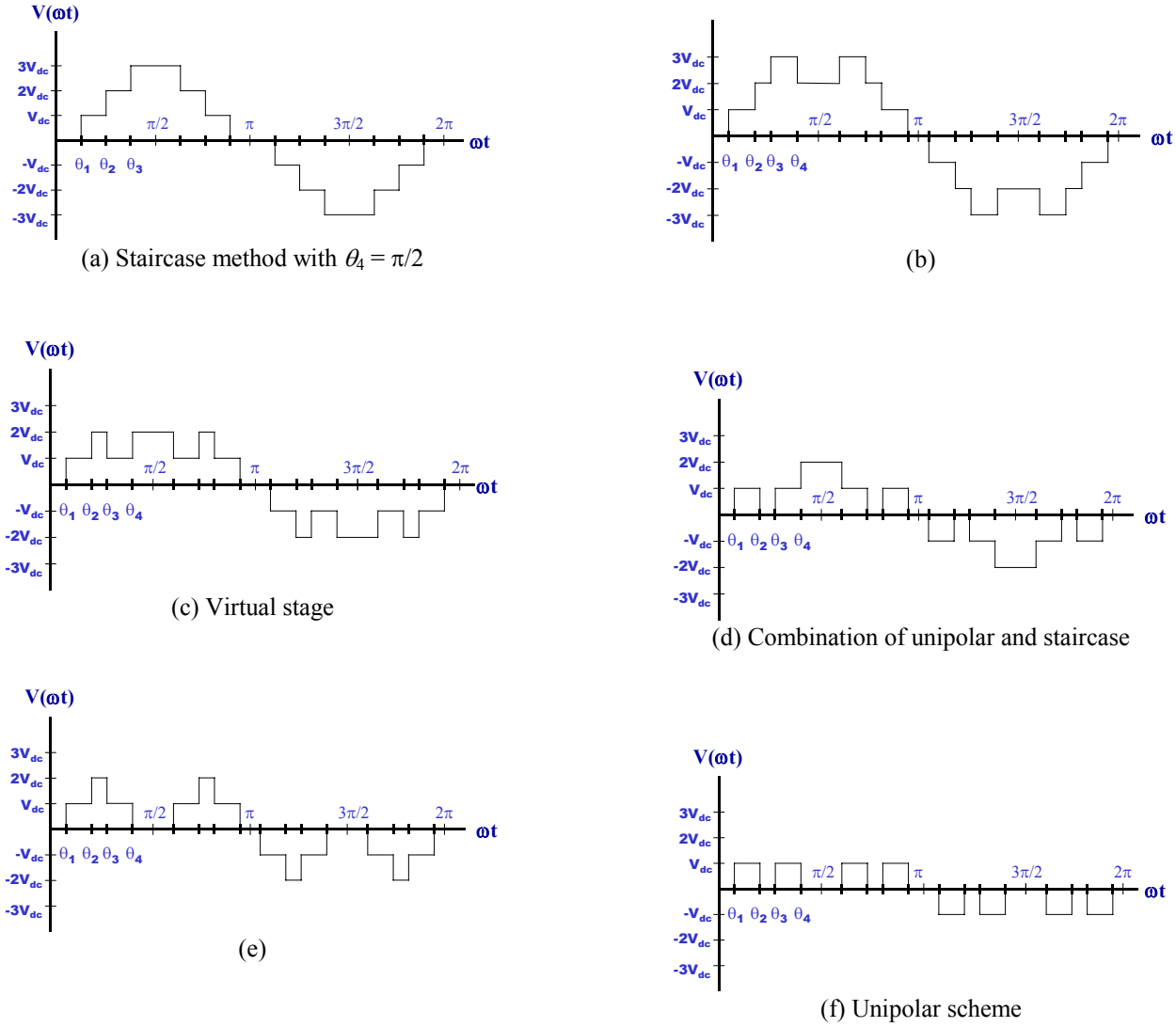
Because the waveforms produced are odd-symmetric, only the odd harmonics are present and the even harmonics are zero. By considering that $\cos(n(\pi-\theta_i)) = -\cos(n\theta_i)$ for n odd, and making the substitution $\theta_i' = \theta_i$ if $\ell_i = 1$ and $\theta_i' = \pi - \theta_i$ if $\ell_i = -1$, equation (1) may then be rewritten in the form

$$V(wt) = \frac{4V_{dc}}{\pi}\sin(nwt)\times\sum_{n}^{\infty}\frac{1}{n} \left(\ell_1\cos(n\theta_1')+\ell_2\cos(n\theta_2')+\ell_3\cos(n\theta_3')+\ell_4\cos(n\theta_4')\right) \quad (3)$$

The objective is then to choose the switching angles in (3) such that the desired fundamental is produced while the 5th, 7th, and 11th harmonics are eliminated. This can be formulated as where $m_a = \pi V/(4V_{dc})$ and V_1 is the rms value of the desired fundamental voltage.

One method to solving the set of transcendental equations given in (4) is the use of a Newton-Raphson technique. However, this technique requires a good initial guess at the angles and will only yield one set of solutions. Another

$$\begin{aligned} \cos(\theta_1')+\cos(\theta_2')+\cos(\theta_3')+\cos(\theta_4') &= sm_a \\ \cos(5\theta_1')+\cos(5\theta_2')+\cos(5\theta_3')+\cos(5\theta_4') &= 0 \\ \cos(7\theta_1')+\cos(7\theta_2')+\cos(7\theta_3')+\cos(7\theta_4') &= 0 \\ \cos(11\theta_1')+\cos(11\theta_2')+\cos(11\theta_3')+\cos(11\theta_4') &= 0 \end{aligned} \quad (4)$$



(a) Staircase method with $\theta_4 = \pi/2$

(b)

(c) Virtual stage

(d) Combination of unipolar and staircase

(e)

(f) Unipolar scheme

Fig. 2. Possible switching schemes for a multilevel inverter with s = 3.

approach is to use the trigonometric identities for $\cos(5\theta)$, $\cos(7\theta)$, and $\cos(11\theta)$ that expand these expressions into polynomial expressions in $\cos(\theta)$ and rewrite (4) as a set of polynomial equations. In other words, the system (4) is transformed into a set of four high-order polynomials in four unknowns. Because of the high order of the new polynomial equations, a systematic procedure known as elimination theory and notion of resultants is required to solve the equations. This is described in detail in [16].

Except for very high modulation indices, one can find a switching angle solution set for (at least) one of the schemes in Fig. 2 in order to achieve the fundamental voltage while eliminating the 5th and 7th harmonics. However, for those modulation indices for which the staircase scheme of Figure 2a can be used, the remaining THD will be smallest [11]. As a result, one would like the design of the SVC to be such that its nominal operating condition is for modulation indices in this range. This is discussed in the next sections.

IV. Switching Angle Results for 5-DC Source Case

As an illustration of where solutions to (4) exist, Fig. 3 shows all of the solutions for the staircase switching scheme illustrated in Fig. 1 for the case with 5 H-bridge levels. The solutions are plotted versus the parameters m where $m = sm_a$. As the plots show, solutions only exist in the intervals [1.88, 1.89], [2.21, 3.66], and [3.74, 4.23]. In these intervals, the desired fundamental converter voltage for the SVC can be produced with no 5th, 7th, 11th, or 13th harmonic content. For some of the intervals, two or three sets of solutions existed to (4). For these cases where multiple solutions exist, one typically would choose to implement the angle set that produce the lowest THD for the residual higher order harmonics. The residual THD through the 31st harmonic is shown for these solution sets in Fig. 4.

On the other hand, note that no solution existed for much of the rest of the m interval from [0, 5]. However, for much of those regions where no solution existed for the staircase waveform switching scheme, likely one of the other switching

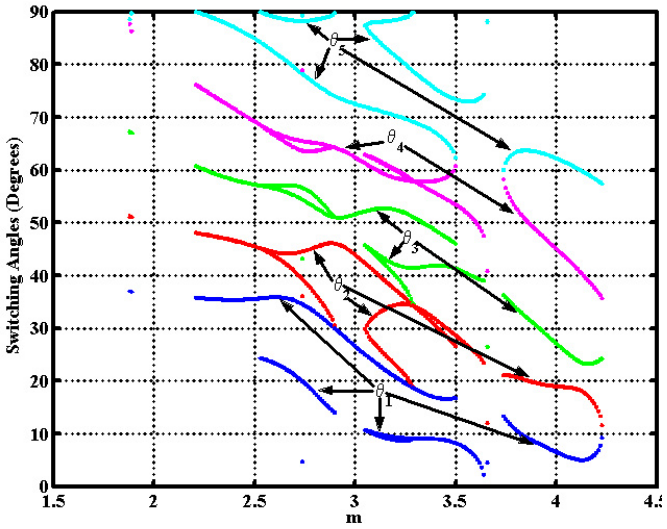


Fig. 3. Switching angles vs. m for a staircase waveform produced by a multilevel inverter with 5 H-bridges.

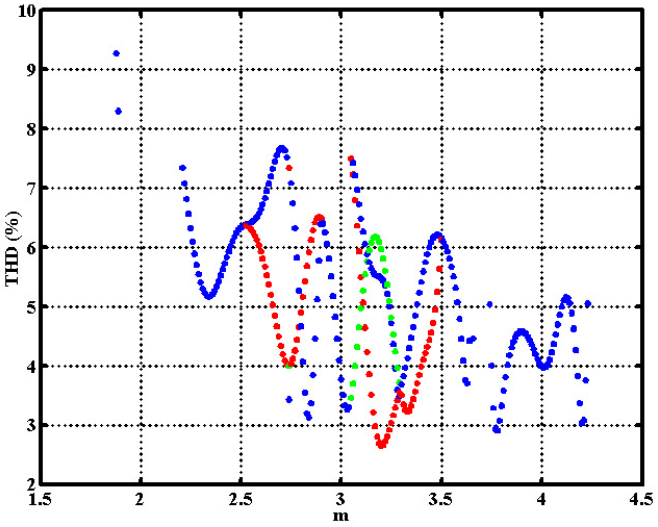


Fig. 4. The total harmonic distortion versus m for each solution set in Fig. 3.

methods illustrated in Fig. 2 would yield a solution. For each increment in the amplitude modulation index region (m_a from [0,1], the scheme that had a solution at that increment of the modulation index (meaning no low order harmonics) *and* that produced the lowest THD for the remaining higher order harmonics would then be chosen to be implemented in the actual SVC control.

It is desirable to operate the SVC at its minimum possible THD at all times. From Fig. 4, using the staircase switching scheme will yield a minimum THD of less than 3% at m = 3.2 (m_a = 3.2/5 = 0.64). Thus, it is desirable to operate the multilevel inverter close to this point at all times. The challenge is then to regulate the voltage levels of the H-bridges' dc capacitors such that the multilevel inverter is operating at a modulation index close to m_a = 0.64. The next section discusses a method to accomplish this.

V. Control of the DC Capacitor Voltages

The amplitude of the fundamental voltage is $V_1 = sm_aV_{dc}$, and the value of the capacitor voltages V_{dc} can be considered as an extra degree of freedom because V_1 can be obtained by varying m_a, V_{dc}, or both. A proposed controller is presented in Fig. 5 for the capacitor voltages to track a varying V_{dc} in order to keep the modulation index in a range for which the THD is a minimum. However, the capacitor voltages cannot be changed instantaneously so that the SVC operates at an optimum amplitude modulation index. In contrast, the switching angles can be changed at each time step of the controlling computer. It is anticipated then that for fast dynamic changes in V_1, V_{dc} will be held constant and m_a will be varied; but for slowly varying or long term changes in V_1, the capacitor voltages V_{dc} will be adjusted such that the modulation index at which the converter operates minimizes the THD of the output voltage.

The dynamic model relating the compensation current to the system and converter voltages for the SVC system shown in Fig. 5 can then be written as follows:

$$L_C(di_C/dt) + R_Ci_C = v_S - v_C \tag{5}$$

where $i_c = (i_{Ca}, i_{Cb}, i_{Cc})^T$ is the SVC current, $v_C = (v_{Ca}, v_{Cb}, v_{Cc})^T$ is the voltage at the output of the SVC, $v_S = (v_{Sa}, v_{Sb}, v_{Sc})^T$ is the source or utility voltage, and L_C and R_C are the inductance and resistance of the coupling inductor, respectively. Also, let

$$\begin{aligned} v_{Sa} &= V_S\cos\theta, \\ v_{Sb} &= V_S\cos(\theta + 2\pi/3), \\ v_{Sc} &= V_S\cos(\theta + 4\pi/3) \end{aligned} \tag{6}$$

Using the three-phase to two-phase and the synchronous reference frame transformation, (5) can then be rewritten in dq coordinates as

$$L_C\frac{d}{dt}\begin{bmatrix} i_{Cd} \\ i_{Cq} \end{bmatrix} + \omega L\begin{bmatrix} -i_{Cq} \\ i_{Cd} \end{bmatrix} + R_C\begin{bmatrix} i_{Cd} \\ i_{Cq} \end{bmatrix} = \begin{bmatrix} v_{Sd} \\ v_{Sq} \end{bmatrix} - \begin{bmatrix} v_{Cd} \\ v_{Cq} \end{bmatrix} \tag{7}$$

It then follows from (6) that

$$\begin{bmatrix} v_{Sd} \\ v_{Sq} \end{bmatrix} = \begin{bmatrix} V_S \\ 0 \end{bmatrix}$$

Several approaches can be taken to control the currents [2], with one scheme formulated as follows:

$$\begin{aligned} v_{Cd} &= v_{Sd} + \omega L_C i_{Cq} + K_1 i_{Cd} - (R_C + K_1)i^*_{Cd} \\ v_{Cq} &= v_{Sq} + \omega L_C i_{Cd} + K_1 i_{Cq} - (R_C + K_1)i^*_{Cq} \end{aligned}$$

where the reference currents are designated with an asterisk.

Using a PI-controller to change the s capacitor voltages and letting $C_{eq} = C/s$ yields a transfer function given as follows:

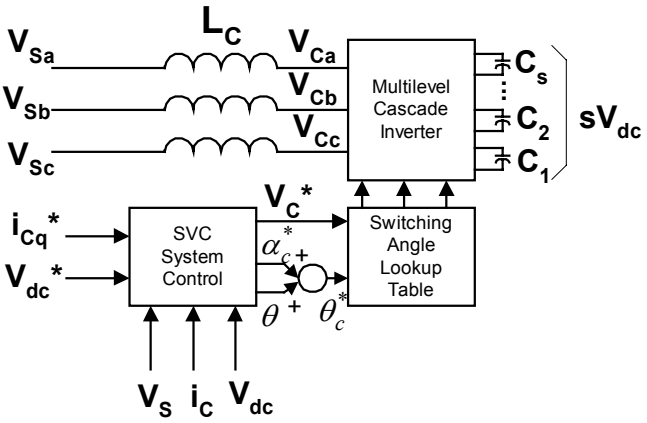
$$\frac{V_{dc}}{V_{dc}^*}(s) = \frac{sK_P + K_I}{s^2 C_{eq} + sK_P + K_I}$$

where s is the Laplace transform variable. The gains K_P, K_I are chosen so that V_{dc} quickly tracks V_{dc}* without requiring the multilevel inverter to attempt to produce a voltage that is higher than its capabilities.

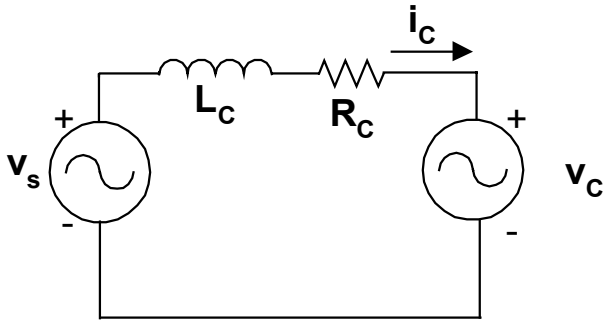
By selecting the appropriate switching scheme shown in Fig. 2, one can quickly (within one electrical cycle) produce the desired output voltage waveform. However, depending on the amplitude modulation index, this may mean that the output voltage has high THD. One can keep the voltage THD to be low by varying V_{dc}, but this may not respond fast enough.

III. Conclusions

In this paper, a strategy to minimize the voltage total harmonic distortion when controlling a multilevel converter to act as a static var compensator has been presented. Use of resultant theory has enabled an exhaustive set of solutions to be found for switching a multilevel inverter's power electronic devices at fundamental frequency and eliminate the lower order harmonics. The voltage levels of the multilevel inverter can be controlled so that it operates in an optimum amplitude modulation index regime that minimizes its output voltage THD.



(a)



(b)

Fig. 5. (a) System configuration and (b) equivalent circuit of the SVC system.

References

[1] F. Z. Peng, J. S. Lai, J. W. McKeever, J. VanCoevering, "A multilevel voltage-source inverter with separate dc sources for static var generation," *IEEE Trans. Industry Applications*, vol. 32, no. 4, Sept./Oct. 1996, pp. 1130-1138.

[2] F. Z. Peng, J. S. Lai, "Dynamic performance and control of a static var generator using cascade multilevel inverters," *IEEE Trans. Industry Applications*, vol. 33, no. 3, May/June 1997, pp. 748-755.

[3] IEEE Task Force, "Effects of harmonics on equipment," *IEEE Trans. Power Delivery*, vol. 8, no. 2, April 1993, pp. 672-680.

[4] J. S. Lai, F. Z. Peng, "Multilevel converters – a new breed of power converters," *IEEE Trans. Industry Applications*, vol. 32, no. 3, May/June 1996, pp. 509-517.

[5] F. Z. Peng, J. W. McKeever, D. J. Adams, "A power line conditioner using cascade multilevel inverters for distribution systems," *IEEE Trans. Industry Applications*, vol. 34, no. 6, Nov./Dec. 1998, pp. 1293-1298.

[6] P. N. Enjeti, P. D. Ziogal, J. F. Lindsay, "Programmed PWM techniques to eliminate harmonics: a critical evaluation," *IEEE Trans. Industry Applications*, vol. 26, no. 2, March/April 1990, pp. 302-316.

[7] N. Mohan, T. M. Undeland, W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, Second Edition, John Wiley and Sons, 1995.

[8] H. S. Patel, R. G. Hoft, "Generalized harmonic elimination and voltage control in thyristor inverters: part I – harmonic elimination," *IEEE Trans. Industry Applications*, vol. 9, no. 3, May/June 1973, pp. 310-317.

[9] H. S. Patel, R. G. Hoft, "Generalized harmonic elimination and voltage control in thyristor inverters: part II – voltage control technique," *IEEE Trans. Industry Applications*, vol. 10, no. 5, Sep./Oct. 1974, pp. 666-673.

[10] J. Chiasson, L. M. Tolbert, K. McKenzie, Z. Du, "Eliminating harmonics in a multilevel inverter using resultant theory," *IEEE Power Electronics Specialists Conference*, June 2002, Cairns, Australia, pp. 503-508.

[11] J. Chiasson, L. M. Tolbert, K. McKenzie, Z. Du, "Harmonic elimination in multilevel inverters," to appear in the proceedings of *IASTED 2003*, Feb 2003, Palm Springs, CA.

[12] L. M. Tolbert, J. Chiasson, K. McKenzie, Z. Du, "Elimination of harmonics in a multilevel converter with non-equal dc sources," *IEEE Applied Power Electronics Conference*, February 2003, Miami, Florida.

[13] J. Chiasson, L. M. Tolbert, K. McKenzie, Z. Du, "A complete solution to the harmonic elimination problem," *IEEE Applied Power Electronics Conference*, February 2003, Miami, Florida.

[14] L. M. Tolbert, F. Z. Peng, "Multilevel converters as utility interface for renewable energy systems," *IEEE Power Engineering Society Summer Meeting*, July 2000, Seattle, Washington, pp. 1271-1274.

[15] J. Sun, I. Grotstollen, "Pulsewidth modulation based on real-time solution of algebraic harmonic elimination equations," *IEEE International Conference on Industrial Electronics, Control and Instrumentation*, 1994, pp. 79-84.

[16] D. Cox, J. Little, D. O'Shea, *Ideals, Varieties, and Algorithms: An Introduction to Computational Algebraic Geometry and Commutativve Algebra,* Springer Verlag, 1996.

[17] C. Hochgraf, R. H. Lasseter, "A transformerless static synchronous compensator employing a multilevel inverter," *IEEE Trans. Power Delivery*, vol. 12, no. 2, April 1997, pp. 881-887.

[18] T. A. Meynard, H. Foch, "Multilevel converters and derived topologies for high power conversion," *IEEE International Conference on Industrial Electronics, Control, and Instrumentation*, 1995, pp. 21-26.

Biographies

Leon M. Tolbert (S 1989 – M 1991 – SM 1998) received the B.E.E., M.S., and Ph.D. in Electrical

Engineering from the Georgia Institute of Technology, Atlanta, Georgia

He joined the Engineering Division of Lockheed Martin Energy Systems in 1991 and worked on several electrical distribution projects at the three U.S. Department of Energy plants in Oak Ridge, TN. In 1997, he became a research engineer in the Power Electronics and Electric Machinery Research Center at the Oak Ridge National Laboratory. In 1999, he was appointed as an assistant professor in the Department of Electrical and Computer Engineering at the University of Tennessee, Knoxville. He is an adjunct participant at the Oak Ridge National Laboratory and conducts joint research at the National Transportation Research Center (NTRC). He does research in the areas of electric power conversion for distributed energy sources, motor drives, multilevel converters, hybrid electric vehicles, and application of SiC power electronics.

Dr. Tolbert is a registered Professional Engineer in the state of Tennessee. He is the recipient of a National Science Foundation CAREER Award and the 2001 IEEE Industry Applications Society Outstanding Young Member Award. He is an associate editor of the *IEEE Power Electronics Letters*.

John N. Chiasson (S 1982 – M 1984) received his Bachelor's in Mathematics from the University of Arizona, his M.S. in Electrical Engineering from Washington State University, and his Ph.D. in Controls from the University of Minnesota.

His work in industry started at Boeing Aerospace from 1978 to 1979 in the area of flight controls, guidance and navigation. From 1982-1983, he worked at Control Data in the area of CAD systems, and from 1984-1985 he worked at Honeywell Science and Technology Center in the area of inertial navigation. His latest stint in industry was from 1996-1999 at ABB Daimler-Benz Transportation where he worked in the development of AC motor propulsion systems, real-time simulators, and the stability analysis of AC propulsion systems. Since 1999, he has been on the faculty of Electrical and Computer Engineering at The University of Tennessee. He does research in the areas of the control of electric motor drives, multilevel converters, hybrid electric vehicles as well as mathematical systems theory.

Dr. Chiasson is an associate editor of the IEEE TRANSACTIONS ON CONTROL SYSTEMS TECHNOLOGY.

Fang Z. Peng (M 1993 – SM 1996) received the B.S. degree in electrical engineering from Wuhan University of Hydraulic and Electrical Engineering, China, in 1983 and the M.S. and Ph.D. degrees in electrical engineering from Nagaoka University of Technology, Japan, in 1987 and 1990, respectively.

He joined Toyo Electric Manufacturing Company, Ltd., from 1990 to 1992 as a research scientist and was engaged in research and development of active power filters, flexible ac transmission systems (FACTS) applications and motor drives. From 1992 to 1994, he worked with Tokyo Institute of Technology as a Research Assistant Professor, where he initiated a multilevel inverter program for FACTS applications and a speed-sensorless vector control project. From 1994 to 1997, he was a Research Assistant Professor at University of Tennessee, working for Oak Ridge National Laboratory (ORNL). In 1997, he became a staff member at ORNL, Lead (principal) Scientist of the Power Electronics and Electric Machinery Research Center. He is presently an associate professor in the Department of Electrical and Computer Engineering at Michigan State University.

Dr. Peng has received many awards including the 1996 First Prize Paper Award and the 1995 Second Prize Paper Award of Industrial Power Converter Committee in IEEE/IAS Annual Meeting; the 1996 Advanced Technology Award of the Inventors Clubs of America, Inc., the International Hall of Fame; the 1991 First Prize Paper Award in *IEEE Transactions on Industry Applications*; and the 1990 Best Paper Award in the Transactions of the IEE of Japan, the Promotion Award of Electrical Academy.