An SOI-based High-Voltage, High-Temperature Gate-Driver for SiC FET

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***Abstract*- A high-voltage and high-temperature gate-driver chip for SiC FET switches is designed and fabricated using 0.8-micron, 2-poly and 3-metal BCD on SOI process. It can generate output voltage swing from -5 V to 30 V and can operate up to 175ºC ambient temperature. This gate-driver chip is intended to drive SiC power FETs in DC-DC converters in a hybrid electric vehicle. The converter modules along with the gate-driver chip will be placed very close to the engine where the temperature can reach up to 175ºC. Successful operation of the chip at this temperature without heat sink and liquid cooling will help to achieve greater power-to-volume as well as power-to-weight ratios for the power electronics module. Initial test results presented in this paper also validate the simulation.**

I. INTRODUCTION

With ever increasing demand for miniaturization and weight reduction of power converters for the automobile industry, electronic circuits capable of operating at higher temperature (175°C or above) with minimal or no heat sink are in great demand. By removing the heat sink and long interconnects, order of magnitude savings in overall mass of the power electronic modules is achievable.

In all power electronic circuitry, a gate driver is an essential component to control the turning "on" and "off" of the power switches. Hence, a gate-driver integrated circuit (IC) capable of operating at elevated temperatures (≥ 175°C) will certainly contribute to the reduction of weight and volume of these modules. This work presents a high-temperature and high-voltage gate-driver IC for driving SiC FET switches that will be used in a DC-DC converter in hybrid electric vehicles. The SiC FET switches under consideration require gate signals in the range of −5 V to 30 V to control their switching operation.

The converter modules will be placed very close to the engine to reduce cabling length that will also help to avoid unreliability associated with the long cables. Thus, the ambient temperature of the gate-driver IC will be as high as 175°C. In this paper, a simple but effective gate-driver IC design is proposed which is capable of operating at this high temperature without a heat sink and can produce the required 20 kHz high voltage pulses at the gate of the SiC FET power switch. The design is supported with simulation and test results. Preliminary test results obtained from the fabricated chip validate the simulation results.

II. HIGH-TEMPERATURE GATE-DRIVER CIRCUIT

For FET-based power switches, different types of gate-driver circuits have been proposed in the literature [1]-[4]. Among these only the circuit reported in [4] is capable of operating at a junction temperature up to 200ºC, while others can work only up to 125°C. In high-temperature electronics, junction leakage is a major issue. Bulk CMOS processes suffer from significant leakage current that contributes to a higher junction temperature (above ambient).

SOI (Silicon-on-Insulator) technology, however, is more attractive for high temperature applications as it provides dielectric isolation that reduces junction leakage currents [7]. SOI also provides improved latch-up immunity, which ultimately increases the reliability of the circuit operation at higher temperature. Modern day processes offer the opportunity of integrating high-voltage devices along with low-voltage devices on SOI substrates. Such a process that combines the advantage of high-voltage devices with SOI technology was chosen for the design and implementation of the proposed gate driver.

The authors of [6] have presented a low-loss high-frequency half-bridge gate driver circuit on SOI for driving MOSFET switches. However, there is no mention of the temperature capability of the circuit. In this work, a similar circuit topology has been used with necessary modifications as required for high temperature operation and suitable drive signal generation for the SiC FET switches under consideration.

III. GATE-DRIVER CIRCUIT DESIGNED

A block diagram showing the gate driver circuit topology used in this work is shown in Fig. 1. This circuit has six distinct blocks. These are the half-bridge high-voltage transistor pair (M_H and M_L), low-side buffer, high-side buffer, bootstrap capacitor based charge pump, low-side to high-side level shifter (M_1, M_2, R_1, and R_2) and pulse-generator. The high- and low-side buffers drive the gates of the low-side and high-side transistors in the half-bridge output stage, respectively.

The bootstrap capacitor (C_B) based charge pump establishes a voltage above the available highest rail voltage that is used to generate the gate pulses for the high-side devices. The high-voltage level shifter converts the incoming digital input signal from the low-side voltage level to the high-side voltage level. The purpose of the pulse generator block is to generate the appropriate timing pulses (I_{ON} and I_{OFF}) to turn "on" and "off" the high-side transistor and synchronize it with the low-side

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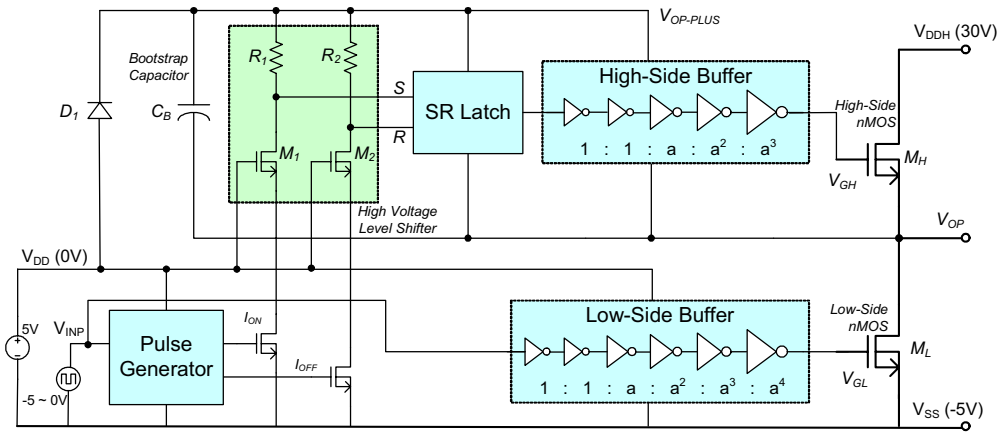


Fig. 1. Schematic of the proposed gate driver circuit.

transistor to avoid short circuit current through both high-voltage transistors in the output stage.

A. Half-bridge high-voltage output stage

The purpose of the half-bridge section is to connect the output to one of the two supply rail voltages. The key factors that should be considered when choosing the half-bridge topology are reverse breakdown voltage, on resistance and switching speed. The topology used in this circuit, as shown in Fig. 1, consists of two NMOS transistors stacked together. A NMOS transistor has lower on resistance and higher switching speed when compared to its PMOS counterpart. Since the peak-to-peak output voltage is large, it needs to switch fast to minimize switching losses. Gate voltage for the top NMOS device is either set at V_{SS} (when M_L is "on" & M_H is "off") or at $V_{OP}+V_{DD}-V_{D1}$ (when M_L is "off" & M_H is "on"), where V_{D1} is the diode voltage drop and V_{OP} is the output voltage generated by the circuit. To generate a voltage above the highest rail voltage, a bootstrap capacitor based charge pump is used [5, 6].

B. Charge pump using bootstrapped capacitor

The bootstrap circuit, consisting of a diode (D_1) and bootstrap capacitor (C_B), supplies a voltage level higher than the highest rail voltage available. This is required for the high-side buffer, SR latch, and level shifter in order to generate the required gate signal for the M_H transistor. The nodes V_{OP} and $V_{OP-PLUS}$ respectively act as the floating ground and as the positive supply rail for the high-side circuitry. Waveforms of V_{OP} and $V_{OP-PLUS}$ are shown in Fig. 2. When the output is low, C_B gets charged by the V_{DD} supply. When the top-side NMOS transistor is turned "on," the output voltage starts to increase making the diode reversed biased and C_B holds the voltage for the period during which the output is high. The purpose of the capacitor is to provide the required gate charge to the high-side NMOS transistor. The capacitance value is described by [5]:

$$C_B \quad \frac{2Q_{G-high}}{V_{DD}-V_{ON}-V_{GH}} \qquad (1)$$

where Q_{G_high} is the charge required to turn "on" the M_H transistor, V_{DD} is the voltage that is used to charge C_B when the output is low, V_{ON} is the diode forward voltage drop when C_B is being charged and V_{GH} is the gate-source voltage of M_H. The value of C_B is typically on the order of nano Farads, which makes it difficult to be integrated on the SOI chip. To reduce the number of external components, the diode D_1 is integrated in the chip.

C. Pulse generator

The pulse generator block provides two pulses with very short duration at the rising and falling edges of the input signal. These are shown in Fig. 3 as I_{ON} and I_{OFF}. These two signals are used to set and reset the SR latch. When the input signal goes "high," then it turns "on" the low-side NMOS switch.

At that instance it is necessary to force the high-side NMOS to switch "off". The I_{ON} pulse sets the SR latch to $V_{OP-PLUS}$. Since the latch output is passed through an inverting buffer, the V_{GS} of the high-side NMOS switch becomes zero to ensure that the transistor is "off". Similarly, when the input signal goes "low", the I_{OFF} pulse resets the latch and the high-side transistor turns "on", and the output is then connected to V_{DDH}.

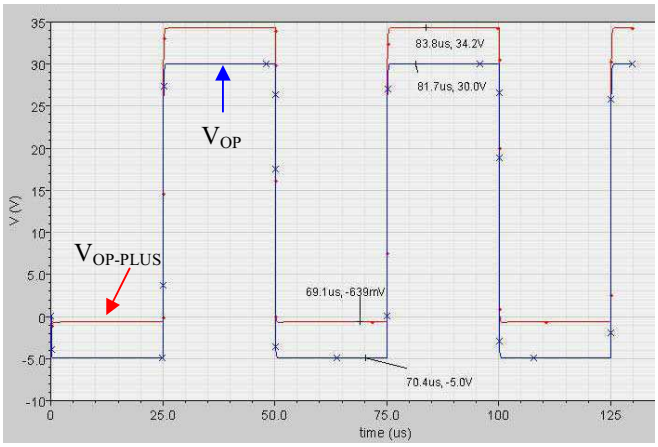


Fig. 2. Wave shapes of the V_{OP} and $V_{OP-PLUS}$.

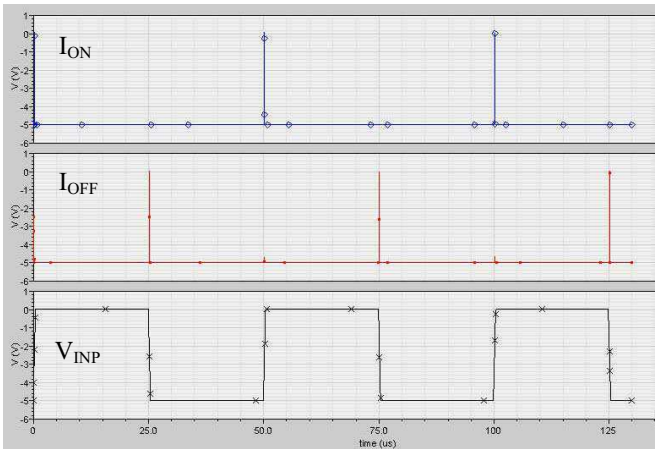


Fig. 3. Simulated plot showing I_{ON} and I_{OFF} pulses generated by the pulse-generator block.

D. *Level shifting of control signal*

The gate driver needs to produce an output voltage swing of 35 V from the 5 V CMOS logic input. Hence, a level-shifting circuit is required to convert the low-level control signals to the desired high-voltage level to generate the gate voltage for the M_H transistor. The high-side transistor's source is connected to the output terminal. Therefore, its gate voltage needs to be either at V_{OP} (to turn it "off") or at $V_{OP\text{-}PLUS} = V_{OP} + V_{DD}\text{-}V_{D1}$ (to turn it "on"). Two high-voltage NMOS transistors (M_1 and M_2) along with two resistors R_1 and R_2 translate the low-level input signal to the high-voltage level between V_{OP} and $V_{OP\text{-}PLUS}$. They turn "on" alternately for a very short period, allowing short current pulses to flow through the resistors from the high- to low-side. The voltage drops across R1 and R2 due to these current pulses provide the "set" and "reset" signals for the active-low latch, which in turn generates the proper gate signal for the high-side transistor.

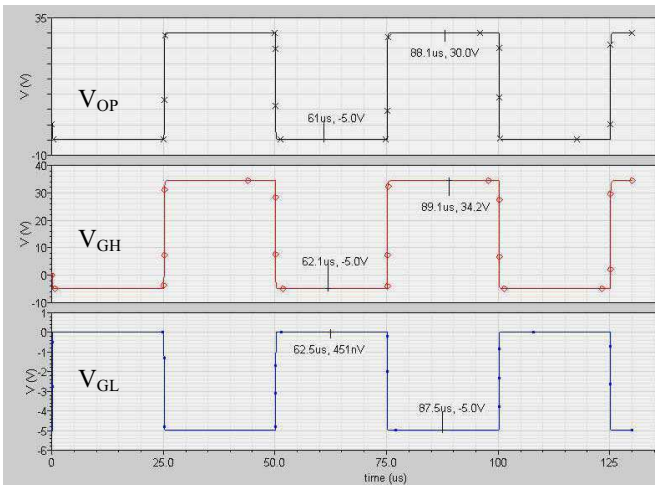


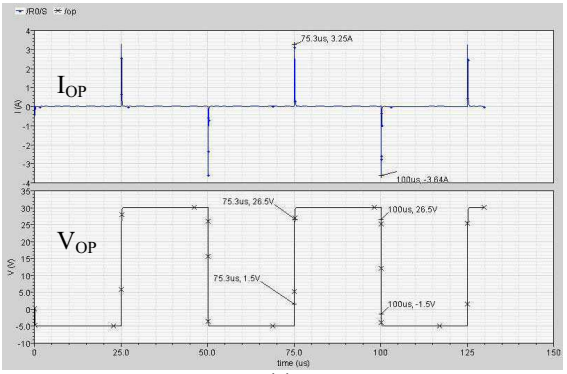
Fig. 4. Simulated plot showing the high-side and low-side gate signals.

E. *High and low- side buffer*

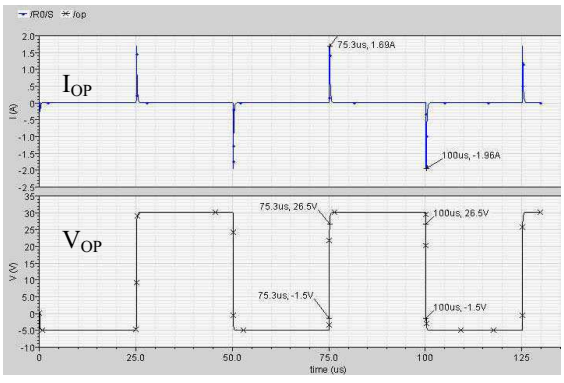
Both transistors of the half-bridge stage are comprised of a large number of parallel-connected high voltage transistors. Hence, both transistors have large gate capacitance, requiring large transient currents to drive them. To meet this requirement, multi-stage buffers with gradually increasing sizes (exponential horn) are added to drive the high- and low-side transistors. The gate-to-source signals V_{GH} and V_{GL} respectively for transistors M_H and M_L transistors are shown in Fig. 4.

IV. Simulation Results

Schematic level simulations were performed over temperature from −40°C up to 175°C. The circuit was simulated with a capacitance load of 10 nF in series with 10 Ω resistance to resemble the load condition (gate of SiC FET power switches). Fig. 5 shows the output voltage and current generated by the gate driver circuit at 175°C and −40°C temperature. From simulation it was observed that other than the switching instances, the output current is zero for the rest of the input signal period to ensure complementary turn "on" and "off" of the half-bridge stage transistors. This will also reduce the power dissipation through these devices and keep the junction temperature closer to the ambient temperature. Simulation



(a)



(b)

Fig. 5. Simulated plot showing the gate-driver output current and voltage (a) at -40^0C and (b) at 175^0C

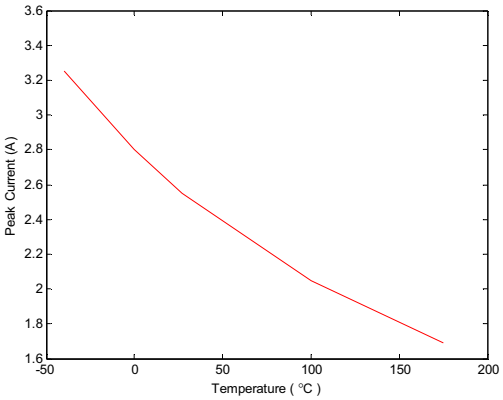


Fig. 6. Output peak-current vs Temperature.

was performed using foundry-provided models. Bond wire and package parasitic inductance and resistance were included in the simulation. Simulation results also show that the peak current delivering capacity of the driver decreases with an increase in temperature. Fig. 6 shows the maximum current generated by the gate-driver at different temperatures.

V. Measurement Results

The chip was designed and fabricated using 0.8 micron, 3-metal and 2-poly BCD on SOI process. Fig. 7 shows the chip microphotograph. The gate driver circuit occupies an area of 3.6 mm^2 (2,240 µm × 1,600 µm) including pads and ESD protections. The two high-voltage NMOS devices of the half-bridge output stage occupy a major portion of the chip area. They are sized (W/L = 24,000 µm/1.6 µm) to provide large peak current as needed to obtain acceptable rise and fall times. Each of these NMOS transistors is comprised of six hundred 45 V NMOS devices (W = 40 µm) connected in parallel. The high-voltage devices are well isolated from the low-voltage devices through a thick dielectric layer. The layout of the high-voltage devices resembles a "race-track" structure [8].

Multiple pad connections are used for the power supply and output nodes to minimize the parasitic bond wire inductance. All critical metal interconnects are made thick to avoid electromigration issues that are enhanced at higher temperatures. The chip was bonded in a LDCC44 package which is capable to operate above 200ºC. Test boards made of polyimide material are currently being used for high temperature testing of the chip. High temperature solder and wires are used for reliable testing of the chip.

Fig. 8 shows the gate driver signal generated by the chip at 175ºC ambient temperature with series connected 10 Ω and 10 nF load. Rising and falling edges are also magnified in Fig. 8. Tests were conducted inside an environmental chamber. Readings were taken 15 minutes after the temperature of the chamber reaches the desired level. Table 1 shows the 10% to 90% rise-time and 90% to 10% fall-time of the generated gate signals at different temperatures and with load.

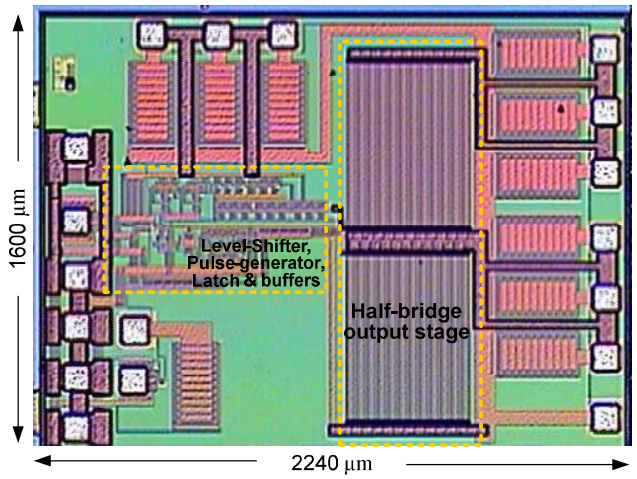


Fig. 7. Micrograph of the chip.

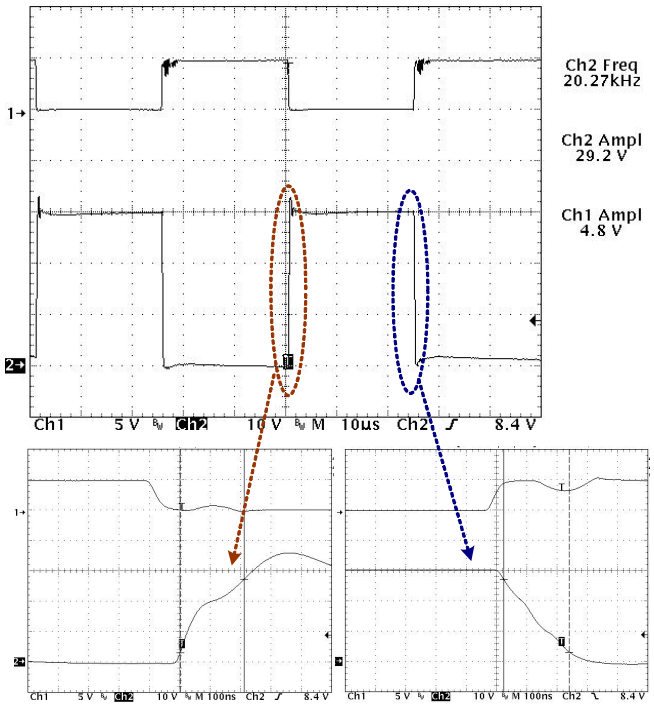


Fig. 8. Chip output at 175ºC with series connected 10 Ω and 10 nF load.

Table 1. Rise-time and fall-time at different ambient temperature

Temperature	$t_{rise\text{-}time}$ (nsec) (10%~90%)	$t_{fall\text{-}time}$ (nsec) (90%~10%)
27ºC	200	78
85ºC	204	90
150ºC	208	158
175ºC	210	216

VI. CONCLUSIONS

The high-temperature and high-voltage gate-driver circuit presented in this paper is part of a research effort to design a heat-sink-less DC-DC converter module for hybrid electric vehicles that can be placed close to the engine. The performance of the circuit looks promising based on the simulation results. Test results so far obtained closely matches with the simulations results. More tests will be conducted to evaluate the performance of this first generation chip, and based on the experience learned the design will be enhanced as necessary, and a second generation of the chip will be fabricated and tested.

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